

Polyimide Restructuring

Application for Printed Leadfree Bump Integrity Improvement

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Abstract

Polyimide is a widely used passivation layer on top of a semiconductor die. In flipchip, this is used as a barrier to protect the die from stress brought about by the difference in coefficient of thermal expansion between the silicon, the bump, the underfill, and the substrate. Use of polyimide has become even more popular with the use of the more brittle lowK dielectric on nanoscale die technology. A trade off however is that the polyimide has shown weakness in adhesion to the underfill compared to the conventional SiN/USG passivation layer. An added value for the polyimide use is that when designed properly it can also provide additional protection to the bump which can be useful now as leadfree bump is getting more and more attention with the speculation that ROHS eutectic bump exemption is coming to an end by 2010. The industry is now searching for an economical leadfree bump solution. Several technologies being developed focuses on plated bump technology as this has a more robust UBM layer compared to printed bump UBM, however, the plated bump is more expensive than printed bump. This paper will discuss how the polyimide layer when restructured can offer extra protection to the printed leadfree bump, including discussions on how the polyimide can be restructured to improve it's adhesion to the underfill.

1.0 Introduction

The industry is closely monitoring if the EU Commission will grant an extension to the exemptions of the RoHS regulation (Directive 2002/95/EC), specially the use of "lead in solders to complete a viable electrical connection between semiconductor die and carrier within integrated circuit Flip Chip packages" [1]. As it is not clear if an extension of this exemption will be granted, it is prudent to have the technology and process available as a backup plan. If the EU Commission's decisions are not favorable, then the industry needs to be ready to implement the new technology and process in high volume production. Several technologies that allows the use of leadfree bumps are expensive as they are mostly focused on plating bump technology, not to mention the cost of setting up additional infrastructure to support the production volume demand. This also undermines the worth of the present printed bump infrastructure as uncertainty is looming on it's value to leadfree bump application. The following discussion will describe how restructuring the polyimide layer can be used to enable the current printed bump technology and equipment for leadfree bump application. Weakness on the adhesion of the polyimide to the underfill will also be discussed and the solution to improve this adhesion.

2.0 Problem Description

The brittleness and the weakness of the IMC layer of a leadfree bump has been one of the biggest concerns in the transition to leadfree bump. Lead-free solder materials are also relatively less ductile than eutectic solder and this increased stiffness can lead to a significant stress to make the brittle intermetallic crack, particularly where operating temperatures are high or where there is a significant mismatch between the coefficients of thermal expansion between the die and the substrate. Adding to this problem is that the intermetallic layer is directly at the corner interface of the bump, the die, and the underfill where the stress is highest. Figure 1 shows a typical cross section of this structure. This is further shown on figure 2 which is the magnified view of a portion of figure 1 circumscribed by a circle labeled as A. This figure shows that the stress concentration center is located exactly at the corner between the die, underfill, and the brittle IMC layer.

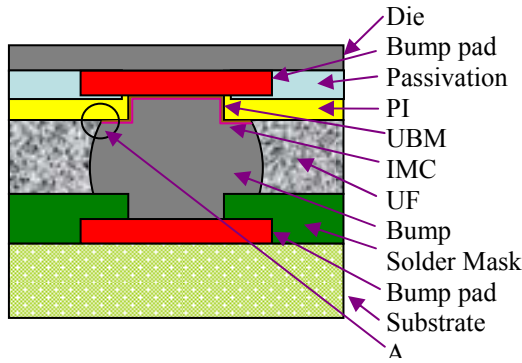


Figure 1. Typical cross section diagram of a FC package with printed bump structure.

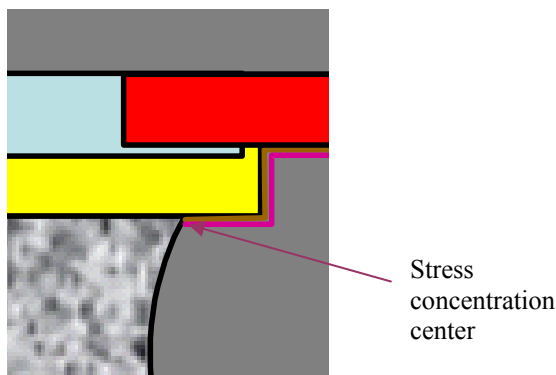


Figure 2. Magnified view of figure 1 circumscribed by a circle labeled as A.

3.0 Common Approach and Industry Solution

The most common approach to protect the leadfree bump and it's IMC layer is to use a higher Tg underfill. Another solution is to use thicker UBM which can only be achieved using plating process. The following items will discuss both the merits and disadvantages of each approach.

3.1 Higher Tg Underfill

The most common question for this topic is how high should the Tg be? Shown in table 1 below are some of the most common underfill property range.

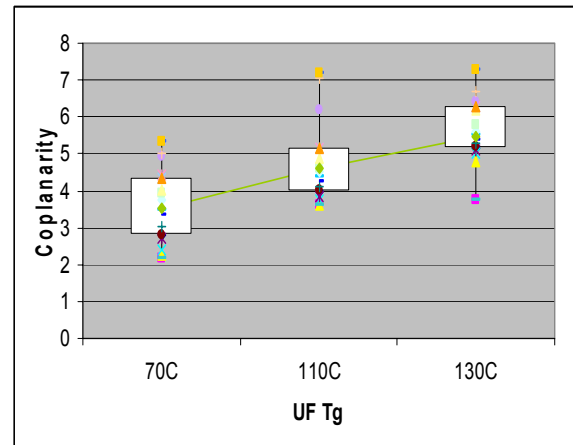
Table 1. Common underfill property range

Item	Unit	Common property range
Composition		Phenol or Amine base
Filler Loading (by weight)	%	55 ~ 65
Filler size Ave, Max	um	0.6 ~ 10
Viscosity @25C	Pa.s	7 ~ 60
Tg (Glass Transition Temperature)	C	60 ~ 130
CTE α_1	ppm/C	24 ~ 32
CTE α_2	ppm/C	90 ~ 120
Young's Modulus (Below Tg)	G Pa	7 ~ 11
Young's Modulus (Above Tg)	G Pa	0.03 ~ 0.11

During temperature cycling or high temperature operation, the interface between the die and the substrate takes the stress brought about by the CTE mismatch between the die and the substrate. Below Tg, the underfill modulus is high so at this stage the underfill distributes the stress on a bigger area thus the stress on the bumps are reduced. Above Tg, the underfill modulus drops down and the bump protection is also reduced. This means the higher the underfill Tg, the better protection for the bumps. Package level temperature cycling is normally done at condition B where the max temperature is 125C. Normal operating temperature of a package also does not exceed 125C so this temperature is ideal for the underfill to protect the bump.

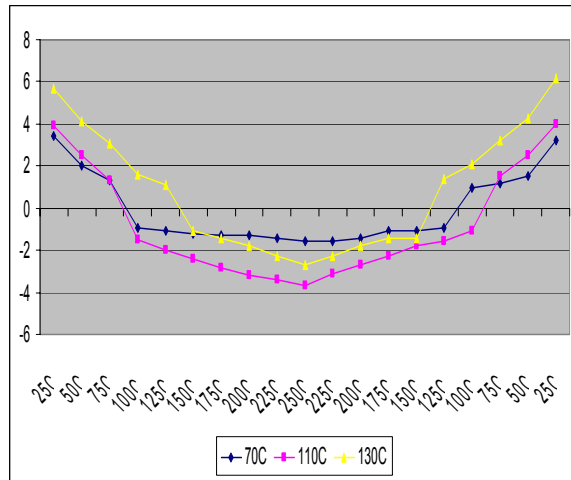
One downside of using a high Tg underfill is that the package warpage at room temperature becomes bigger. This mechanism is related to the UF Tg as this is the point where the UF hardens and engages the CTE interaction between the substrate and the die. Since the substrate CTE is about 8x higher than the die, the substrate will shrink faster and the higher the Tg of the UF is, the longer the substrate shrinkage interacts with the die thus causing a higher package warpage. Table 2 below shows an actual coplanarity data comparison using the same package structure with different UF Tg at 70C, 110C, and 130C.

Table 2. Coplanarity comparison between different underfill UF with low, medium, and high Tg



Shadow moiré was also performed to analyze the behavior of the package at elevated temperature using these different UF. As shown on table 3 below, the underfills with higher Tg exhibited higher room temperature warpage and a bigger warpage change between room temperature and elevated temperature.

Table 3. Shadow moiré comparison between different UF with low, medium, and high Tg.



Another downside of high Tg underfill is that for dice with lowK dielectrics, the stress on the die remains high during temperature cycling because the UF modulus is maintained high below Tg. This combined with a bigger package warpage and warpage change in varying temperature can cause the lowK dielectric to crack.

3.2 Plated Bump Process

Shown in figure 3 below is a common cross section of a plated bump. The top UBM layer connected to the bump is thick which provides the elevation needed to move the intermetallic layer away from the stress concentration center. This is further shown on figure 4 which is the magnified view of a portion of figure 3 circumscribed by a circle labeled as A'. This figure shows that the stress concentration center is now between the die, underfill, and the less ductile solder instead of the more brittle IMC layer.

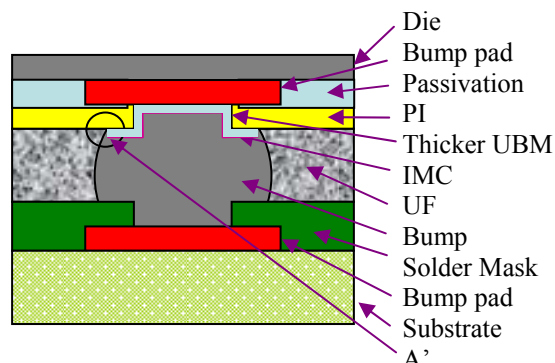


Figure 3. Typical cross section diagram of a FC package with plated bump structure.

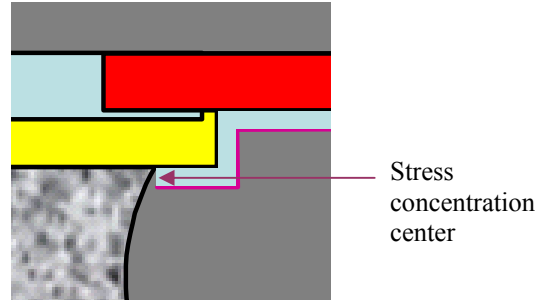


Figure 4. Magnified view of figure 3 circumscribed by a circle labeled as A'.

The downside in using plated leadfree bump process is that this is more expensive compared to printed bump process. The deposition rate also becomes slower by about 40% compared to high lead bump plating process which majority of the plated bump capacity is allocated on. This means that once the industry converts to plated leadfree bump the overall plating capacity will be reduced by 40%.

4.0 The Printed Leadfree Bump Solution

In order to improve the printed leadfree bump structure, we need to find a way to protect the brittle IMC layer or to move it away from the stress concentration corner. Also, in order for this solution to be economical, use of the current equipment, process, and infrastructure has to be utilized. These items will be discussed below.

4.1 The PI Over UBM Approach

The difficulty with the conventional technique stems from the relative positions of the polyimide layer, the under bump metallization layer and the solder bumps. Because the polyimide layer is essentially separated from the solder bumps by the under bump metallization layer, the stress reducing abilities of the polyimide layer are not available to the solder bumps. Accordingly, high mechanical stresses may be inflicted on the solder bumps, particularly at the edges of the solder bumps near the interfaces with the under bump metallization layer. The stresses can lead to crack in the solders bumps. If the stresses are acute enough, mechanical failure of the solder bumps can occur and produce electrical device failure. The PI over UBM solution is directed to overcoming or reducing the effects of one or more of the foregoing disadvantages. The following figures 5 and 6 will show the structure of PI over UBM.

Shown in figure 5 below is a cross section view of PI over UBM structure. The UBM layer has been methodically moved between the die passivation and the polyimide layer. The opening on the PI layer exposes a portion of the UBM layer

where the bump is deposited and solderjoint is formed. As shown in figure 6 which is a portion of figure 5 circumscribed by a circle labeled as A'', this structure has strategically moved the intermetallic layer away from the original stress concentration corner. Although the new position of the IMC has a stress concentration center of its own between the die, the PI, and the IMC layer, the stress reducing ability of the polyimide is now available to protect this corner at application temperature and temperature cycling as the typical Tg of the PI is greater than 300 degrees celcius.

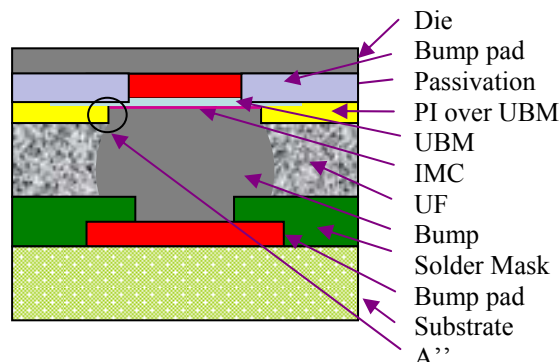


Figure 5. Typical cross section diagram of a FC package with printed bump using PI over UBM structure.

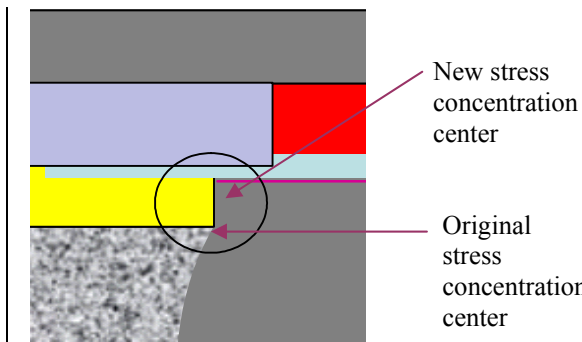


Figure 6. Magnified view of figure 5 circumscribed by a circle labeled as A''.

4.2 The PI Over UBM Result

The test vehicle used to validate the reliability of PI over UBM is a 33mm x 33mm package with a 10mm x 10mm die using Sn/Cu leadfree bump. The parts were subjected to reliability test with the conditions shown in table 4.

The PI over UBM test vehicle was able to pass all the reliability tests. Test to failure was even conducted by continuing TCT to 2000cycles and the result was also good. For comparison, the data from previous tests done on this structure using the normal PI structure failed at TCT300 due to bump failures

Table 4. Reliability test conditions.

Test	Condition
Moisture sensitivity level	JESD22-A113/J-STD-020 LEVEL-4, 255+5/-0C reflow temp
Highly accelerated stress test (Unbiased)	JEDEC 22-A118; 130°C/85%RH3.5PSIG; 100H
Temperature cycling test	JEDEC 22-A104; -55°C~125°C ; 1000 cycles
High temperature storage	JEDEC 22-A103; 150°C ; 1000H ; no preconditioning
Multiple reflow	255+5/-0C reflow temp, 5X to failure

5.0 Polyimide to UF Adhesion Improvement

When the flip-chip package is exposed to stress, the adhesive bond between the polyimide layer and the underfill material may weaken. The weakened adhesive bond may result in a delamination between the polyimide layer and the underfill material which is undesirable. One method used to try to overcome this problem involves treating the polyimide layer such as by plasma etching or any other suitable method. Treating the surface results in a rougher surface area by introducing submicron valleys or other configurations, which aids in adhering the polyimide layer to the underfill material. In another method, adhesive properties of the underfill material or the polyimide material may be altered to increase bonding properties. In yet another method, the surface of polyimide layer may be cleaned with an additional cleaning process during manufacture. However, these methods mentioned not only increases manufacturing costs but more importantly these methods still relies on an adhesive surface bond which may weaken under certain stress conditions.

It is therefore desirable to provide, among other things, an integrated circuit having a polyimide layer that attaches to an underfill material in an improved manner. A method to achieve this is by introducing structured mechanical locking mechanisms between the polyimide and the underfill. An exemplary structure of such method is the polyimide anchor hole.

The figures below will show the comparison between a normal PI structure as shown in figure 7 and a modified PI structure with anchor holes as shown in figure 8. The PI anchor holes are created at the same time the PI opening on the bump areas are created thus this method does not require

additional process step and does not have any cost adder.

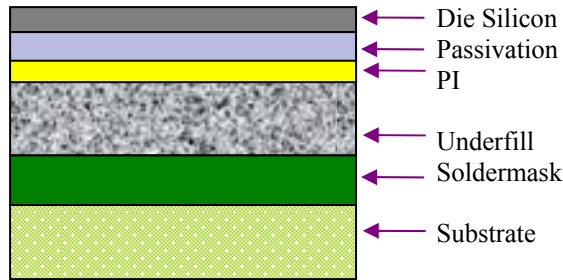


Figure 7. Typical cross section diagram of a FC package showing the substrate and the die with underfill in between them.

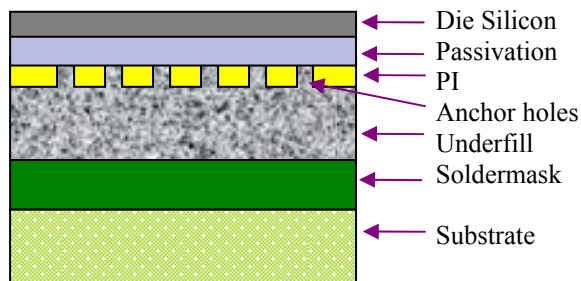


Figure 8. Modified cross section diagram of figure 7 showing the PI anchor holes mechanically locking the underfill to the PI structure as the underfill fills up the holes.

The PI anchor hole structure was able to pass all the reliability tests shown in table 4. For comparison, the data from previous tests done on this structure using the normal PI structure started to have PI to UF delamination after preconditioning reflow.

6.0 Summary

This paper has shown how the current polyimide structure can be changed to overcome disadvantages of using printed leadfree bump process where the polyimide goes over the UBM thus effectively transferring the IMC stress concentration center to a position where the polyimide offers the maximum protection to the IMC at application and stress temperature. This work has been used as basis in doing additional evaluation on different leadfree alloys and underfill in consideration for leadfree and ultra lowK die application.

This paper has also shown how the polyimide to underfill adhesion can be improved by using structured mechanical locking mechanisms instead of just relying on the polyimide and underfill adhesive surface bond. This work has lead to the use of the PI anchor hole design on actual products.

Numerous US and international patents were filed on the PI over UBM structure and the PI structured mechanical locking structure.

References

1.0 DIRECTIVE 2002/95/EC OF THE EUROPEAN PARLIAMENT AND OF THE COUNCIL on the restriction of the use of certain hazardous substances in electrical and electronic equipment, COMMISSION DECISION of 21 October 2005, Annex 15.