

Thermal Verification of a High-Temperature Power Package Utilizing Silicon Carbide Devices

R. Shaw, B. McPherson, J. Hornberger, A. Lostetter
Arkansas Power Electronics International, Inc.
535 W. Research Blvd. Suite 209
Fayetteville, AR 72701
Phone: 479-443-5759
Email: rshaw@apei.net

and

K. Okumura, T. Otsuka
ROHM CO., LTD.
21 Saiin Mizosaki-cho
Ukyo-ku, Kyoto 615-8585 Japan

Abstract

The researchers at Arkansas Power Electronics International, Inc. and ROHM CO., LTD. have simulated and tested high-temperature packaging technologies for SiC devices in an effort to develop more accurate modeling parameters for future applications. The laboratory test consists of parallel SiC power DMOSFETs, manufactured by Rohm, and SiC power VJFETs operating under self-regulating current sharing conditions.

To produce accurate thermal simulations, thermal models require numerous design parameters that are constrained to strict tolerances. Moreover, this presents an interesting challenge at junction temperatures (T_j) over 175 °C as most individual components have not been previously tested or verified at these temperatures. To extract these parameters at high-temperatures, the researchers have modeled a complete thermal system (including bare die, substrate, package, heatsink, and all thermal interfaces between said components) then built and tested an identical system to characterize the system's parameters over temperature. Specifically, the advantages between different types of thermal interfaces, including die attaches, substrate attaches, and thermal greases, were characterized over temperature. A high resolution thermal imaging camera was used to capture surface temperatures of the system to compare with simulation results. Due to mismatches in emissivity between components, multiple high-temperature conformal coatings were tested and characterized over temperature, as well. In this paper, the researchers will present the results of the laboratory testing that included the characterization of SiC DMOSFETs and SiC VJFETs operating up to 300 °C, as well as the thermal simulation results.

Key Words: High-temperature packaging, Extreme environment packaging, Thermal model verification

1.0 Introduction

Silicon carbide (SiC) power devices have long been a very attractive solution to high power modules due to their ability to operate at high-temperature (upwards of $T_j = 600$ °C) [1]. Thanks to recent improvements in manufacturing reliability, a few SiC power devices are readily available in the commercial market. As these devices become more prominent in the commercial arena, designers must adapt to the unique design rules that are required by operating at junction temperatures (T_j) over 175 °C.

By exploiting the high-temperature operation of SiC power devices, designers are able to reduce the volumetric and gravimetric impact that the cooling system can have for a given application [2-5]. However, this introduces the challenge of selecting appropriate packaging materials that can handle high-temperature operation.

This paper will introduce initial thermal characterization of two high-temperature die and substrate attach methods, 95Pb/5Sn solder paste and silver loaded glass epoxy. Also, thermal interface materials, including high-temperature thermal

grease, thermal pad, and graphite paste will be characterized. Experiments were also conducted with no thermal interface material to provide a baseline for subsequent materials.

Datasheets rarely supply thermal characteristics at any point over room temperature for a given material; this leaves the designer with a large variable in the overall system when designing for high-temperature applications. The purpose of this paper is not to validate or dispute manufacturers' given parameters but to show how different thermal interfaces can affect the system, which consists of the complete thermal resistance path from die to heatsink.

To facilitate a system level approach, power modules consisting of parallel devices of either SiC DMOSFETs, provided by ROHM CO. LTD., or SiC VJFETs bare die were packaged in-house at Arkansas Power Electronics International, Inc. The entire system was tested in a laboratory setting and then modeled with SolidWorks™ COSMOS finite element analysis (FEA) software to extract the thermal characteristics of the interfaces.

2.0 Experimental Procedure

The power module consisted of two bare die attached to a nickel-plated, aluminum nitride DBC substrate that had been pattern etched in-house to provide the appropriate circuit traces. The substrate was attached to a five pin power package (2 power pins and 3 signal pins) which was then bolted to an aluminum heatsink. The bare die were wire bonded to the substrate traces and the substrate traces were wire bonded to the package pins. Figure 1 shows a rendering of the completed test module.

Thermal imaging of the module would not be accurate at this point due to the dissimilar emissivities of the various components in the module. To overcome this variance, the entire module was coated in a high-temperature encapsulation. Multiple encapsulations were evaluated that satisfied testing requirements; the most appropriate of which was selected for this module. Selection process is discussed in further detail in Section 3.1.

The module was suspended in air by two small diameter wires running between the outer fins of the heatsink, thus simplifying the model global parameters.

The thermal imager, a Fluke Ti55FT, was tripod mounted directly above the experimental module. The Ti55FT has a range of -20 °C to 350 °C with an accuracy of 2%.

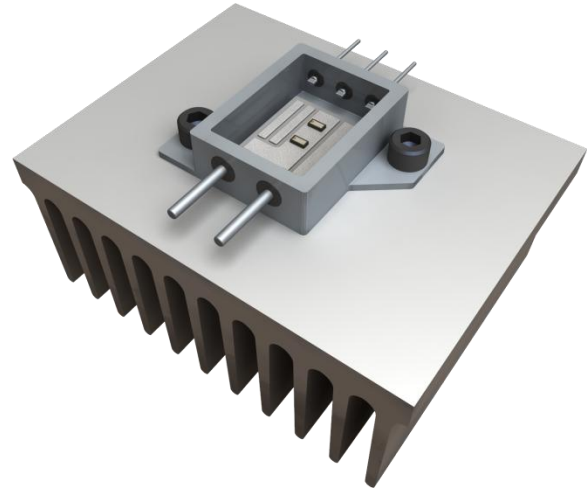


Figure 1. Complete test module with two parallel SiC DMOSFETs.

The module was connected to a high current, low voltage power supply via connectors soldered to the two power pins. Additional wires were soldered onto the power pins to accommodate a Kelvin connection to the package pins. By creating a Kelvin connection, the resistance of the power supply leads are bypassed, which produced a more accurate measurement of the device power dissipation. The devices were operated strictly in forward conduction mode, and all power dissipation in the devices was a result of conduction losses only. By measuring the voltage drop and current through the parallel devices during conduction, the power dissipation of the devices can be accurately calculated.

The power supply was set to a pre-selected voltage, and measurements were taken only after the entire system has reached thermal stability. Measurements taken included voltage drop across both devices and current through both devices; a thermal image is also captured. This process was repeated incrementally until the maximum operating temperature was reached. Once the data was collected, it was used to build an equivalent thermal model in the FEA software.

To model the system in the FEA software, a three-dimensional, 1:1 scale model was designed in SolidWorks™; an exploded view of the model can be seen in Figure 2. The model is then converted to a COSMOS (a SolidWorks™ add-on) model which allowed for steady state and transient thermal analysis. The individual materials that have known thermal properties were then defined. It is important to note that the properties assigned to each material were temperature dependent to provide the most accurate representation possible.

As can be seen in Figure 5, temperature can have a significant impact on the thermal conductivity of the various materials.

Figure 2 shows the various thermal resistances that were used in the COSMOS model. Layer 1 is the die attach, which could be 95Pb/5Sn solder or silver filled glass epoxy. Layers 2 and 4 are the DBC top and bottom side nickel-plated copper, and Layer 3 is the aluminum nitride ceramic dielectric. Layer 5 is the substrate attach, which is either 95Pb/5Sn solder or silver filled glass epoxy. Layer 6 is the package baseplate, which in this case is copper.

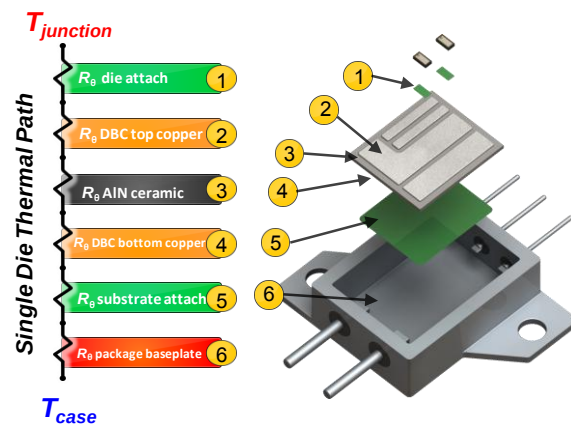


Figure 2. Exploded view of thermal model.

Extraction of thermal interface properties began by probing specific temperature points on the captured thermal image using the SmartView software that accompanies the Ti55FT. An example of said probing can be seen in Figure 3. The thermal, physical, and ambient properties of the COSMOS model were then adjusted until the model matched the laboratory data. The temperature difference (ΔT) across a thermal interface, e.g. die to

substrate, was of significant importance as this was determined mainly by the thermal resistance of the interface. Figure 4 shows the resulting model analysis which correlates to laboratory results shown in Figure 3.

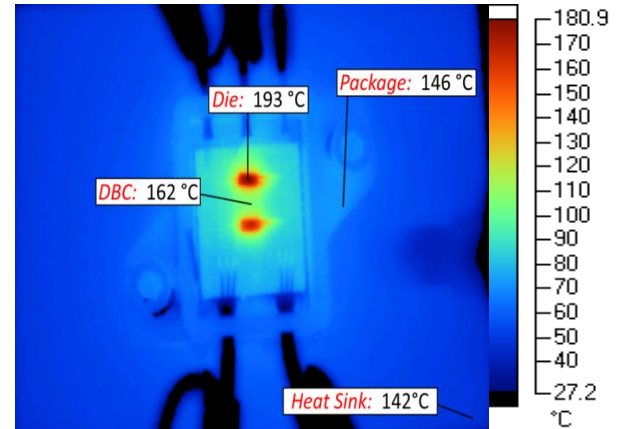


Figure 3. Thermal image with probe points.

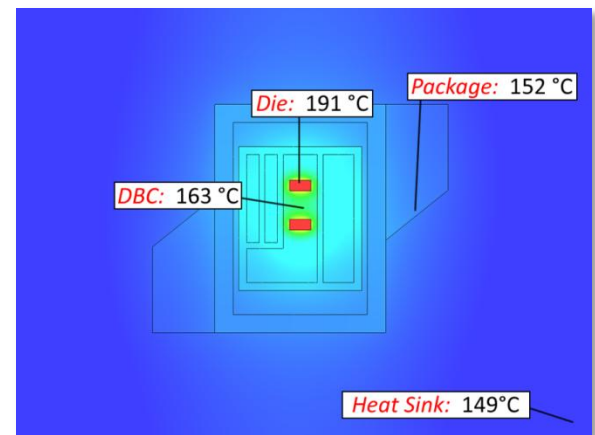


Figure 4. COSMOS thermal model.

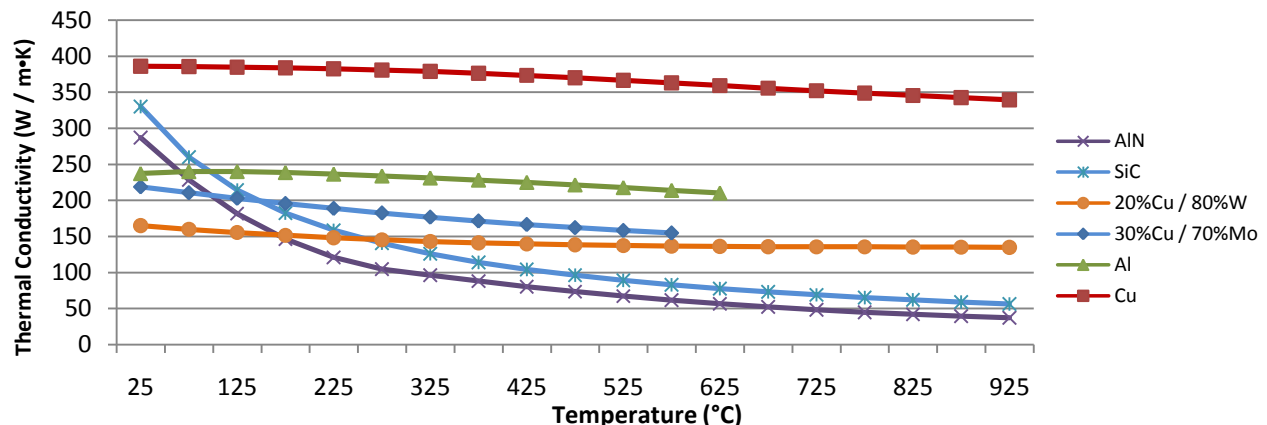


Figure 5. Change in thermal conductivity over temperature for different materials.

3.0 Results and Discussion

3.1 Encapsulation Selection

Before any thermal testing, an appropriate encapsulation was selected. By encapsulating the entire module in a uniform layer of material, the entire module had a uniform emissivity. The requirements for the encapsulation included high-temperature capability, as well as a stable emissivity across a broad range of temperatures.

Testing was accomplished by coating a large piece of aluminum with each encapsulation. Before application of the encapsulation, a thermocouple was attached to the piece of aluminum to provide an accurate temperature reference. The entire piece of aluminum was placed on a hot plate, and the temperature was swept up to 350 °C. At intervals during the sweep, the emissivity of the thermal camera was adjusted until the temperature of the thermal camera matched that as displayed by the thermocouple. Figure 6 shows the plot of four different encapsulations that were evaluated.

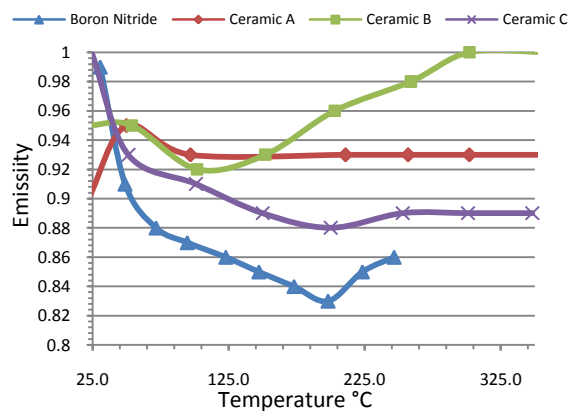


Figure 6. Emissivity of coatings over temperature.

Boron nitride was the first encapsulation to be tested. As can be seen in Figure 6, boron nitride's emissivity varies greatly over the temperature range required. Another drawback of boron nitride is the fact that the boron nitride actually lost adhesion to the metal surface at temperatures over 225 °C. Next, three ceramic encapsulations were tested with promising results. All three ceramic encapsulations survived temperatures up to 350 °C. The emissivity of Ceramic A was very stable, exhibiting no change after 100 °C. Ceramic B was eliminated as a possible solution since the emissivity was unstable over temperature. Ceramic C was also stable over temperature. Ultimately, Ceramic C was chosen over Ceramic A due to the ease of application and curing.

3.2 Evaluation of Solder Attach

The solder selected was a 95Pb/5Sn solder paste with a solidus/liquidus temperature of 308/312 °C. The solder was used as both the die and substrate attach when the test module was built. The solder paste was applied manually with a syringe as an automated dispenser was not available. This type of manual application proved to be an acceptable method, as the solder tended to wick to the component surfaces and self-level itself. The solder was reflowed in open air on a multi-stage reflow system. Ideally, all of the flux would burn off during the reflow process. However, on such a large attach area as the substrate (500 x 450 mil), gasses released by the flux during reflow cannot completely escape the solder attach, causing voids. To validate the quality of the substrate attach, the attach interface was imaged using a Scanning Acoustic Microscope (SAM). The SAM allows for a non-destructive method of inspecting the attach interface.

Figure 7 shows the substrate attach SAM image of the test module used for thermal characterization.

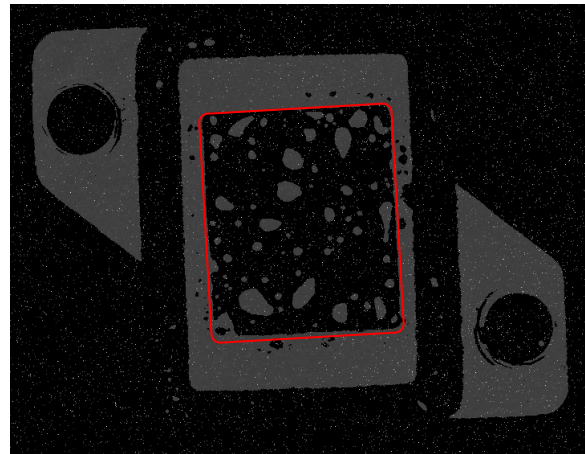


Figure 7. SAM of 95Pb/5Sn solder paste reflow, with approximately 15-20 %voiding.

The outline of the package can be seen by the gray tabs with bolt holes through the centers. The wall of the package is solid black and the solder interface is seen as the innermost black rectangle surrounded by the box outline. The gray areas throughout the solder interface are voids where the solder was not completely contacting both the package and the substrate. Voiding can be very problematic as it causes areas of high thermal resistance. Therefore, an interface that has a high concentration of voiding will have a higher effective

thermal resistance than an interface with a lower concentration of voiding.

To overcome this problem, a process is required that results in a low void interface. One possible solution would be to eliminate the use of flux by using a solder ribbon. However, if the flux is eliminated, the surfaces would be free to oxidize on the open air reflow system due to the high-temperatures required to reflow the solder. So, the entire module must be reflowed in an inert environment to prevent oxidation. Figure 8 shows a 95Pb/5Sn ribbon reflowed in such a way.

The image in Figure 8 is a substrate that was soldered to a test piece of DBC with solder ribbon and no flux. The reflow was performed in a vacuum reflow oven in which the entire chamber was evacuated and then filled with a 95% Nitrogen, 5% Hydrogen forming gas to prevent oxidation. Due to the uniformity of the solder interface, the boundary of the DBC substrate was almost indistinguishable. The outline signifies the actual boundary of the solder attach to the DBC. As seen in the figure, the interface was virtually void free. Future research will include comparing the thermal properties between the attach methods demonstrated in Figures 7 and 8. However, the scope of this paper only includes the characterization of the thermal properties of the attach method demonstrated in Figure 7.

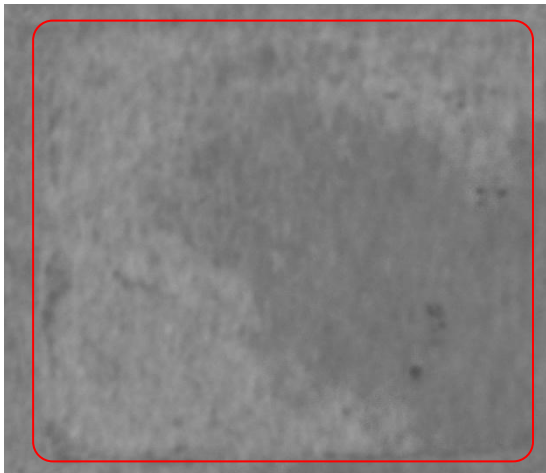


Figure 8. SAM of 95Pb/5Sn solder ribbon fluxless reflow, with near 0% voiding

3.3 Evaluation of Epoxy Attach

The epoxy utilized for testing is a proprietary silver loaded glass epoxy. As with solder paste, the epoxy was applied manually with a syringe. Unlike the paste, though, the epoxy did not wick to the components or itself; as a result, factors such as thickness and epoxy spread were difficult to

control. This resulted in testing two modules with varying thicknesses of epoxy on both the die attach and the substrate attach.

The recommended epoxy bondline is 2 – 6 mils for die sizes up to 700 x 700 mils. The bondline of each attach was measured using a Keyence digital measuring microscope. Module 1 had a die attach bondline of 4.5 mil and a substrate attach bondline of 1 mil. Module 2 had a die attach bondline of 1 mil and substrate attach bondline of 14 mil. The variance of epoxy bondline was attributed to the lack of accuracy encountered when dispensing epoxy manually. Since the thickness of the attach was known, it could be reflected into the COSMOS model to increase simulation accuracy.

SAM images were taken of the substrate interface of both modules as seen in Figure 9 and 10. Figure 9 shows the epoxy attach of Module 1, and Figure 10 shows the epoxy attach of Module 2. A SAM image of an epoxy attach is very different from that of a solder attach. With an epoxy attach, the quality of the attach can be indicated by a uniform distribution of epoxy. Epoxy will exhibit variances in shading that indicate changes in density, as opposed to the well defined voids seen in a solder attach. For Module 1, the less dense areas are the very light areas of the innermost rectangle, which in this case occupy the majority of this attach. Module 2, on the other hand, has a very uniform distribution of epoxy as can be seen by the more uniform color gradient.

One would expect the substrate attach of Module 1 to have a much higher effective thermal resistance than that of Module 2 due to the non-uniformity of the substrate attach of Module 1. Effective resistance is the thermal resistance of the attach as a whole including contributions from voiding, not simply the bulk thermal resistance of the epoxy as defined by the manufacturer's datasheet. The expected difference in attaches can be verified by looking at the temperature difference across the substrate attach, i.e. from substrate to package as plotted in Figure 11.

In Figure 11, the temperature differences across the substrate of each module are plotted for varying power dissipations of the die. As expected, the less uniform substrate attach of Module 1 has much larger temperature differences for a given power dissipation than that of Module 2, indicating a higher effective thermal resistance. Also plotted in Figure 11 is the temperature difference across the die attach, i.e. from die to substrate. The effective thermal resistances of both die attaches are very similar. However, SAM images of the die attaches were not possible at the time due to the depth of the package and limitations of the SAM.

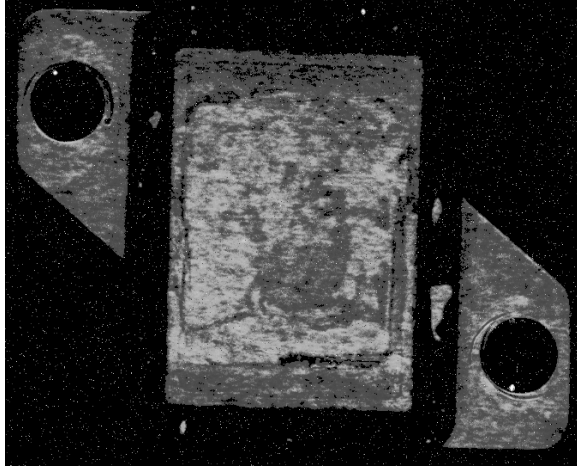


Figure 9. Module 1 with a non-uniform epoxy attach.

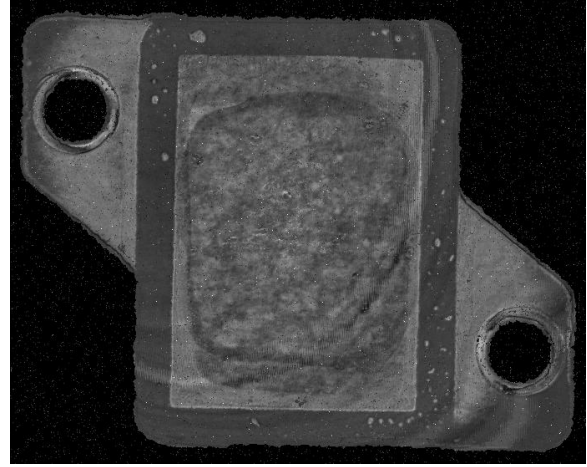


Figure 10. Module 2 with a uniform epoxy attach.

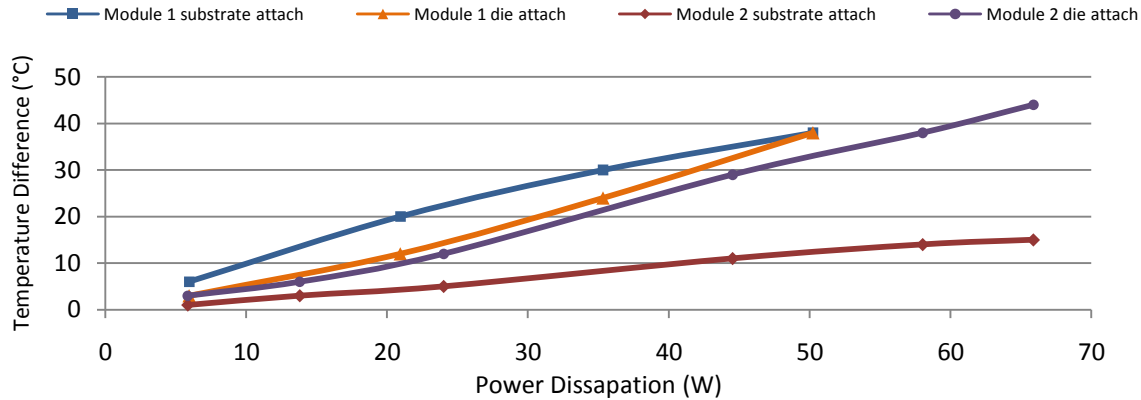


Figure 11. Temperature difference across different APEI, Inc. proprietary epoxy attaches.

3.3 Thermal Conductivity Modeling of Attaches

One source of error when working with an attachment method can be the temperature dependence of the thermal conductivity. Temperature dependent thermal conductivity is available for elemental metal but is rarely available for solders. Using the experimental results verified through COSMOS, the researchers were able to define the temperature dependent thermal conductivity of both the solder and epoxy.

Another possible source of modeling error can be the interfacial thermal resistance between materials, e.g. between epoxy and DBC. Interfacial thermal resistance has been previously shown as a major contributor to an attachment material's effective thermal resistance [6]. FEA software simply cannot determine interfacial resistance; it can, however, be used to determine an effective thermal

resistance that is more useful to a designer on a system level.

Using the COSMOS software, the system was modeled in 1:1 scale with special care taken to model the attachment thickness as measured in the laboratory. Using the procedure described in Section 2.0, the effective thermal conductivity of 95Pb/5Sn and the silver loaded glass epoxy was determined. The plots of both of these can be seen in Figure 12.

In Figure 12, the data points extracted from the thermal model are plotted and the points are fitted with a trendline. As expected, the effective thermal conductivity of the solder decreases as operating temperature is increased. Surprisingly, the thermal conductivity of the epoxy is very stable over such a broad range of temperatures.

The extrapolated effective thermal conductivity of 35 W/m•K at room temperature for 95Pb/5Sn correlate perfectly with the published bulk thermal conductivity of 35 W/m•K. The extrapolated

trendline of the silver loaded glass epoxy shows an effective thermal conductivity value of 11 W/m•K at room temperature, which is much lower than the published bulk thermal conductivity of 65 W/m•K.

One inference that could be made here is that the solder has an almost zero interfacial thermal resistance, which would correlate to a bulk thermal resistance being very similar to the effective thermal resistance. The epoxy, however, has a very large interfacial thermal resistance, which correlates to the effective thermal resistance being much lower than the bulk thermal resistance. However, more testing would need to be conducted to reach a conclusive result.

3.4 Evaluation of Thermal Grease

Ideally, the package and heatsink surfaces would contact each other perfectly, thereby creating the optimum thermal path. This is not possible in a practical application, so thermal grease is used. Thermal grease increases the thermal conductivity of the interface by filling in the tiny surface mismatches that occur between the package and heatsink. These mismatches can be caused by surface roughness, an uneven package, etc. The idea is to eliminate as much open space between package and heatsink as possible.

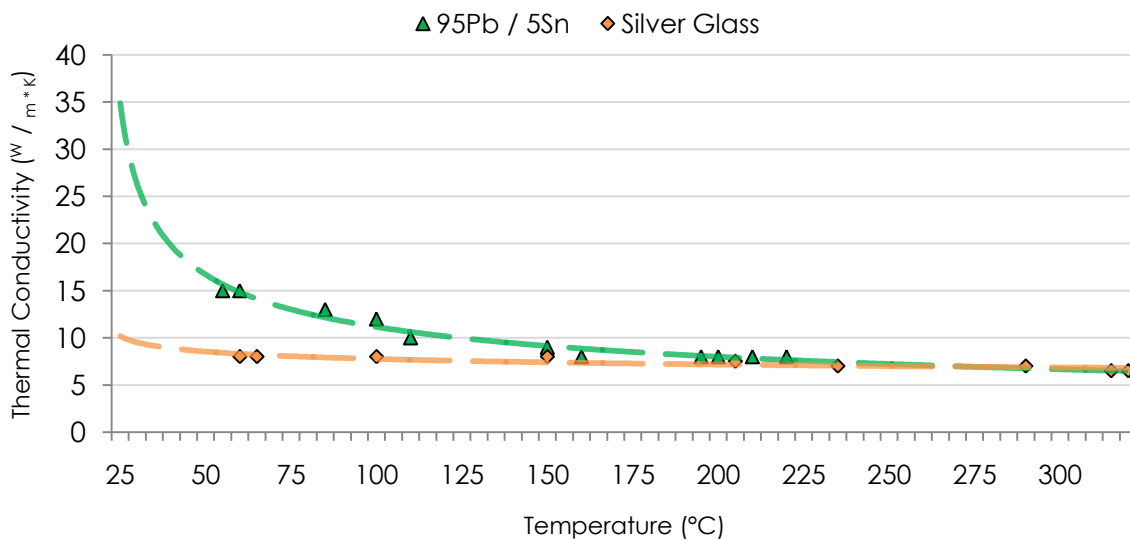


Figure 12. Thermal conductivity over temperature extracted from thermal modeling.

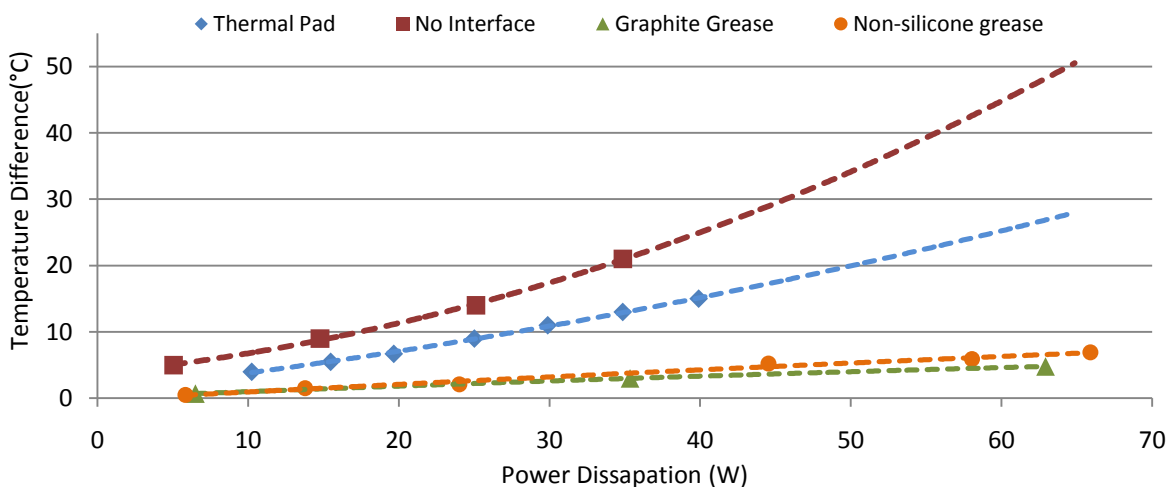


Figure 13. Temperature difference from package to heatsink for varying thermal interfaces.

Classically, silicone grease is used as the thermal interface between package and heatsink. At high-temperature, though, this is not a viable solution, mainly due to evaporation of the grease at elevated temperatures. To overcome this challenge, several non-silicone, high-temperature thermal greases were evaluated, along with a low-temperature thermal pad and no thermal interface material between package and heatsink. Even though the thermal pad and the practice of not using any thermal interface are not recommended at high-temperature, they are still valuable as a baseline reference.

The thermal grease is not a solid layer of material but an uneven distribution of thickness across the entire interface acting as a filler material for mismatches between package and heatsink. The lack of uniform thickness makes FEA analysis impractical for this situation. To provide a beneficial comparison between interfaces, it is necessary to evaluate the temperature differences across the package and heatsink interface. Figure 13 shows the temperature difference between the package and heatsink of varying power dissipation levels for multiple thermal interfaces.

As Figure 13 shows, the worst case scenario is having no thermal interface at all. The low-temperature thermal pad is better than having no interface, but is significantly inferior to the high-temperature thermal greases. Both high-temperature non-silicone thermal grease, and high-temperature graphite thermal grease are fairly comparable, with the graphite grease having a slight advantage at higher power levels.

4.0 Conclusions and Future Work

When designing a system for high temperature operation, special care must be taken to select materials that have satisfactory performance at higher operating temperatures. This paper only introduces a few of the choices for high-temperature die attach, substrate attach, and thermal grease. As shown by the supporting data, material properties at high-temperature can vary greatly from properties at room-temperature. However, given the proper material considerations, a module with a low effective thermal resistance can be designed.

Future work will include a continuation of testing various high-temperature thermal interfaces. Also, testing of the low-void, vacuum attach method for the 95Pb/5Sn solder will be compared to results using an open air reflow system that are presented in this paper.

The epoxy will also be re-evaluated with different curing schedules that could possibly decrease effective thermal resistance, including a solvent drive off at lower temperature before curing completely in a vacuum oven.

6.0 References

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