

Prototyping a SiC JFET Drop-in Replacement Module for a 600-V, 600-A Si IGBT Half-Bridge Module

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Abstract

Silicon carbide power vertical-channel junction field effect transistors (VJFETs) are ideal candidates for next generation vehicle power systems. They combine the switching speed of MOSFETs with the voltage and current handling properties of IGBTs and the excellent thermal properties derived from the SiC material. As a unipolar device they can be easily paralleled over the entire operating range of the device and generate extremely high current for high power application. With the drop-in replacement, the case temperature of the motor drive can be significantly increased above the current limit of 80 °C, which will permit the designer new opportunities for decreasing size, weight, and cost.

With current die area yields, the only way to fabricate high-current IPMs that can address 600-A IGBT replacement is to parallel SiC die. A process for packaging a 600-V, 600-A IGBT replacement module based on very low specific on-resistance SiC VJFETs (2.5 mΩcm²) co-packed with SiC Schottky Barrier Diodes (SBD) is reported. The design covering thermal design, material selection, and thermal (soldering) budget for the DBC and copper base plate commercial packaging is presented. The DBC design will be presented, which took into consideration accommodating 80 VJFETs in parallel and 40 SBDs in anti-parallel. All DBC were screened for single die failures using a multi-step process including high-temperature reverse bias screening. Finite element thermal analysis was utilized for appropriate packaging material selection. Successful completion of the packaging process was confirmed by DC and switching characterization.

Key Words: SiC, VJFETs, power system, drop-in replacement, half-bridge module

1.0 Introduction

Silicon (Si) IGBT has been utilized as power switch since the early 1990's. The continuing development in Si IGBT technology has further enhanced the IGBT performance by increasing the device switching speed and reducing the power loss [1-2]. However, the IGBT is a bipolar device with a relatively slow switching speed and high switching loss. Significant improvements in performance can be achieved with the use of wide band gap silicon carbide (SiC) VJFET and Schottky diodes due to its low on-resistance, fast switching characteristics and capabilities of handling high operation temperature and power. A recent EMPF study using P-Spice modeling on the performance of a Si IGBT module and a SiC VJFET revealed a great improvement in most cases when SiC devices replace Si devices [3]. One of example given was to use SiC VJFET instead of a Si IGBT in a test circuit similar to power conversion module sub-system; the power dissipation

has been improved by a factor of 25. Inoue [4] also proved that the switching loss could be dramatically reduced by the use of a unipolar SiC switch to replace Si IGBTs. The commercialization of SiC switches is the expected next logical step [5].

This paper will discuss the fabrication process of SiC VJFET half-bridge module for a drop-in replacement of Si IGBT module. The DC and switching characterization will also be presented for the confirmation of a successful completion of the packaging process.

2.0 Substrate Design

The cross section illustration of original Si IGBT half bridge module for replacement is shown in Figure 1. In addition to the new gate driver design for VJFET, the DBC (direct bond copper) substrate needs to be redesigned to accommodate the 80 SiC VJFETs and 40 SBDs.

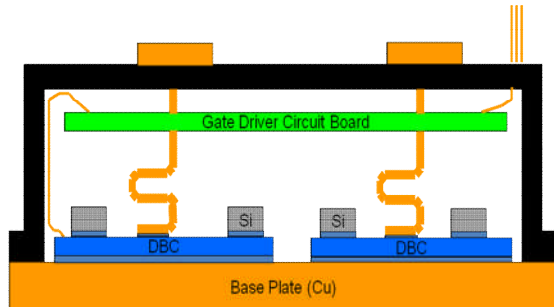


Figure 1: Cross section view of the 600-V, 600-A Si IGBT half bridge module

The Direct bond copper (DBC) substrate in which a thick copper layer is cladded on a ceramic substrate has been extensively used in power electronics applications due to its good thermal conductivity, low coefficient of thermal expansion (CTE), high mechanical strength and high current carrying capability. The commonly used substrate materials are beryllium oxide (BeO), silicon nitride (Si_3N_4), aluminum nitride (AlN) and aluminum oxide (Al_2O_3). The thermal and mechanical properties of these materials are listed in Table 1. Even though BeO has the highest thermal conductivity, it is not considered as the choice of material for this application due to its high cost and toxicity. AlN has the highest thermal conductivity and better match of CTE to SiC among the remaining materials. However, with thick Cu metallization, the AlN is prone to fracture during thermal cycling due to its low fracture toughness and flexural strength. In consideration of low cost, availability, electrical properties and thermal conductivity, 96% Al_2O_3 is the selected material for the DBC substrate fabrication.

Table 1. Properties of Substrate Materials

Materials	Al_2O_3 [6]	Si_3N_4 [6]	AlN[6]	BeO[7]
Properties				
TC ($\text{W/m}^2\text{C}$)	20	30-90	170-230	280-290
CTE ($\text{ppm}/^\circ\text{C}$)	6.7-7.1	2.7	4.5	7.0-9.0
Young's modulus (GPa)	380	310	330	345
Fracture toughness ($\text{MPa}\cdot\text{m}^{1/2}$)	3.3-3.7	5-6.5	2.7	3.68
Flexural strength (MPa)	274	850	400	232

To complete the module for drop-in replacement, four DBCs are required. The dimension of each Al_2O_3 substrate is 45mm x 40mm x .635mm. To carry large currents and provide better heat dissipation, the thickness of 0.25 mm (10 mil) direct bond Cu was on both sides of Al_2O_3 . The backside Cu is full face with 0.5mm pull back on four edges. The electroless plated Ni at the thickness of 5.08 μm

(200 $\mu\text{-in}$) is utilized as diffusion barrier, followed by an electroless plating of 7.62 μm (300 $\mu\text{-in}$) Au to protect Ni from oxidation. To accommodate 80 VJFETs of 1.33mm x 1.33mm x 0.25mm and 40 SBDs of 1.705mm x 1.38mm x 0.35mm, the topside Cu is etched to the pattern shown in Figure 2. The design A and design B in parallel is required to complete the half switch. The conductor spacing is 0.5mm. To sub-group the entire paralleled devices for trouble shooting, individual Cu pads of 4.22mm x 1mm or 4.22mm x 2mm were designed to accommodate the source or gate bonding wires of four VJFETs and two SBDs. These individual Cu pads can be wire-bonded eventually to form the source and gate connections.

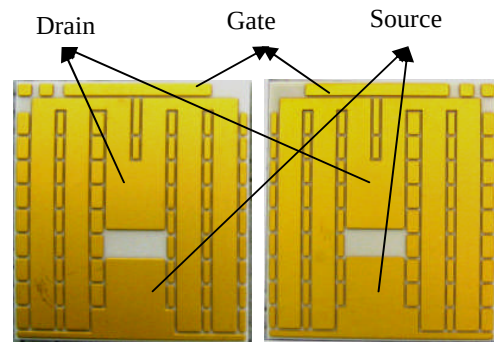


Figure 2: DBC designs (left-design A, right-design B)

3.0 Packaging Material Selections

Power module packaging involves several steps and materials associated with each step. The packaging procedures to be taken in this study are listed in order: SiC devices attaching to DBC top Cu, wire bonding to make connection from device terminal to its corresponding Cu pad, DBC bottom Cu attaching to Cu base plate, gate driver connecting to gate terminal on DBC, external drain and source connecting to their corresponding terminals on DBC and encapsulation. The interconnection materials along the path from device to base plate have to provide good thermal dissipation path in order to sufficiently dissipate the heat generated when device is on. Solder interconnection materials are the choice of materials for this application due to their high thermal conductivity and electrical conductivity as applicable. In the process of selecting solder, melting temperature and environmental friendliness are major concerns. The solder melting temperature of next step should be at least 20 $^\circ\text{C}$ lower than that of previous step. Lead free solder is chosen over lead containing solder if it is possible. The detailed assembly sequence and its corresponding materials are shown in Figure 3. The packaging materials and some of the interested properties are summarized in Table 2.

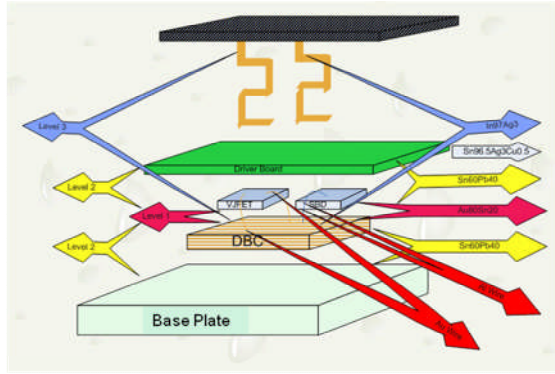


Figure 3: Interconnection sequence and materials

3.1 Verification of Material Selection

3D finite element analysis was employed to investigate the steady state temperature distribution on the surface of DBC. Figure 4 shows the geometry segment selected for simulation. It is a segment on one side of drain-source external contact, includes two top Cu conductors with two VJFETs attached to each. The spacing between two Cu conductors is 2 mm, which is the actual spacing from design. The positions of JFETs are approximately the same as the actual assembly.

Per design specification, the on-resistance of JFET is about 0.17 ohms at 25 °C. The on-resistance is about 0.46 ohms at 175 °C with the consideration of 1% increase in thermal resistance at every 1 °C increase in temperature. The power dissipation of each JFET is about 6.47W at 600-A rated current and 175 °C targeted junction temperature. The thermal conductivities of associated materials are listed in Table 2. Only the thermal conductivity of SiC varies enough to use the temperature-dependent values in the simulation. The temperature-dependent thermal conductivities were calculated based on the formula stated by Adachi [8]. All boundaries are insulating

except the bottom of the base plate which is held at a constant temperature of 125 °C.

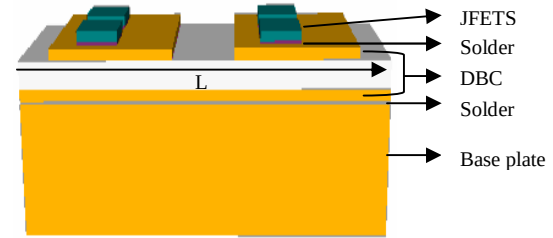


Figure 4: Geometry segment for simulation

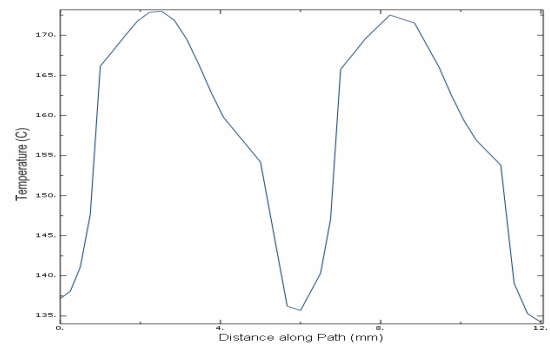


Figure 5: Temperature distribution on the top Surface of DBC along path L

The temperature distribution on the top of DBC along the path L is shown in Figure 5. The maximum temperature is under the SiC devices, which is expected. The temperature at the point close to the external drain-source contact is about 133 °C. The actual temperature on the external drain-source contact is expected to be lower since it is farther away from devices. It verifies that the choice of 97In3Ag solder is practical in terms of its lowest melting temperature.

Table 2. Materials Selected for the Prototype Module

Component	Material	Dimension	Thermal Conductivity* (W/mK)	Melting Temp. (°C)
Bond Wires	Au	1 & 5 mil	301	1064
	Al	5 mil (dia.)	210	600
Base Plate	Cu	127x87 (mm ²)	393	1083
Solder (DBC to heat sink)	Sn63Pb37	wire (0.78mm dia.)	49	183
Substrate	DBC	45x40 (mm ²)	393 (Cu)	1083
			20 (Al ₂ O ₃)	2053
Solder (Die attach)	Au80Sn20	Preform (1mm ²)	57	280
SiC Devices	JFET(Au metallization)	1.3x1.3 (mm ²)	(4H-SiC) 370 @ 25°C	N/A
	SBD (Al metallization)		290 @ 75°C	
			240 @ 125°C	
			200 @ 175°C	
Solder (external contact)	In97Ag3	Wire (D-0.78mm)	73 @ 85°C	143
Solder (Driver Board)	Sn96.5Ag3Cu0.5	Wire (D-0.78mm)		217
Dielectric Gel	Q3-6575			

4.0 Screening for Device Infant Mortality Failure

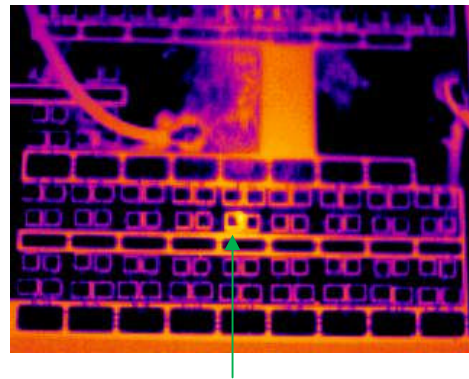
Even though the selected devices have passed the initial on wafer screening, it can possibly fail the DC testing after DBC level packaging. The failure may result from device itself and/or damaging initiated during the following processes such as wafer dicing, die attachment and wire bonding. Especially critical with the larger number of devices has been through this process. In order to reduce infant mortality failure, DBC level screening at room temperature reverse bias (RTRB) was performed followed by the screening at high temperature reverse bias (HTRB) condition.

RTRB: The room temperature screening was performed under Cascade semi-automatic probe station. The DBC was submerged in dielectric material named Fluonert. The 600V rated drain-source voltage was applied to drain-source through probes with gate-source reversed biased voltage of -25V. The off-state gate-source current I_{gs} and drain-source current I_{ds} were recorded every 10 sec for the first minute under constant bias voltage. To simulate the device on and off status, two voltage pulses with $t_{on}=30\text{sec}$ and $t_{off}=2\text{sec}$ were applied to the drain-source should no failure occur during the first minute stressing. Then additional 5 minutes' constant drain-source voltage stressing followed, the I_{gs} and I_{ds} were recorded every 20sec. Device failure occurred if either I_{gs} or I_{ds} was over the preset compliance which is 100mA for I_{gs} and 10mA for I_{ds} .

To identify the device(s) with high leakage current, thermal imaging camera "ThermoVision A20" from Flir Systems with a temperature sensitivity of 0.1°C was utilized. In this process, a reverse voltage was applied either at gate-drain (100V or less) or at gate-source (-25V or less) through lab power supply instrument (s). The device temperature was monitored by the thermal imaging camera and the thermal image was displayed on computer monitor. By turning on and off the power supply, the device with more than 10mA leakage current can be easily identified since it was heated up immediately as turning on. A thermal image of a DBC with gate-drain reverse bias of 50V was shown in Figure 6. The total gate-drain leakage current was 96mA in this case. After this device was removed from the system by disconnecting the bonding wires, the total gate-drain leakage current was below 10mA which is acceptable.

HTRB: HTRB testing was performed to further screening the devices at elevated temperature. Due to oven temperature limitation, the DBC with paralleled devices was exposed to a constant oven temperature of 200°C in an air environment. In contrast of applying 600V rated blocking voltage at drain-source, a maximum voltage of 200V was applied at

drain-source with gate-source voltage of -25V due to the lack of dielectric material over the devices. The maximum and minimum I_{gs} and I_{ds} were selected based on the result of DC characterization and the actual I_{gs} and I_{ds} were in-situ recorded every 10sec. The test was interrupted should any actual leakage current be over the limit. And the procedures mentioned above were immediately performed to identify the failed device(s). The selected testing criterion was 24 hours without failure.



device with high leakage current

Figure 6: Thermal image of a DBC under gate-drain voltage of -50V

5.0 Module Assembly and Packaging

We have illustrated the assembly sequence and interconnection materials associated with each step in section 3.0. The solder interconnections were accomplished through a process similar to transient liquid phase bonding. But instead of heating the sandwiched structure (top component-solder layer-bottom component) at the same time, we placed either solder preform or solder wire on the heated bottom component (the heating temperature adjusted to about 10 degree higher than the melting point of corresponding solder). The top component was then place into the melting solder. A manual or programmed scrubbing stroke was conducted as appropriate to remove the air trapped. The assembly was then brought to room temperature for cooling down and solder solidification. The final step of packaging is the dielectric gel application. The calculated volume (about 90 ml) of Q3-6575 dielectric gel was applied through a predesigned opening on top of the case and cured at room temperature for 24 hours. The photo of completed module is shown in Figure 7.

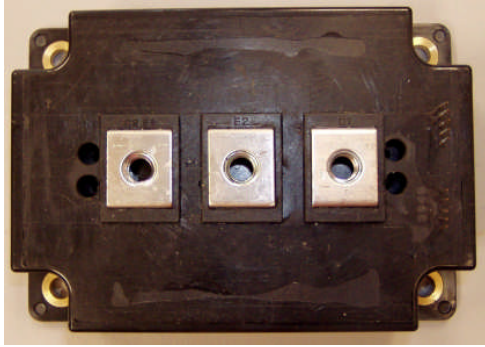


Figure 7: Prototype of SiC half-bridge module

6.0 Module Testing

Static DC Characterization: Figure 8 shows the measured on-state DC characteristics on a half-bridge module. A forward current of 473-A was achieved at $V_{ds} = 1.4$ V and $V_{gs} = 2.5$ V, however it has not reached saturation yet. A much higher current is expected to be delivered with a higher V_{ds} . Figure 9 illustrates the drain-source current I_{ds} as a function of V_{ds} at blocking state with $V_{gs} = -25$ V of all four DBCs in this module. It shows that all the DBCs can block 600 V with I_{DS} current less than 2 mA.

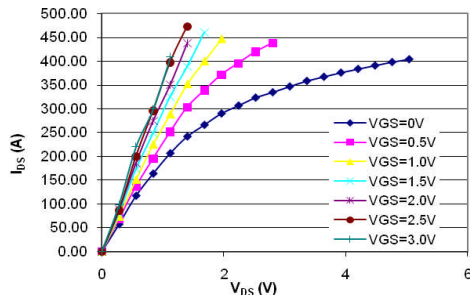


Figure 8: Drain-source forward DC characteristics of half switch, containing 130 SiC VJFETs in parallel.

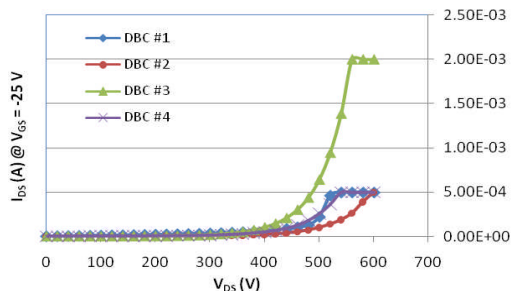


Figure 9: Drain-source DC blocking characteristics of the four DBCs in the prototype module (each half switch contains two DBCs in parallel).

Dynamic Switching Testing:

Switching performance of the completed half-bridge module was evaluated using a clamped inductive load test circuit. This circuit was employed primarily to qualify the switching performance of the module for the intended inverter application. Inductive current switching measurements were recorded for both the low side and high side switch exceeding 220 A at a drain source voltages above 400 V. Switching energies for turn on and turn off of both the high and low side switch were roughly 25 mJ and 30 mJ respectively. A screen capture for a turn off switching transient is shown in figure 10.

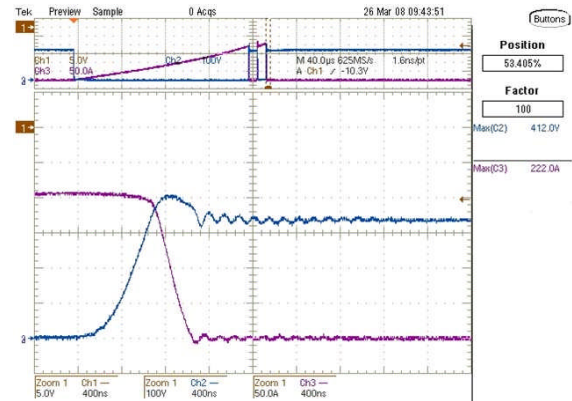


Figure 10: Turn off clamped switching transient waveform recorded during clamped inductive load switching evaluations. The blue trace is drain-source voltage (100 V/div). The purple trace is drain current (50 A/div). The time axis is 400 ns/div.

7.0 Summary and Conclusions

In this work, we have presented the fabrication processes of a prototype SiC half-bridge power module. The DC characteristics shows that the module can meet the requirement of 600-V and 600-A. The initial dynamic switching performance results have shown that the module reported in this paper can safely switch load currents in excess of 200 A continuously in applications up to 20 kHz. This module has been demonstrated to work as a drop in replacement for an intelligent power module IGBT in a motor drive application. Second generation devices presently in development should be able to increase the voltage margin by 100 % with a much less negative gate-source voltage (1200-V blocking with $V_{GS} \approx -5$ V) while maintaining or increasing the current handling capability at a junction temperature greater than typical for the silicon IGBT.

8.0 References

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