

Thermal Stress Analysis in a Multilayer Power Module

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Abstract

The focus of this work is to analyze the thermo-mechanical stresses in Multi-Chip Power Module (MCPM) systems being developed for high-temperature power electronics applications. Silicon Carbide (SiC) based electronics show considerable promise for demanding applications (hybrid electric commercial and combat vehicles, interplanetary exploration, power distribution, etc.) in part due to its capability to withstand temperatures upwards of 600°C. While high-temperature SiC based systems are an enabling technology for a wide range of applications, the harsh conditions introduce exceedingly high thermally-induced stresses in the system due to the coefficient of thermal expansion (CTE) mismatches between the different materials in the structure. High thermal stresses in the die or solder interface may result in peeling or fracturing, and thus are a major reliability concern for these systems. This paper investigates the case of a single SiC device bonded to a thick metal power substrate using a variety of solder alloys. Analytical models and Finite Element analysis (FEA) software is employed to evaluate the shear stress, peeling stress, and normal stress examined over temperatures ranging from 25 to 700°C. Multiple solder thicknesses and die geometries are analyzed in order to determine an optimal bond line. The FEA results are compared to several well adopted analytical approaches for comparison. In addition, methods to reduce the overall stresses are presented.

Key Words: high temperature power electronics, high temperature packaging, thermal stress

1.0 Introduction

Silicon-based devices have been the most widely used for power systems and power electronics applications. The demand for higher power, higher system voltages and higher operating temperatures for military, aerospace, hybrid, and fully electric vehicles has intensified research in wide bandgap switches such as SiC and Gallium Nitride (GaN) based electronics [1]. It has been shown that the SiC power devices, when implemented properly, are capable of achieving greater power densities with lower switching losses in comparison to a similar Si-based system [2-5]. In addition to high power densities, the exceptional thermal stability of SiC allows operation in very harsh ambient conditions upwards of 600 °C [6]. The potential for higher operating temperatures allows for the reduction of heat removal systems (heat sinks, cold plates, etc.), providing an effective solution to reduce overall system size and weight. A major concern for the success of high-temperature SiC based power modules is linked to the long-term reliability of the various dissimilar material bond interfaces. Due to the mismatch in the coefficient of thermal expansion of the materials, high thermal stresses are induced at

the interfaces that can lead to mechanical failures of the bonds and materials, ultimately instigating a failure of an individual device or the entire system [7].

A typical SiC power module consists of five layers of different materials as shown in Figure 1. These five layers consist of a SiC die bonded to a direct bond copper (DBC) substrate using a solder. The DBC is also attached to a base plate and heat sink (not shown in Figure 1), however they have negligible effect on the stresses induced in the die-solder and solder-substrate interfaces.

Typically for high temperature applications, hard solders such as Au-Sn alloys are used as they are mechanically stronger and are less prone to thermal fatigue compared to the soft solders such as the Pb-Sn alloys [8]. The majority of the failures are expected either in die-solder or solder-DBC interfaces where the thermal stresses are greatest. In this work, analytical and finite element modeling is utilized to acquire an understanding of the effect of various design parameters such as solder thickness, distance of die from the trace and Cu thickness on

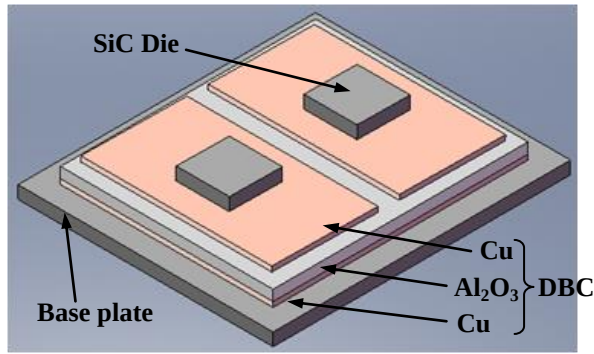


Figure 3: Schematic of a SiC power module.

the maximum thermal stress. These modeling results will provide “trends” and guidance to engineers to design assemblies with improved mechanical reliability.

2.0 Analytical Method

While FEA can provide accurate results, any “human-error” in setting up the model can easily go undetected leading to errors in the output. To avoid this problem, an analytical verification is desirable to ensure the accuracy of the model. Once simulation results are verified with known experimental or analytical values, the same model may be simulated under a wide range of conditions with a high degree of accuracy. The initial analytical model for analyzing thermal stresses in a bi-metal thermostat was developed by Timoshenko [9] using beam theory and linear elasticity. However this model was limited to only few cases and did not account for presence of a solder layer. In this paper more accurate versions of the bi-metal model that were developed by Suhir [10] and Schmidt [11] are utilized. Also, unlike the model developed by Timoshenko, the models by Suhir and Schmidt account for bending effects, thus making them more accurate. Other methods by Suhir and Schmidt take into consideration the fact that when the thickness and stiffness of the solder is comparatively small, the stress variation along the thickness of the solder is negligible. In effect a tri-material assembly can be treated as a bi-material assembly. A comparison of the thermal stresses calculated from the different analytical methods is discussed in Section 4.

The assembly under investigation for analytical calculations consists of a large SiC die (200 x 200 x 20 mils) soldered to a Cu substrate (200 x 200 x 12 mils) using Au-Sn (80-20) alloy. The default thickness of solder for all calculations is selected as 3 mils. The FEA simulations conducted for the full

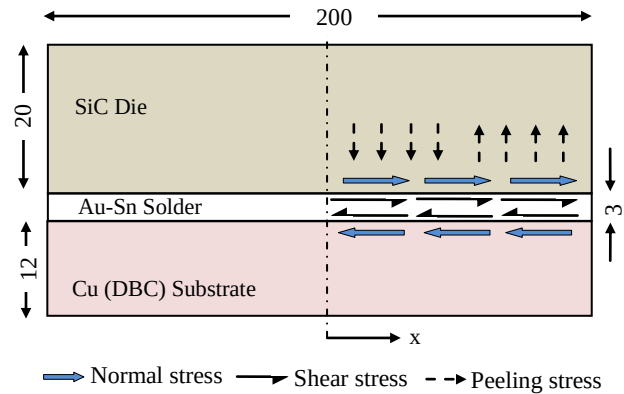


Figure 1: Schematic of thermal stresses in a bonded assembly. All dimensions are in mils.

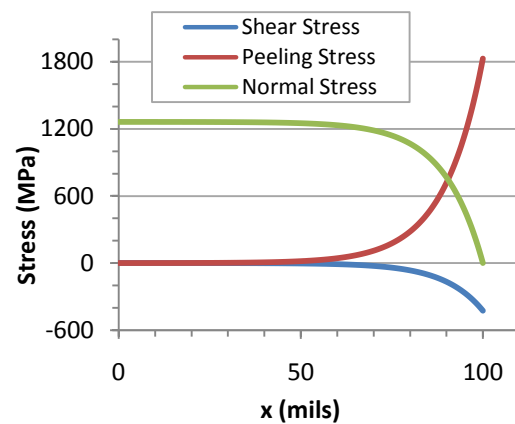


Figure 2: Variation of stresses along the length of the die for $T = 527^{\circ}\text{C}$ ($\Delta T = 500^{\circ}\text{C}$).

power module showed that the ceramic and lower copper layers of the DBC and the base plate have minimal effects on stresses at the die-solder and solder-substrate interfaces. Therefore, to simplify the analysis, these layers have been omitted from the analytical models used to determine thermal stresses. The temperature dependent material properties for Cu and SiC are taken from the Material Property Database (MPDB) v 6.77 [12]. As per the author’s knowledge, high temperature material properties for Au-Sn alloy are not available and hence the properties at room temperature (27°C) are used for all temperatures. The elastic modulus and the Poisson ratio of Au-Sn solder used for all calculations is 59.03 GPa and is 0.30 respectively.

Assuming that complete stress relaxation occurs while cooling after the bonding process, the assembly is considered stress-free at room temperature. However, as the assembly is heated, shear stresses (τ_s) are introduced at the die-solder and solder-

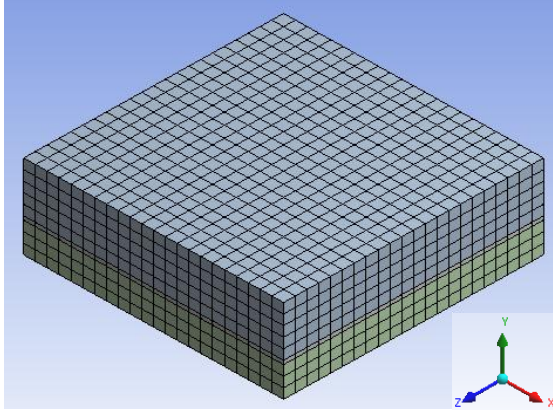


Figure 4: FEA model of die-solder-substrate showing the mesh.

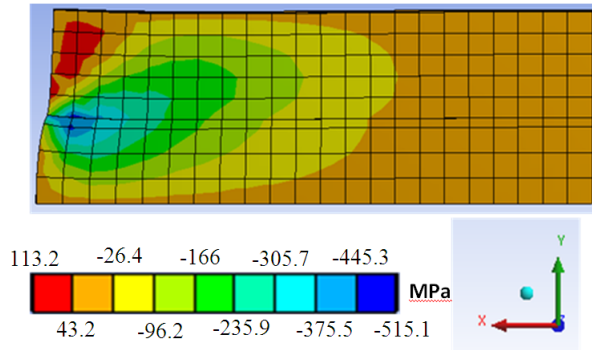


Figure 5: Shear stress (τ_s) distribution using FEA for $\Delta T = 500$ °C.

substrate interfaces. Also, the die experiences tensile normal stresses (σ_N) and the substrate experiences compressive normal stresses. Since the Cu substrate expands more than the SiC die, it causes bending stresses in the die and the substrate and transverse normal stresses also called peeling stresses (σ_P) between the die and the solder, see Figure 2 [11]. The peeling stress is very important for studying strength of the interface bond as high peeling stress can cause delamination failures [13]. It is important to note that the peeling stress is related to the shear stress (τ) as per the relation [11]:

$$P(x) = -a \frac{d\tau}{dx} \quad (1) .$$

In the above relation, a is a constant determined by the geometry and material properties of the assembly and x is the distance from center of the die as indicated in Figure 2. Hence, for a given assembly,

the magnitude of the peeling stress is directly proportional to the shear stress.

The primary thermal stresses along the length of the die calculated using the bi-material method developed by Schmidt [11] for the assembly heated to a temperature of 527 °C is shown in Figure 3. Since the stress free temperature is assumed to be 27 °C, the net temperature difference (ΔT) is 500 °C. As seen from Figure 3, the normal stresses are maximum at the center of the die and zero at the edge, whereas the shear and peeling stresses are zero at the center and maximum at the edge of the die. The shear and peeling stresses are maximum at the edges and negligible at the center of the die whereas the normal stress is almost constant over the length of the die and negligible at the ends.

3.0 Simulation Methodology

The FEA simulations of a three dimensional model of the power module are conducted using a commercial finite element package, ANSYS Work Bench ver. 11. The model is meshed using an 8-node brick element, and by using rules of symmetry only one-fourth of the model is analyzed to reduce computation time and increase mesh density. Since our interest lies in evaluating the stresses at the material interfaces, the mesh is refined at the contact surfaces using the 'contact-sizing' tool for larger models. The number of elements used in the entire models is approximately 5,200 (30,000 nodes) and any increase in the number of elements changed the maximum stress output values by less than 2%. The material properties for SiC, Cu and Al_2O_3 for the temperature range from 27-700 °C are taken from the MPDB ver. 6.77 database [12]. Room temperature material properties for Au-Sn (80-20%) alloy are used for all simulations. It is expected that at higher temperatures the elastic modulus of the solder will decrease, however the results in this paper do not include this effect. Our future work will focus on obtaining high temperature material property data for Au-Sn alloy and incorporating it in the analysis.

4.0 Verification of FEA model and analysis for solder selection.

4.1 Comparison analytical and FEA method

To check the accuracy of the FEA model, the shear stress obtained from the numerical analysis of the package shown in Figure 1 are compared with the analytical solutions of tri-metal and bi-metal assemblies discussed in the Section 2. The FEA model of the quarter of the package used is shown in Figure 4. The boundary conditions are applied such that the XY and YZ planes were chosen as the planes of symmetry and y-translation in the XZ plane was

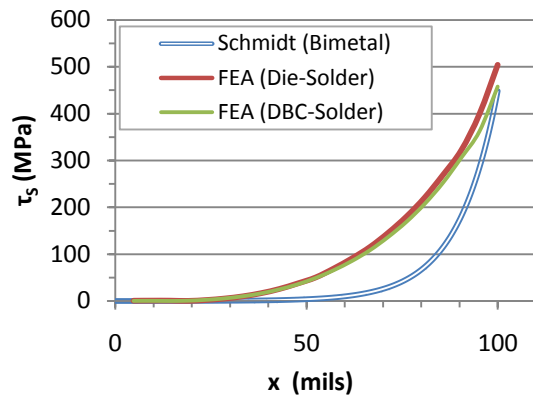


Figure 6: Variation of stresses along the length of the die for $\Delta T = 500^\circ\text{C}$.

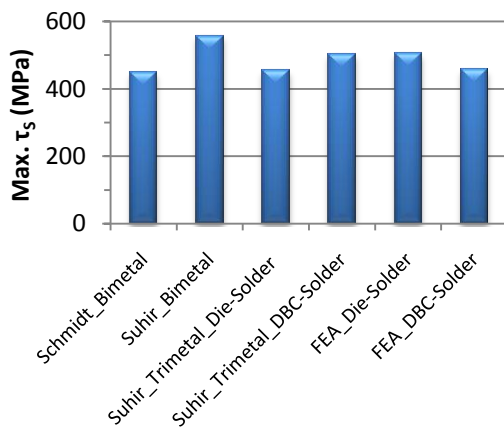


Figure 7: Maximum shear stress calculated using analytical and FEA methods ($\Delta T = 500^\circ\text{C}$).

zero. Also, the origin is fixed to eliminate any rigid body motion.

The magnitudes of the stress values at the die-solder and the solder-substrate interfaces were compared for the FEA and the analytical bi-metal model by Schmidt [11]. The distribution of shear stress at the plane of symmetry, calculated using the FEA method, is shown in Figure 5. It can be seen from the figure that the maximum stress is not at the edge of the die but a small distance away from it. This is because the FEA method calculates the stresses at the edge to be zero thereby causing this shift [11]. This artifact of the FEA method is ignored and the maximum stress is assumed to be at the edge of the die. The comparison from both methods, analytical and FEA, is shown in Figure 6. It can be seen that there is

close agreement for the maximum stress value at the edge (at $x = 100$ mils). The difference in the shape of the stress profile can be explained by the fact that the FEA model is three dimensional whereas the analytical model is based on a simpler, 2-dimensional approach. Also, a finer mesh will improve the accuracy of the results at the interfaces and the edges.

Similar analysis is conducted using the Suhir [10] tri-metal and bi-metal approach and the comparison of maximum shear stress from all the methods is shown in Figure 7. Since the method by Schmidt [11] for the bi-metal approach is in the closest agreement with the FEA results, it is selected for the further calculations. It is to be noted that for the bi-metal approach, the stress at the die-solder and solder-substrate are assumed equal.

4.2 Effect of Solder thickness

The thickness of the solder used for bonding dies to the substrate can significantly affect the magnitude of the shear and peeling stresses at the interfaces. Since the thickness of the solder can be controlled while building the power module, it is important to understand the relation between the solder thickness and the magnitude of the thermal stresses. Using the bi-metal approach by Schmidt [11], the primary stresses are calculated for the power package shown in Figure 1 for solder thickness of 0.1 mils up to 3 mils. The results for the maximum primary stresses for the various solder thicknesses at $\Delta T = 500^\circ\text{C}$ are presented in Figure 8.

It can be seen that the normal stress does not vary appreciably with change in solder thickness but the solder thickness has a significant effect on the shear and peeling stresses and these stresses decrease with increasing solder thickness. An important observation to be made is that the peeling stresses significantly drop in magnitude at about 1.5 mils solder thickness and beyond 1.5 mils, the stresses decrease more gradually and almost linearly with increasing solder thickness. Similar trends to that shown in Figure 8 are observed for thermal stresses for other temperature states i.e. $\Delta T = 50, 250$ and 700°C . Also, due to the low thermal conductivity of solders and epoxies, and with the small area of the SiC die, the thickness of solder alloy can significantly affect the heat dissipation rate from the die. Along with the stress analysis, the thermal analysis must be included for the selection criteria of solder type and thickness.

4.3 Selection of solder thickness based on maximum allowable stress.

There are several types of solders that can be used for

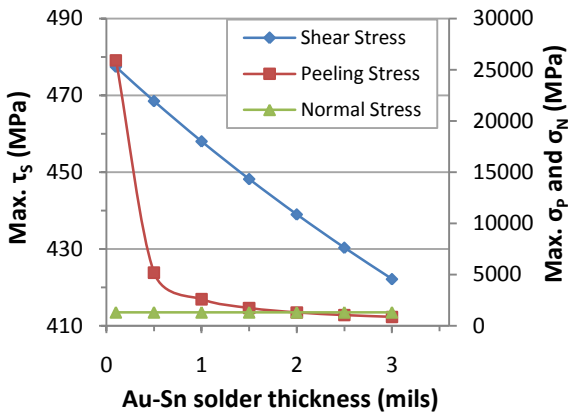


Figure 8: Effect of solder thickness on the primary stresses for $\Delta T = 500^\circ\text{C}$.

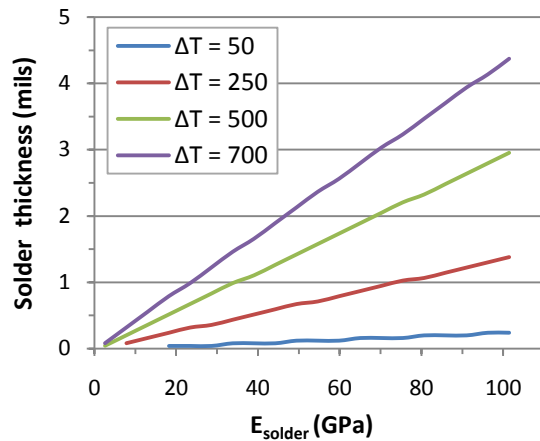


Figure 9: Minimum solder thickness required for a maximum peeling stress = 1500 MPa for a particular solder.

bonding which include hard solders, soft solders and metal-filled epoxies [8]. Metal-filled epoxies have poor thermal conductivity and can be very brittle (in the case of many high-temperature varieties) and hence can impact reliability. The soft solders such as Pb-Sn alloys have adequate thermal conductivity but are mechanically weaker. For high temperature applications, hard solders such as Au-Sn alloys are typically used. Hard solders have good thermal conductivity and higher elastic modulus and thus provide mechanically stronger bonds. In an attempt to provide packaging engineers with some guidance for solder selection, the bi-metal Schmidt [11] model is used to calculate the solder thickness required that will result in a maximum peeling stress of 1500 MPa.

The analysis is conducted for a range of solder elastic modulus (2-100 GPa) and for various temperature states (Figure 9). The range for the elastic modulus is selected such that it covers most commercial solders and the cut-off stress of 1500 MPa is selected such the solder thicknesses are within the maximum practical limit of 4-5 mils. The information in Figure 9 can be used to choose the appropriate solder based on its elastic modulus and the operating temperature such that the maximum peeling stress does not exceed 1500 MPa.

5.0 Design of trace on DBC and thickness of Cu layer

5.1 Effect of distance of die from trace on DBC

Most applications require several devices in a power module to increase the total power capacity. The devices are electrically separated at the base by a trace etched on the top Cu layer of the DBC (Figure 1). The distance of the edge of the trace from the die is a key design parameter that can affect the stress in the die-solder and solder-DBC interface. To analyze this effect, an FEA model consisting of a single die soldered on a full DBC (Cu- Al_2O_3 -Cu) is used. There is no simple analytical model available to analyze stresses in a module with greater than 3 layers; hence the FEA method is adopted. The FEA model is similar to the one shown in Figure 4 except the full DBC area is modeled. The maximum shear stress at the die-solder and solder-DBC interface are calculated for range of distances from the edge of the trace to the die, see Figure 10. The thicknesses of the Cu layers in the DBC are selected as 8 mils.

It can be seen in Figure 10 that the shear stresses are quite high for small distances (< 4 mils) and change direction (sign) as the distance increases. The stresses reach a maximum at about 20 mils and do not change appreciably beyond it. The shear stresses are less than maximum (positive and negative) for the distance between the 5 and 20 mils. This clearly indicates, that keeping all other design parameters fixed, the position of the trace can have a significant effect on the magnitude of the stresses. The change in the sign of stresses is because, as the size of Cu trace increases, it is able to overcome the negative shear stress induced by the SiC die.

5.2 Selection of Cu thickness on DBC.

The DBC is a standard substrate used for high temperature power modules due to the high thermal capacity and heat dissipation of the copper layer and the high thermal conductivity of the ceramic layer, Al_2O_3 in this case. Design engineers have several choices for the thickness of the Cu layer on the DBC. To analyze the effect of Cu thickness on the

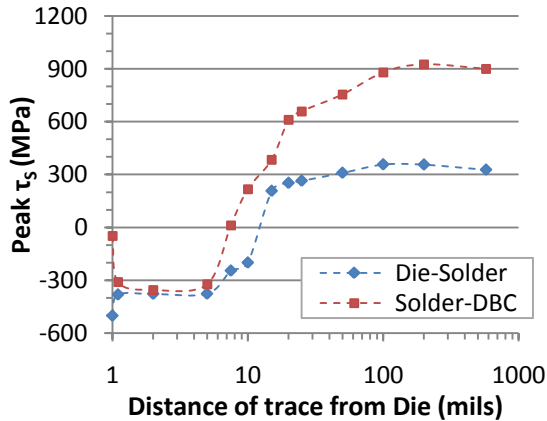


Figure 10: The effect of distance of edge of trace from die on the peak shear stresses at the interfaces (for $\Delta T = 500^\circ\text{C}$).

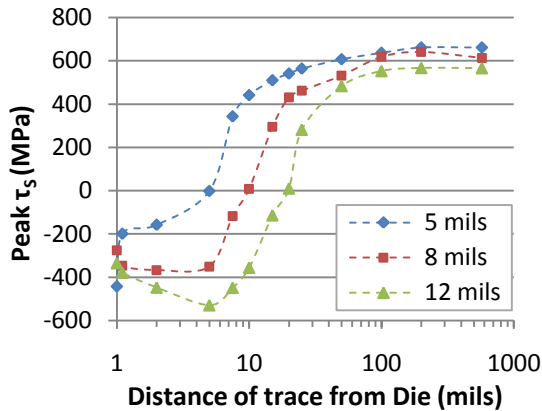


Figure 11: Variation of peak shear stress for various thicknesses of Cu layers ($\Delta T = 500^\circ\text{C}$).

maximum shear stress, the analysis shown in Figure 10 is repeated for Cu thickness of 5 and 12 mils. To simplify the analysis of the results, the average of the maximum shear stress at the die-solder and solder-DBC interface is plotted for all Cu thicknesses, see Figure 11. From the figure it can be seen that the peak shear stress is higher for the 12 mils thickness for distances $< \sim 10$ mils. However, for distances larger than 10 mils from the die, the stress is higher for lower Cu thicknesses. Hence, to keep the stresses at a minimum, the selection of the Cu thickness is dependent upon the position of the traces relative to the die. Also, if the distance of the trace is larger than 100 mils, then the stresses are quite similar for all three Cu thicknesses and the Cu thickness can be selected independently. Cost, voltage, and current requirements, and thermal performance will also influence the selection of the Cu thickness.

6.0 Conclusions

The FEA model is compared with the known analytical solutions and this supports the validity of our findings. It is shown that the solder thickness selection, position of traces on DBC and Cu layer thicknesses, significantly affect the magnitude of the shear stresses at the interfaces. The higher peak stresses will accelerate the other failures including fatigue and corrosion. In section 4.3 it was shown that the peeling stresses drop significantly at solder thickness > 1.5 mils. Also, the position of the edge of the trace from the die and the Cu thickness are interrelated design parameters and must be selected to minimize the peak stresses and increase the performance life of the power module. Future work will include incorporation of temperature dependent material properties of Au-Sn alloy. Also, other failure mechanisms such as fatigue life will be included in the analysis.

7.0 References

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