

Efficient Gate Drive Mechanism for Novel Silicon Carbide Power FETs

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Abstract

A novel method for driving high side switch of a synchronous rectifier is described. A gate drive mechanism with signal and power transfer through coreless planar transformer is presented. The transformer is implemented in commercial polyimide printed circuit board technology in an area of 13 mm x 13mm. Enhancement mode silicon carbide junction field effect transistors and a custom designed silicon-on-insulator based controller chip are used in conjunction with the gate drive transformers to establish their functionality and performance. A design procedure based on transfer function analysis is presented. The proposed drive mechanism is applicable for extremely wide temperature range operation.

Keywords - gate drive, smps, PCB transformer, silicon carbide, PCB, verilog-A, JFET

1. Introduction

Efficient gate drive design is a key challenge in designing switch mode power supplies. The requirements of a gate drive differ from one type of converter to another. Floating power supplies and feedback control using optocouplers are used to turn ON/OFF the power devices of a synchronous rectifier. Since high speed switching optocouplers for high temperature environment is not commercially available, transformer coupled gate drive is used as an alternative. Also the availability of a floating power source is not practical or commercially desirable in many cases. Therefore achieving power in addition to control transfer through an inductive coupling is very attractive. A conventional core type transformer for this purpose is not efficient in terms of volume occupied and used only when high power gate drives are required. For medium and low power drive requirements, recent studies illustrate the use of coreless planar transformers for volume efficient designs [1, 2]. However no attempt has been made to study the analytical behavior of the transformer including the source and load. Here we present in detail the transfer function modeling of the transformer and an associated design procedure.

A block diagram of the proposed gate drive mechanism with a vee-square controller IC chip and silicon carbide enhancement mode JFETs are shown in figure 1. A detailed mathematical analysis of the coreless planar gate drive transformer at a system level is given in section 2. The advantage of using the silicon carbide devices is discussed in section 3. A

brief description of the custom designed controller IC is provided in section 4. The performance of the prototype converter and the associated gate drive circuitry is discussed.

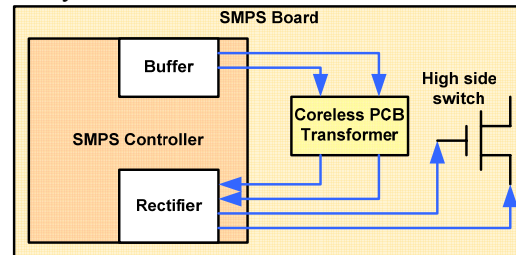


Figure 1. Block diagram of the PCB transformer coupled driver.

Nomenclature

R_s	source resistance
R_{lp}	dc resistance of primary winding
R_{ls}	dc resistance of secondary winding
R_{dc}	dc resistance, assuming $R_{dc} = R_{lp} = R_{ls}$
R_l	load resistance
L_{lp}	leakage inductance in primary side
L_{ls}	leakage inductance in secondary side
L_l	leakage inductance, assuming $L_l = L_{lp} = L_{ls}$
L_m	mutual inductance
L_p	self inductance of primary winding
L_s	self inductance of secondary winding
C_f	feed forward capacitance
C_l	load capacitance
ω_n	natural resonance frequency
ζ	damping factor
f	operating frequency
T_r	rise time
T_g	glass transition temperature

2. Coreless Planar Transformer

Coreless planar transformers (CPT) fabricated on the printed circuit boards are popular for low power gate drives. The availability of well established PCB technologies and the ability to integrate CPTs and their control electronics on the same PCB as the power supply make this very attractive.

Two critical parameters in the design of CPT are the leakage inductance and winding capacitance. The leakage inductance affects the mutual coupling between the primary and secondary windings and hence limits the transformation ratio. Interwinding and intrawinding capacitances limit the useful bandwidth of the CPT design. Minimizing these performance limiting factors are not independent since any measure to improve the mutual coupling also increases the capacitance. The various structures for on-chip transformer implementation on silicon substrate were previously presented [3]. In general a planar structure minimizes the stray capacitance and hence is suitable for high frequency applications. The physical size of the transformer is directly dependent upon the frequency of operation. Typically very high frequency designs (greater than 500 MHz) benefit more from on-chip transformers instead of off-chip PCB solutions. For off chip CPTs the maximum operating frequency is limited to few MHz.

2.1. Mathematical Analysis of CPT

The turns ratio in the transformer is assumed to be unity in following analysis. This simplifies the analysis to some extent while being extendable to transformers with non unity transformation ratio. The 'T' equivalent circuit of the transformer used for the mathematical analysis is shown in figure 2. The model includes the parasitic capacitances and resistance of the transformer winding. The behavior of the transformer is also dependent upon the source and load characteristics and hence is included in the model. Applying nodal analysis in the s domain, the

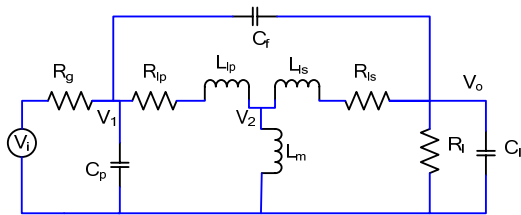


Figure 2. Equivalent circuit model of the transformer including parasitic, source and load components.

transfer function of the equivalent circuit in figure 2 is obtained. Since the overall transfer function is very complicated with fourth order terms in numerator and denominator, suitable simplifying assumptions are made to reduce the complexity.

It is reasonable to assume the leakage inductance of the primary and secondary windings and their dc resistances are equal for a 1:1 transformer. Though this does not reduce the order of the system, it greatly reduces the number of parameters. The simplified transfer function is given in the appendix A. With use of Matlab®, the frequency response of the transfer function is observed for nominal values of the components. The values are based on previous reports on CPT and given source and load specifications for this project. Figure 3 shows the magnitude and phase response of 1) simplified system (blue curves), 2) simplified system with $R_{lp}=R_{ls}=0$ (green curves), and 3) simplified system with $R_{lp}=R_{ls}=R_g=0$ (red curves). It can be clearly seen that the dc resistance of the primary and secondary coils along with the generator resistance influence the low frequency gain of the system. The response for an ideal source with zero source resistance is largely different from a practical source. Hence the parasitic resistance of the windings along with the generator resistance are the limiting factors that set the lower operating frequency for transformer.

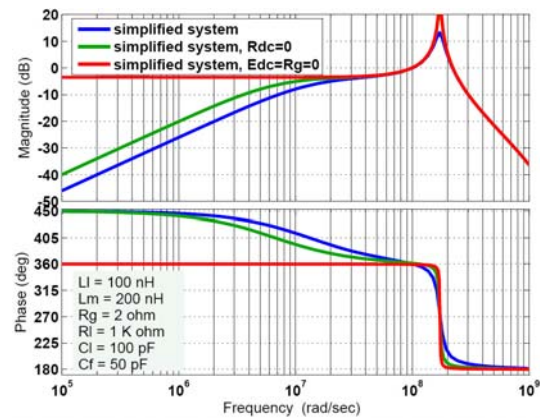


Figure 3. Bode plots of the complete system with several approximations.

Conventionally the gate drive transformers referred as pulse/video/broadband transformers are analyzed with the rise time, top of the pulse and fall time of the input pulse in mind [4]. Based on the different pulse parameter subsections, corresponding equivalent circuits are developed by elimination of non-dominant components. This typically results in low and high frequency models.

2.1.1. Rise time analysis

A high frequency equivalent circuit model is considered for the rise time analysis of the transformer. Figure 4 shows the equivalent circuit corresponding to pulse rise time. Applying nodal analysis the transfer function of the system is obtained (see appendix A). It is reasonable to assume that the load resistance is much greater than source resistance, as a result of typical high side switch being a FET. Further assumptions are made such as equal leakage inductance in primary and secondary and negligible resistance for the windings, to represent the transfer function as a standard second order system[5].

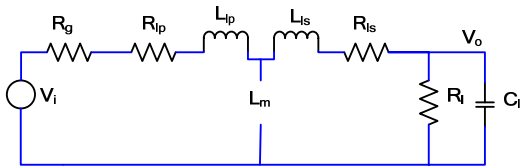


Figure 4. Equivalent circuit for the rise time of the input pulse.

Hence comparing the derived transfer function with standard second order system, the natural resonance frequency of the system and the damping ratio are given by equations 1 and 2 respectively. The rise time is given by equation 3.

$$\omega_n = \frac{1}{\sqrt{2 \cdot L_l \cdot C_l}} \quad [1]$$

$$\zeta = \frac{R_g}{\sqrt{8} \sqrt{L_l / C_l}} + \frac{\sqrt{L_l / C_l}}{\sqrt{2} \cdot R_l} \quad [2]$$

$$T_r = \frac{\pi - \cos^{-1}(\zeta)}{\omega_n \cdot (1 - \zeta^2)^{0.5}} \quad [3]$$

The load capacitance, load resistance and rise time are usually specified as design inputs. It is also desirable to obtain a damping coefficient less than 0.707 to satisfy a critical damping requirement. Therefore using the given values in the equations 1 and 2 a relation between the leakage inductance and source resistance can be obtained. For a load capacitance of 200 pF in parallel with 2K Ω and a rise time of less than 50nS, leakage inductance and source resistance requirements are as given in equation 4 and 5.

$$0 \leq L_l \leq 5.5 \times 10^{-7} H \quad [4]$$

$$R_g = \sqrt{L_l} \cdot (1.414 \cdot 10^5 - 5 \cdot 10^6 \cdot \sqrt{L_l}) \quad [5]$$

Often the source resistance of the drivers is fixed to the lowest possible value while avoiding under-damping. As seen from the previous section an ideal source with zero resistance provides excellent low frequency response. In the current work the generator resistance is given to be 2 ohms. Therefore to satisfy the critical damping constraint with this source resistance, the leakage inductance has to be lower than 0.2 nH. This is a very small value and cannot be obtained in practice. Hence it is not possible to obtain the desired rise time for given conditions with a critically damped system. However the damping requirement shall be relaxed. The resulting low damping coefficient results in oscillatory behavior for a unit step input. The step response of the rise time equivalent circuit (red curve) and the complete equivalent circuit (blue and green curves) are shown in figure 5. The overshoot value is much higher in approximated rise time equivalent circuit response compared to the complete system. This is an indicator of the trade off in accuracy due to various assumptions made in the rise time transfer function derivation.

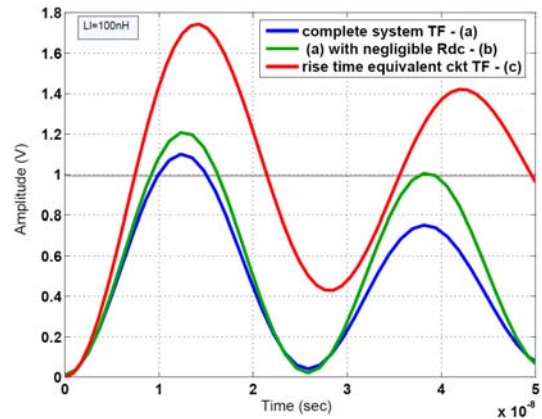


Figure 5. Step response of the transfer function representing the rise time equivalent circuit and complete equivalent circuit.

Therefore a suitable option is to limit the leakage inductance to meet the required rise time and trade off the low damping. In special cases an external series resistance can be added between the source and the primary windings to improve damping.

2.1.2. Pulse top analysis

In contrast to pulse transformers the gate drive circuitries often involve a rectifier at the secondary side. The use of rectifiers in the secondary side reduces the constraints in the pulse top period. The approximated equivalent circuit for the pulse top

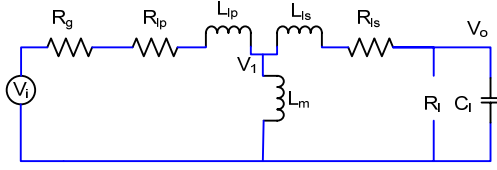


Figure 6. Equivalent circuit for the pulse top duration.

duration is shown in figure 6. A complete transfer function of this circuit yields a 5th order system. A simplified expression obtained by assuming equal leakage inductances and negligible dc winding resistance is given in appendix-A. Further assuming a negligible leakage inductance, the following relationship is obtained.

$$\frac{V_o}{V_i} = \frac{s \cdot \left(\frac{L_m}{R_g} \right)}{1 + s \cdot \left(\frac{L_m}{R_g} \right)} \quad [6]$$

Equation 6 indicates the response of the system during pulse top duration is dominated by the mutual inductance and dictates a low source resistance. Hence a high mutual inductance and a low source resistance are preferred.

The time constant of the primary side series RL circuit imposes a minimum required self inductance to keep the power dissipation lower. The droop in secondary voltage is proportional to the pulse duration. As a rule of thumb the on time of the circuit has to be lower than 10% of the time constant. Hence for a given operating frequency, the minimum required self inductance is given by equation 7 [6], where $T_{on}=1/f$ and R_p is the sum of the source and primary winding resistance.

$$T_{on} \leq 10\% \left(\frac{L_p}{R_p} \right) \Rightarrow L_p \geq 10 \cdot R_p \cdot T_{on} \quad [7]$$

For a given operating frequency, it is recommended to use a differential buffer to drive the transformer since a single ended drive can saturate the winding easily. Also due to differential switching, the fall and rise time analysis are identical.

2.2 Transformer Design

Based on the previous discussions there exists more than one way of designing the transformer. One such approach is disclosed in the following discussion. Of all the transformer

structures, stacked transformers provide higher mutual coupling and are also easy to layout. A pictorial 3-D view of a stacked structure used in this study is shown in figure 7. The transformer area is usually desired to be minimum and hence mostly a given constraint. Results from previous reports on CPT are used in selecting a starting area for design. However the number of turns, spacing between the conductors and the conductor width are arbitrary to the designer.

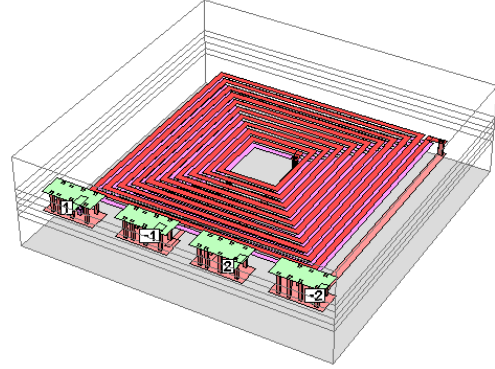


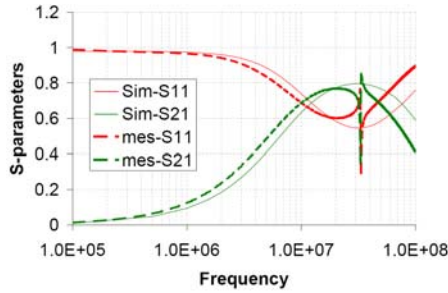
Figure 7. Layout of planar stacked transformer considered in this work.

The inductance of the winding is proportional to the square of the turns and is logarithmically dependent upon the conductor width. Hence it is advisable to use lean conductors with large turns to achieve high inductance. The spacing between the adjacent conductors affects the flux linkage between the two and hence influences the self inductance. Hence a closer spacing yields better performance but higher parasitic capacitance. Most PCB process rules sets a minimum line and space width that sets the minimum limit for conductor width and spacing. Also since PCB transformers are coreless candidates the internal area has no/minimal effect in the operation. In special cases magnetic materials are introduced as core to increase the value of inductance.

For the design exercise a transformer with specifications as given in table 1 was fabricated and tested to analyze its performance. A 2 port push-pull analysis of the selected structure is simulated in the Sonnet® software, based on the finite element analysis. The transmission (S11) and reflection (S21) coefficients are observed and shown in figure 8. The same characteristics for the fabricated transformer are measured using network analyzer and are also appended in figure 8.

Table 1. Specifications of the gate drive transformer.

Parameter	Value
Structure	Stacked
Area	13 mm x 13 mm
Conductor width	10 mil
Conductor spacing	6 mil
Number of turns	10
Turns ratio	1:1
Dielectric thickness	12 mil
Material	RO 4350 – Tg>280°C
Copper thickness	1 Oz

**Figure 8. Measured and simulated values of s-parameters of the two port transformer.**

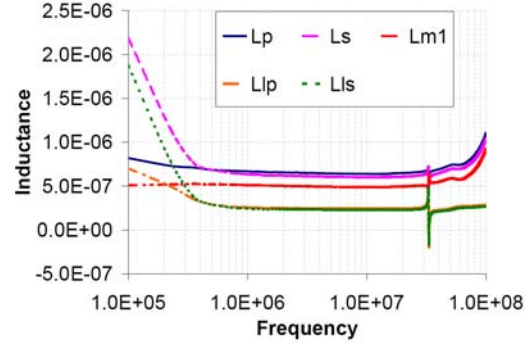
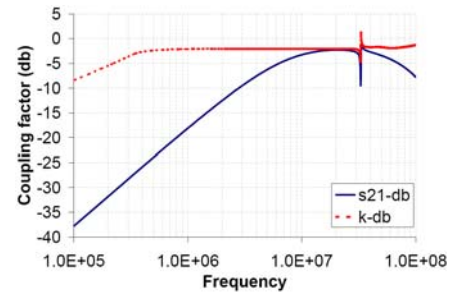
The curves show a good agreement between the simulated and measured value. Standard SOLT calibrations are performed prior to measurement. From the measured results, the bandwidth is calculated to be greater than 60 MHz. This wide bandwidth allows higher harmonics of the input pulse to couple through, which in turn improves the rise performance of the transformer.

From the measured S-parameters of the two port network, the individual parameters are extracted assuming a wide band model. The inductances are calculated using equation 8 assuming the inductance dominates the effect in the frequency of interest. The calculated self, mutual and leakage inductance are shown in figure 9.

From figure 10, it can be observed that the measured transmission coefficient which is equivalent to be power gain of the system is maximized when the source impedance is matched to the load impedance. The coupling coefficient as a measure of voltage gain is calculated from the extracted leakage and mutual inductance using equation 9. The measured values of mutual and leakage inductance are 550 nH and 200 nH, respectively and a coupling coefficient greater than 75% is obtained from the structure.

$$L_p = \frac{\text{Im}(Z_{11})}{2 \cdot \pi \cdot f} \quad [8]$$

$$k = \frac{L_m}{\sqrt{L_p \cdot L_s}} \quad [9]$$

**Figure 9. Extracted values of primary and secondary inductance, mutual inductance, and leakage inductance.****Figure 10. Comparison of measured transmission coefficient (S21) and the calculated coupling coefficient (k).**

3. Power FET

The usability of coreless PCB transformers for power transmission to high side switch is limited by its design constraints such as area and power dissipation and is not universally suitable for any power device. Conventional MOS type and bipolar power devices have high gate voltage or base input current requirement. This demands considerable power to turn on these devices. The newer generation silicon carbide JFETs breaks this barrier. Feasibility of enhancement mode JFETs that block several thousands of volts and with smaller threshold voltage is established [7, 8]. These devices are also extreme temperature harsh environment tolerant due to their wide bandgap structures. The device characteristics of these devices are measured in the lab and a simple verilog-A model for the device was developed from the important parameters derived from the test results. The electrical characteristic of the devices at

higher temperature was presented earlier [9]. The verilog-A model with the planar transformer model was used to simulate the behavior of the gate drive system.

4. System Performance

A vee-square control based synchronously switched step down dc-dc converter has been designed with the silicon carbide devices and the PCB gate drive transformers. A MOS switch based rectifier circuit used in the secondary side of the transformer is shown in figure 11. Unlike conventional full wave rectifiers (FWR) using diodes the proposed switch based rectifiers does not need any forward voltage to turn ON and hence are more efficient having only and R_{DSon} .

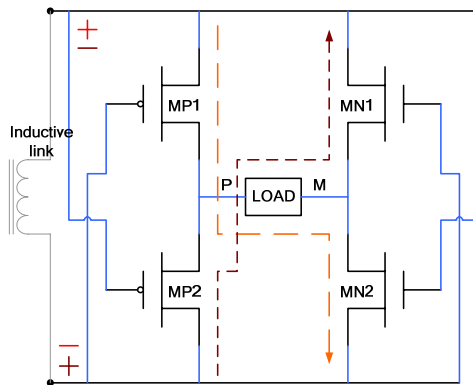


Figure 11. On chip full wave rectifier using complementary MOS switches

During turn OFF the decaying of the voltage at the load is set by the passive RC time constant, figure 12. To enhance the decay an active circuit as shown in figure 12 is proposed. The time constant for the RC network that controls the turn off switch 'MD' is chosen such that the circuit remains ineffective in the ON period. The diode connected device BC acts as a blocking diode to prevent cross conduction during the turn ON and turn OFF of alternate switch pairs in FWR, figure 11.

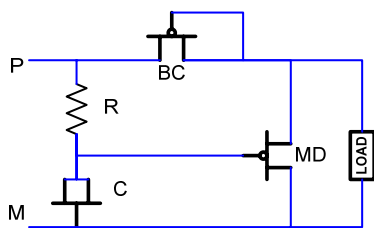


Figure 12. Active discharge circuit with diode blocking cross conduction.

4.1. Circuit board assembly

The transformer drivers and rectifiers, the power switches and the PCB transformer itself are mounted on an aluminum nitride mother board to form a complete switch mode power supply (SMPS). The aluminum nitride is selected due to its high thermal conductivity. As a heat spreader, the material helps in removing the heat from the power transistor junctions operating at high ambient temperature. The complete assembly that involves epoxy, eutectic and wire bonding is shown in figure 13.

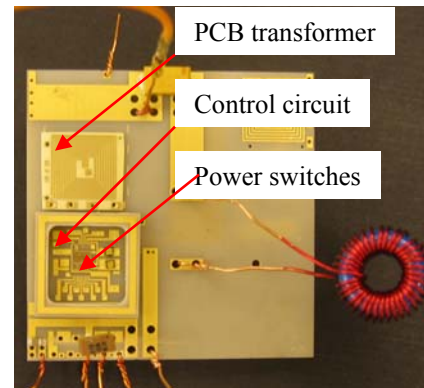


Figure 13. Circuit board assembly of the switch mode power supply with on board control dice, power switches and PCB transformer.

The simulated waveforms related to the gate drive circuitries are presented in figure 14. The figure shows the voltage across the primary (top) and secondary windings (middle), the fall and rise characteristics of the rectified voltage and the control signal (bottom). The source resistance is about 3Ω and load capacitance and resistance are 200 pF and $2K\Omega$ respectively. The switching frequency is 10 MHz. The average value of rectified voltage is about 2.9V which is sufficient to drive the power FET in deep triode. The rise and fall times are lesser than 50 nS.

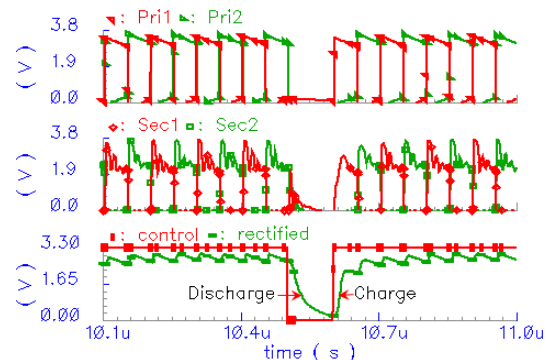


Figure 14. Waveforms at various stages in the high side switching Circuit.

5. Conclusion

A novel design method for high side switch is presented based on a simple CPT model. The design methodology is extended using simulations and s-parameter measurements. Further refinements to the design were carried out using SPICE and Matlab simulations to achieve an optimum CPT. The novel use of power efficient switched rectifier circuit is also presented.

A design flowchart based on the simple models is presented in figure 15. The planar PCB transformers present advantages such as low cost, low volume, high operating voltage. However being coreless, the operation of PCB transformers are considerably different than a conventional transformer, whose performance largely depends on the core. The complex transfer functions and nonlinear load at the secondary side make accurate mathematical representation of the planar transformer difficult and time consuming. Nevertheless the performance is verified by the analytical and experimental methods. The PCT is robust such that minor changes in its physical parameters or electrical parameters do not significantly affect their performance. A good performance of a prototype of SMPS using PCB transformer gate drive has been verified at 275°C.

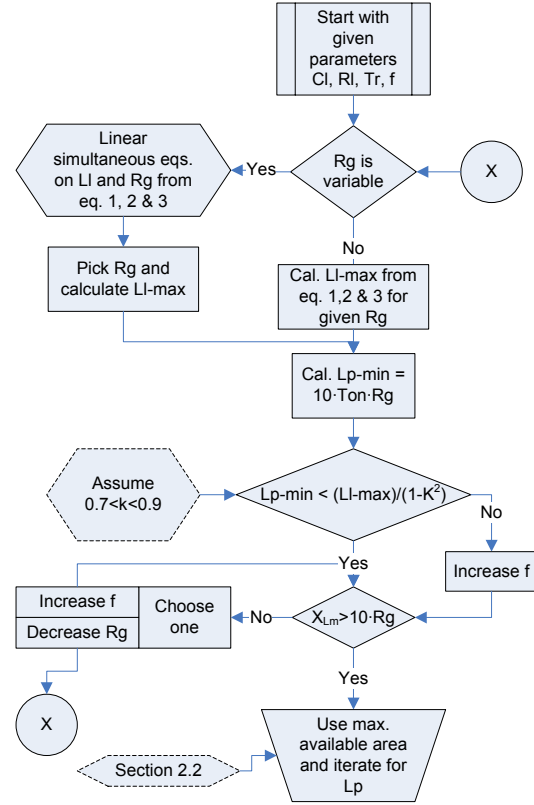


Figure 15. Design flowchart.

6. Appendix – A

6.1. Transfer function of complete equivalent

$$\begin{aligned}
 & R_l \cdot s \cdot (C_f \cdot L_l \cdot R_g \cdot s^3 \cdot (C_f + C_p) \cdot (L_l + 2 \cdot L_m) + C_f \cdot s^2 \cdot (2 \cdot C_f \cdot R_{dc} \cdot R_g \cdot (L_l + L_m) \\
 & + 2 \cdot C_p \cdot R_{dc} \cdot R_g \cdot (L_l + L_m) + L_l \cdot (L_l + 2 \cdot L_m)) + C_f \cdot s \cdot (C_f \cdot R_{dc}^2 \cdot R_g) + C_p \cdot R_{dc}^2 \cdot R_g \\
 & + (L_l + L_m) \cdot (2 \cdot R_{dc} + R_g)) + C_f \cdot R_{dc} \cdot (R_{dc} + R_g) + L_m \\
 & \hline
 & L_l \cdot R_g \cdot R_l \cdot s^4 \cdot (C_f + C_l) \cdot (C_f + C_p) \cdot (L_l + 2 \cdot L_m) + s^3 \cdot (2 \cdot C_f^2 \cdot R_{dc} \cdot R_g \cdot R_l \cdot (L_l + L_m) \\
 & + C_f \cdot (2 \cdot C_l \cdot R_{dc} \cdot R_g \cdot R_l \cdot (L_l + L_m) + 2 \cdot C_p \cdot R_{dc} \cdot R_g \cdot R_l \cdot (L_l + L_m) + L_l \cdot (L_l + 2 \cdot L_m) \cdot (R_g \\
 & + R_l)) + C_l \cdot R_l \cdot (2 \cdot C_p \cdot R_{dc} \cdot R_g \cdot (L_l + L_m) + L_l \cdot (L_l + 2 \cdot L_m) + C_p \cdot L_l \cdot R_g \cdot (L_l + 2 \cdot L_m)) \\
 & + s^2 \cdot (C_f^2 \cdot R_{dc}^2 \cdot R_g \cdot R_l + C_p \cdot R_{dc}^2 \cdot R_g \cdot R_l + 2 \cdot L_l \cdot (R_{dc} \cdot (R_g + R_l) + R_g \cdot R_l) \\
 & + L_m \cdot (2 \cdot R_{dc} \cdot (R_g + R_l) + R_g \cdot R_l) + C_l \cdot R_l \cdot (C_p \cdot R_{dc}^2 \cdot R_g \cdot (L_l + L_m) \cdot (2 \cdot R_{dc} + R_g)) \\
 & + C_p \cdot R_g \cdot (L_l + L_m) \cdot (2 \cdot R_{dc} + R_l) + L_l \cdot (L_l + 2 \cdot L_m) + s \cdot (C_f \cdot R_{dc} \cdot (R_{dc} \cdot (R_g + R_l) \\
 & + 2 \cdot R_g \cdot R_l) + C_l \cdot R_{dc} \cdot R_l \cdot (R_{dc} + R_g) + C_p \cdot R_{dc} \cdot R_g \cdot (R_{dc} + R_l) \\
 & + (L_l + L_m) \cdot (2 \cdot R_{dc} + R_g + R_l)) + (R_{dc} + R_g) \cdot (R_{dc} + R_l)
 \end{aligned} \tag{10}$$

6.2. Transfer function of the rise time equivalent circuit

$$\frac{V_o(s)}{V_i(s)} = \frac{R_l}{s^2 \cdot C_l \cdot R_l (L_l p + L_{ls}) + s \cdot (C_l \cdot R_l \cdot (R_g + R_{lp} + R_{ls}) + L_{lp} + L_{ls}) + R_g + R_l + R_{lp} + R_{ls}} \quad [11]$$

6.3. Transfer function of the pulse top period equivalent circuit

$$\frac{V_o(s)}{V_i(s)} = \frac{L_m \cdot R_l^2 \cdot s}{s^5 \cdot C_l^2 \cdot L_l^2 \cdot L_m \cdot R_l^2 + s^4 \cdot C_l \cdot L_l \cdot L_m \cdot R_l \cdot (C_l \cdot R_g \cdot R_l + 2 \cdot Ll) + s^3 \cdot Ll \cdot (C_l \cdot R_l \cdot (Ll \cdot R_l + L_m \cdot (2 \cdot R_g + R_l)) + L_l \cdot L_m) + s^2 \cdot L_l \cdot (C_l \cdot R_g \cdot R_l^2 + L_l \cdot R_l + L_m \cdot (R_g + R_l)) + s \cdot R_l \cdot (L_l \cdot (R_g + R_l) + L_m \cdot R_l) + R_g \cdot R_l^2} \quad [12]$$

7. References

- [1] S. C. Tang, S. C. Tang, S. Y. Hui, and C. Henry Shu-Hung, "Coreless planar printed-circuit-board (PCB) transformers-a fundamental concept for signal and energy transfer," *Power Electronics, IEEE Transactions on*, vol. 15, pp. 931-941, 2000.
- [2] S. C. Tang, S. Y. R. Hui, and H. Chung, "Coreless printed circuit board (PCB) transformers with high power density and high efficiency," *Electronics Letters*, vol. 36, pp. 943-944, 2000.
- [3] J. R. Long, "Monolithic transformers for silicon RF IC design," *Solid-State Circuits, IEEE Journal of*, vol. 35, pp. 1368-1382, 2000.
- [4] S. Moskowitz and J. Racker, *Pulse Techniques*. New York: Prentice-Hall, Inc., 1953.
- [5] M. Gopal, *Control systems : principles and design*, 1 ed. Dubuque, Iowa: McGraw-Hill, c2008.
- [6] R. Nagel, "Transformer design considerations for noncontinuous mode, boost, flyback converters," in *Electrical Electronics Insulation Conference, 1995, and Electrical Manufacturing & Coil Winding Conference. Proceedings, 1995*, pp. 153-155.
- [7] C. Young Chul, C. Ho-Young, L. F. Eastman, and M. G. Spencer, "A new 4H-SiC normally off lateral channel vertical JFET with extremely low power losses: source inserted double-gate structure with a supplementary highly doped region," *Electron Devices, IEEE Transactions on*, vol. 52, pp. 1940-1948, 2005.
- [8] M. Su, K. Sheng, Y. Li, Y. A. Z. Y. Zhang, J. A. W. J. Wu, J. H. A. Z. J. H. Zhao, J. A. Z. J. Zhang, and L. X. A. L. L. X. Li, "430-V 12.4- μ s normally off 4H-SiC Lateral JFET," *Electron Device Letters, IEEE*, vol. 27, pp. 834-836, 2006.
- [9] V. Madhuravasal, S. Venkataraman, C.-M. Liu, and C. Hutchens, "Extreme Temperature Switch Mode Power Supply based on Vee-square Control Using SiC, Si on Sapphire, Hybrid Technology," in *IMAPS International Conference and Exhibition on High Temperature Electronics*, Albuquerque, New Mexico, USA, 2008.