

Evaluation of DirectFET® Flip Chip Packaging Technology, Lead and Indium Solder Alloys in Extreme Cold Thermal Environments

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Abstract

DirectFET® packaging technology, developed by International Rectifier Corporation, offers substantial improvements in thermal and power efficiencies for power MOSFETs while also reducing device form factor. The use of these devices in space applications could serve to significantly extend mission life by reducing power consumption onboard satellites, deep space probes and planetary rovers. Further thermal and power efficiencies could also be reaped by mounting the power electronics with a thermal conduction path to the spacecraft body. However, exposure to the extreme temperatures in these environments has deleterious effects on some electronics assembly integrity and reliability and has to date, kept electronic hardware within the thermally regulated interior of the spacecraft. To evaluate the effects of these environments on electrical performance and reliability, several sets of DirectFET® assemblies were fabricated using a variety of lead and indium solder alloys and subjected to temperature cycling. The testing sought to simulate three extreme thermal environments: the "high reliability" environment (-65°C to +150°C), the Mars environment (-120°C to +115°C) and the Deep Space environment (-180°C to +85°C). Results of electrical testing, cross-sectional analyses, and thermomechanical stress simulations are presented within this article.

Key Words: Extreme Environments, Flip Chip, DirectFET®, Reliability

1. Introduction

International Rectifier (IR) developed a new form of MOSFET packaging known as DirectFET® (Figure 1), which it introduced in 2003 into commercial production. This new packaging concept was designed to address a number of the shortcomings of conventional SO-8 plastic packaging, which is used for most commercial power MOSFETs: high thermal resistance, high on resistance, and reduced power efficiency [1]-[4]. Figure 2 illustrates the differences between the two types of packaging construction.

In the DirectFET® package, the backside drain connection of the IC provides an unimpeded thermal pathway to the copper lid which acts as an efficient heat spreader. The flip chip connections of the source and drain to the PWB also provide good thermal pathways. The net result is a package with reduced junction to lead thermal resistances of up to 75 percent over plastic SO-8 packaging [1][2][5]. The

improved thermal performance also translates to a lower R_{dsOn} resistance and lower power consumption at the same drain current values [5].



Figure 1 . DirectFET® MOSFET Packaging
(image courtesy of International Rectifier)

High thermal and electrical efficiency is of great importance in the design of satellites and vehicles for extra-terrestrial exploration and deep space missions where a key objective is to maximize mission life. To achieve this end, electrical power consumption must be minimized to extend the life of

the batteries whose relatively short life span is often the limiting factor.

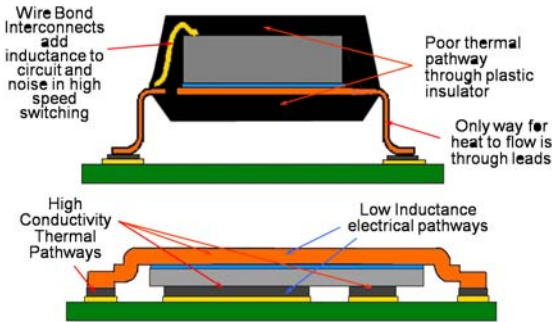


Figure 2 . SO-8 plastic packaging vs. DirectFET®

In an effort to improve the power efficiency of their deep space probes and planetary rovers, NASA Jet Propulsion Laboratory (JPL) has been studying the performance of DirectFET® packaged MOSFETs [5][6]. Of interest is their reliability in the extreme thermal environments of Mars (-120°C to +115°C) and in deep space (-180°C to +85°C) [7]. Potentially these devices could be placed external to the thermally controlled environment within the spacecraft body to yield improved efficiency and reduce the overall system power consumption.

Subjecting soldered assemblies to such extreme environments imposes large stresses on solder joints, leading to solder creep and fatigue [8]. This is especially a concern for non-leaded SMT devices such as flip chips, BGAs and CCAs, whose construction is similar to DirectFET®s. The unsupported solder joints of these devices are acutely susceptible to this type of damage. Numerous studies have examined their reliability with lead-tin eutectic (Sn63:Pb37) solder in various extreme thermal environments [7][9]. Provided proper care is taken with the materials selection and assembly processing, the studies demonstrated assemblies could survive through hundreds of temperature cycles without failure.

Indium alloys could potentially be a more reliable alternative to lead-tin eutectic alloys. The latter are prone to creep and fatigue and become brittle below -110°C [10]. The use of indium solder alloys has been investigated in SMT assemblies under extreme conditions with mixed results[11][12].

To better understand and evaluate the effects of these thermal environments on DirectFET®s and to investigate the reliability of indium solder alloys, several sets of these devices assembled on PWBs were subjected to extreme temperature cycling that

simulated the Mars and deep space environments. This study evaluated these devices soldered with conventional lead-tin eutectic solder alloy as well as two indium alloy compositions, Sn77.2:In20:Ag2.8 and Pb60:In40. The assemblies were electrically tested over the course of temperature cycling and finally subjected to cross-section analysis, the results of which are reported herein. Thermo-mechanical simulations of the assemblies were also undertaken and the results compared against the experimental data in this study.

2. Extreme Temperature Cycling

2.1 Experimental

2.1.1 Test Assemblies

Two DirectFET® device types were selected for this study: IRF6635 (30V device) and IRF6644 (100V device). Additionally, two versions of the IRF6635 were evaluated, referred to as IRF6635V1 and IRF6635V2, representing an older and a newer device design, respectively. These devices, shown in Figure 3, are representative of the range of different device performance ranges and construction (“large” versus “small” flip chip pads). Additionally, the IRF6635V2 and IRF6644 had source and drain pads that were pre-tinned with SAC305 solder alloy. The pre-tinned bumps act as shims, insuring a consistent solder joint height and volume.

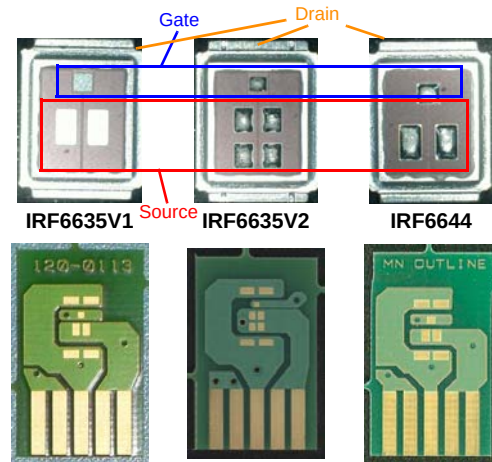


Figure 3 . Test Circuit Boards and Devices

The devices were mounted onto three different circuit board designs shown in Figure 3. The board designs were obtained from IR and fabricated using standard epoxy FR-4 laminate materials and 0.5 oz. copper with ENIG surface finish.

The test assemblies were fabricated using automated assembly equipment and three different

Type III, solder pastes: lead-tin eutectic (Sn63:Pb37), Sn77.2:In20:Ag2.8, and Pb60:In40. The lead tin paste, Kester R596, used a water soluble flux while the indium bearing pastes used a no-clean flux, Indium Corp NC-SMQ. The indium alloys were selected partly as “drop-in” alternates to the lead-tin eutectic alloy, since these have their liquidus’ at approximately the same temperature as the eutectic point of Sn63:Pb37. The Sn77.2:In20:Ag2.8 solder alloy also has the virtue of being lead-free..

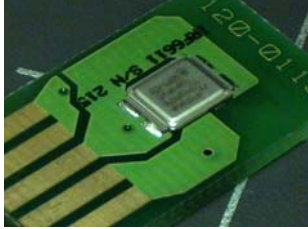


Figure 4 . Electronic Test Assembly

A finished assembly is depicted in Figure 4. 20 lead-tin eutectic assemblies of IRF6635V1 and IRF6635V2 devices and 40 lead-tin eutectic assemblies of IRF6644 devices were fabricated. Ten assemblies each with the three device types were fabricated with Sn77.2:In20:Ag2.8 and Pb60:In40 solders. Five control units for each part type were fabricated using lead-tin eutectic solder. The control samples were not temperature cycled and were used to correct for test instrument drift

2.1.2 Temperature Cycle Testing

The test assemblies were sequentially subjected to three sets of temperature cycles as described in Table I. Set 1 temperature cycling is the standard temperature cycling that space level assemblies are often subjected to for screening and qualification. Sets 2 and 3 test conditions and temperature limits were taken from work performed by Rameshan [7].

The set 2 and 3 temperature cycle conditions are designed to subject the parts to conditions which more closely resembled real world cycling yet while doing it in a reasonable period of time. The relatively slow ramp rate and long dwell at the elevated temperatures would subject the solder joints to low cycle fatigue and creep [8]. In contrast, the rapid temperature cycling rate and short dwells that are specified by MIL-STD-883 subject the assemblies to high cycle fatigue which is in some ways less damaging as the assembly materials do not have time to come to full equilibrium, minimizing creep.

Test set 1 was performed using a Ransco Temperature Cycle chamber. Assemblies were electrically tested before and after the 100 cycles were completed. Test sets 2 and 3 were performed using a Sigma Systems M18-C4 Temperature Chamber capable of cycling between -180°C and +150°C. Assemblies were electrically tested at 25 cycle intervals over the course of the temperature cycling.

Table I . Temperature Cycle Testing Sequence

Set #	Test Condition	# of Cycles
1	-65°C to + 150°C MIL-STD-883, Method 1010, Condition C	100
2	-120°C to +115°C (<i>Mars Environment</i>), 5°C/min. ramp up/down Dwell: 10 min. at -120°C, 45 min. at +115°C	100
3	-180°C to +85°C (<i>Deep Space Environment</i>), 5°C/min. ramp up/down Dwell: 10 min. at -180°C, 45 min. at +85°C	250

2.1.3 Electrical Testing

Electrical testing was performed using an automatic FET Test system Model 9400. The system was programmed to measure all the electrical parameters of each device specified in Table II and using the test conditions outlined in the device specifications. The specifications were taken from the data sheets for the IRF6635V1 and IRF6644 devices. Note that specifications for IRF6635V1 and IRF6635V2 are identical.

2.1.3.1 Electrical Test Data Analysis

The shift in all the measured parameters was calculated relative to the initial measurements on these same devices prior to temperature cycling. A mean percent delta and standard deviation for each device parameter of device type was computed. Likewise, a mean percent delta and standard deviation were computed for the control samples and were subtracted from those of the test samples. This operation was performed to correct for FET Test instrument drift and the percent deltas were said to be “corrected”. This insured that the instrument drift or fluctuations are stripped from the data leaving only the “real” change in the R_{dsOn} .

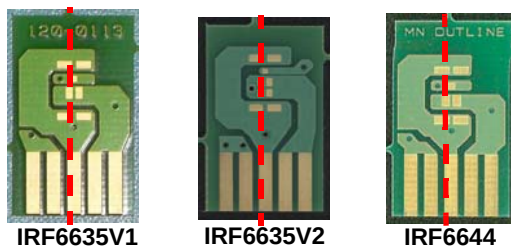
Table II . Device Electrical Parameters Specifications

Parameter	Description	IRF6635	IRF6644
Max. RdsOn (mOhm)	Static Drain-to-Source Resistance	1.8 (Vgs = 10V; Id = 32A)	13 (Vgs = 10V; Id = 10.3A)
Max. Idss (nA)	Drain-to-Source Leakage Current	1,000 (Vds = 24V; Vgs = 0V)	20,000 (Vds = 100V; Vgs = 0V)
Max. Vgs(th) (Volt)	Gate Threshold Voltage	2.35 (Vds = Vgs; Id = 250μA)	4.8 (Vds = Vgs; Id = 150μA)
Min. BVdss (Volt)	Drain-to-Source Breakdown Voltage	100 (Vgs = 0V; Id = 250μA)	100 (Vgs = 0V; Id = 250μA)
Max. Igss1 (nA)	Gate-to-Source Forward Leakage	100 (Vgs = 20V)	100 (Vgs = 20V)
Max. Igss2 (nA)	Gate-to-Source Reverse Leakage	-100 (Vgs = -20V)	-100 (Vgs = -20V)
Max. Vdsp (Volt)	Body Diode Forward Voltage	-1.0 (Is = 25A; Vgs = 0V)	-1.3 (Is = 6.2A; Vgs = 0V)

The control units were always electrically tested at the same time as the test assemblies. In this way, it was possible to determine whether a shift in measured parameter values of the test assemblies was real or simply due to drift in the FET Tester. This instrument drift

2.1.4 Cross-Sectional and SEM Analysis

At the completion of all the temperature cycling, a set of assemblies was sent for cross-sectional and SEM analysis to Photometrics (Huntington Beach, CA). A selection of assemblies, representing the three types of devices and solder alloys from the three sequences of temperature cycling analyzed. The parts were cross-sectioned along the cut line indicated by Figure 5 to inspect the drain and source solder joints. The parts were etched and polished and then inspected under a SEM and high power optical microscope.

**Figure 5 . Assembly Cross-Section: Cut Locations**

2.2 Results and Discussion

2.2.1 Electrical Test Results: Yield Analysis

Figure 6 plots the percent yield of all the device types versus the number temperature cycles. All devices survived the initial temperature cycling (-65°C to +150°C). Most devices survived the first set of extreme temperature cycles (-120°C to +115°C) with the exception of the IRF6635V1 Pb-Sn, which saw one Igss (reverse gate-to-source leakage) failure. This may be due to device damage. Significant fallout began to occur after 100 cycles of -180°C to +85°C and accelerated thereafter.

The majority of electrical failures could be largely split into two categories: complete failures and internal device failures. Internal device failures were characterized by passing static on resistances (RdsOn) yet with high leakage currents and threshold voltages and/or low breakdown voltages. The high thermo-mechanical temperature cycle stresses are presumed to have induced these failures internal to the die, possibly near the die surface adjacent to the source and gate pads. The DirectFET® die devices themselves appeared as likely to be damaged by temperature cycling as the solder joints. It is noted that most of these failed devices appeared to retain passing static on resistances even after many subsequent temperature cycles.

Failures, as shown in the next section, all occurred without warning. In all cases, the measured electrical parameters, with the possible exception of the RdsOn, showed no statistically significant shifts in magnitude over the course of the temperature cycling. It was only when a failure occurred that a jump in magnitude occurred. The leakage current, threshold and breakdown voltage parameters are internal to the microchip device and are not as such subject to thermo-mechanical wear which is consistent with this observation.

In general, it appears that the SAC305 standoffs may have enhanced the assembly reliability. The smaller solder volume of the IRF6635V1 solder joints meant there was less solder to absorb the thermo-mechanical stresses leading to a higher failure incidence than other devices. In contrast, the IRF6635V2 devices, irrespective of solder alloy type, saw no electrical failures until nearly 400 cycles. Likewise, the IRF6644 devices did not experience failures until near completion of second sequence of temperature cycles.

The assemblies built using the indium solder alloys exhibited the least number of electrical failures. The lead-tin eutectic assemblies regardless of device type, had a lower yield.

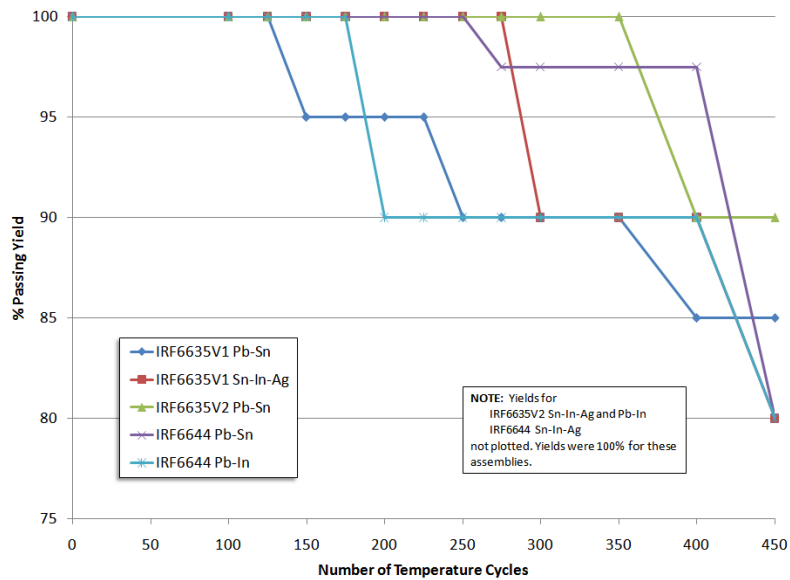


Figure 6 . Electrical Test Yields

2.2.2 Electrical Test Results: RdsOn Analysis

Figures 7 and 8 show the mean percent change (% Delta) in RdsOn parameter for IRF6635 and IRF6644 over the course of all the temperature cycle testing that was performed. The delta is calculated with respect to the initial RdsOn measurement of each assembly. The percent delta is corrected for shifts in the FET Test instrument as discussed in Section 2.1.3.1. Note that data obtained from any of the failed units was omitted from the mean RdsOn calculation and does not show up in these plots.

The general observed trend is of an initial decrease in on-resistance after the initial 100 cycles of -65°C to +150°C resistance followed by a gradual rise in on-resistance throughout the course of the extreme temperature cycling. The cause of the initial drop in resistance is unknown. However, the subsequent rise in resistance was due to the gradual degradation (fatigue) of the solder joints: as the joints fatigue, cracks and voids develop within them that increase solder resistivity. The effect of solder joint fatigue are also apparent in larger scatter in the RdsOn data. The wider distribution of test results could be attributed to the variation in the amount of solder joint degradation.

All the device types, relative to the RdsOn as measured after the initial temperature cycling (Sequence Step 1), experienced comparable net RdsOn shifts of between 1 and 5 percent over the course of extreme temperature cycle testing. Although these are real measurable shifts, they are still

relatively small given the temperature extremes that the assemblies were subjected to. Furthermore, they are small enough that they would probably not even be noticeable in normal applications. For instance, operating the IRF6635 at the test conditions used for measuring RdsOn, the device dissipates about 1.5 Watts and 5 percent shift the equates to only about 7.5 mW. Small variations in drain current would likely have a far more noticeable effect.

2.3 Cross-Sectional Analysis

2.3.1 Lead-Tin Eutectic Soldered Assemblies

The cross-sections of test samples of both versions of IRF6635 and IRF6644 are shown in Figures 9 and 10. All cross-sectioned assemblies were electrically good units that passed all parameter tests.

The drain solder joints in all cases did not show any sign of degradation. However, the source solder joints on nearly all devices, particularly those exposed to the Mars and deep space thermal environments, showed evidence of significant grain coarsening and fatigue cracking. These cracks were all located at or near the interface between the solder joint and the die pad. In the case of IRF6635V1 and IRF6644 assemblies, the cracks even appeared to traverse the entire length of the source solder joint. In contrast, the IRF6635V2 solder joints appear largely intact. There was some evidence of minor fatigue cracking but none which traversed the joint, even after completing 450 temperature cycles.

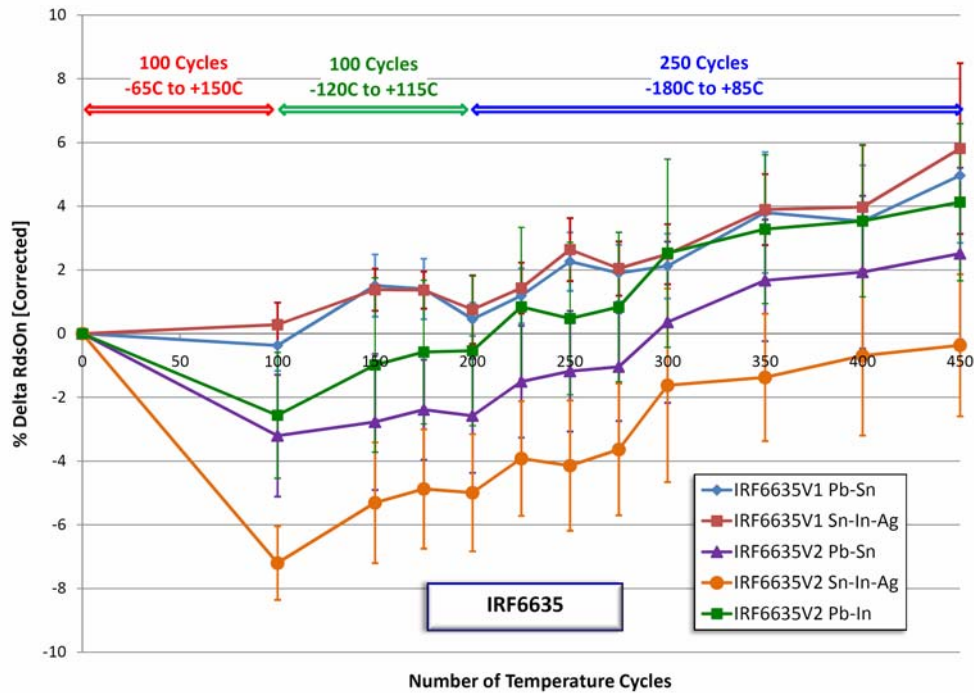


Figure 7 . Temperature Cycle Testing: IRF6635 RdsOn

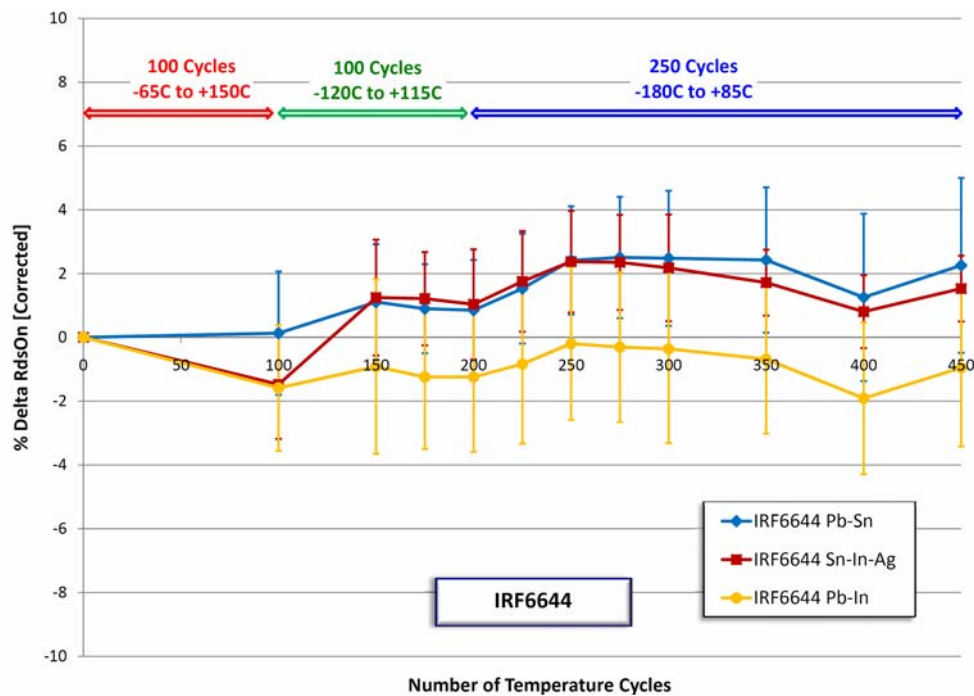


Figure 8 . Temperature Cycle Testing: IRF6644 RdsOn

2.3.1.1 CTE Mismatch and Solder Joint Fatigue

The region where the cracks appeared is also where the stresses and strains are the largest due to the CTE mismatch between the die and PWB. A typical FR4 laminate will have a CTE of between 12 and 16

ppm/°C whereas silicon has a CTE of only 2.4 ppm/°C. This large mismatch, particularly over the large temperature delta in temperature cycling (265°C in the deep space environment cycling) imposes large CTE stresses at the die to solder interface.

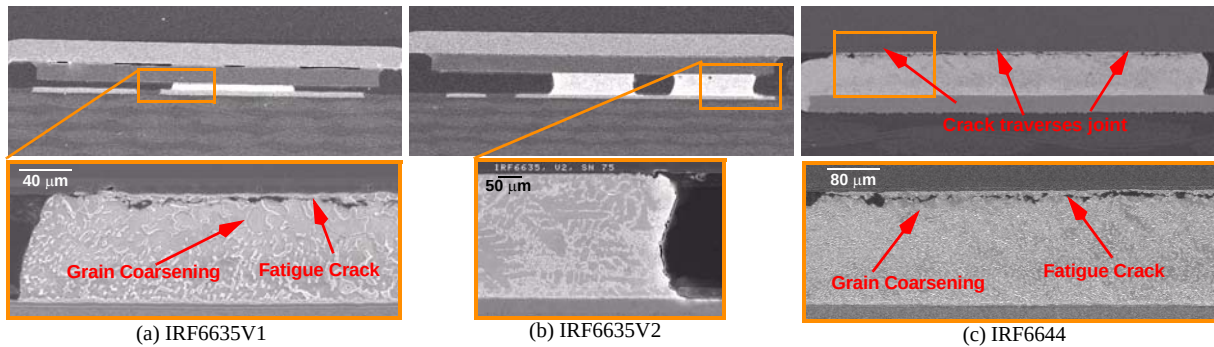


Figure 9 . Cross-Section Analysis: Pb-Sn Assemblies After 100 Cycles, -120°C to +115°C

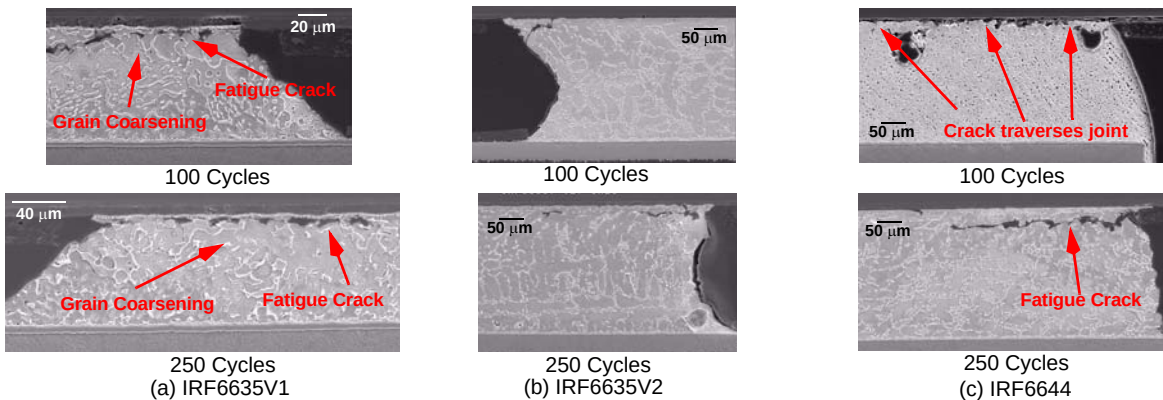


Figure 10 . Cross-Section Analysis: Pb-Sn Assemblies After 100 & 250 Cycles, -180°C to +85°C

The cyclic loading gradually weakened the joint at the interface via grain coarsening and crack initiation. The devices eventually failed once the cracks fully propagated through the joint. This was a particular problem for the IRF6635V1, which had a much smaller solder joint height (0.004 inch) than the other two devices (0.0105 inch).

The absence of cracks in the IRF6635V2 source solder joints may be attributed to the geometry of the solder joint. Both the IRF6644 and IRF6635V2 had the same solder joint thickness and experienced the same stresses at the solder joint to die interface. The IRF6644, in contrast to the IRF6635V2, has a much larger interfacial area and correspondingly larger solder volume per source pad, which should allow it to dissipate stresses over a larger amount of solder. However, the IRF6635V2, with its smaller pads forms joints which are nearly cylindrical columns with concave solder fillets while the IRF6644 forms rectangular columns with minimally concave (even convex in some instances) fillets. It is thought that the shape of the IRF6635V2 solder column coupled with its small interfacial area allows for better dissipation of solder stresses at interfaces. The fillet shape eliminates sharp corners, regions of typically high stress concentrations.

The effects of the solder joint geometry and thickness are evaluated through thermo-mechanical simulations in Section 3.

2.3.1.2 Fatigue Cracks and Electrical Testing

In spite of the presence of cracks in the source solder joint, as noted above, none of the cross-sectioned units failed electrical test or displayed any adverse effect on the measured device parameters. For instance, the IRF6644 device in Figure 9 shows a crack which appears to traverse the entire length of the source solder joint. Yet, the R_{dsOn} measurement for this device (10.4 mOhm) was well within the specification limits and the corrected percent delta R_{dsOn} was not large (+2.6 percent). Significant deterioration of the solder joint had minimal effect on the measured R_{dsOn} .

One concludes, then, that monitoring of DC electrical parameters during environmental testing is a poor indicator of solder joint integrity. These measurements cannot be solely relied upon to determine device or assembly reliability. Destructive physical analysis, high resolution CT X-ray scanning or acoustic microscopy of assemblies randomly must also be performed. Recently, new RF electrical techniques based on tdr measurements have begun

development that may prove to be better predictors [14].

2.3.2 Sn77.2:In20:Ag2.8 Soldered Assemblies

Figure 11 depicts the cross-sections of the assemblies soldered with the Sn77.2:In20:Ag2.8 solder. All cross-sectioned test samples were electrically good units that passed all parameter tests.

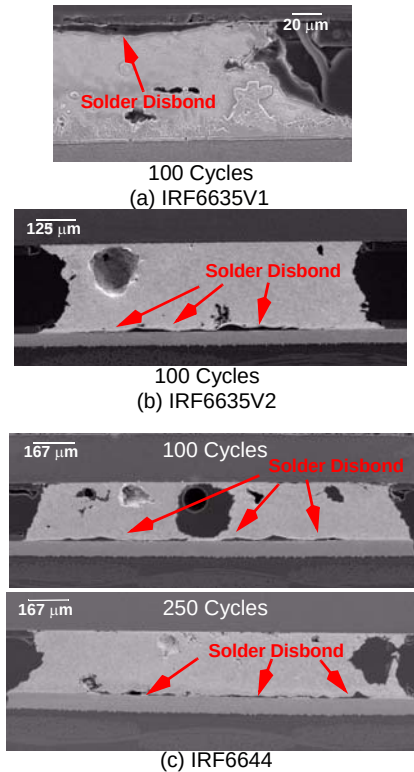


Figure 11 . Cross-Section Analysis: Sn-In-Ag Assemblies After 100 & 250 Cycles, -180°C to +85°C

All samples display a homogeneous solder joint, indicating complete mixing of the SAC305 and the indium alloy. A determination of the actual solder alloy composition of the joints was not attempted on any of the assemblies in this study. Non-destructive analytical techniques of solder joints would not yield reliable quantitative data. The samples all show a distinct interfacial region that was disbonded from either PWB or the die pads. A large gap between the intermetallic layer of the solder and the PWB or die is clearly visible. The solder formed a thick (3 to 4 microns) and very dense intermetallic with the ENIG plating (see). The presence of additional tin from the SAC305 bump may also have contributed to the intermetallic formation. Being as thick and dense as it was, it was inflexible and lifted during temperature

cycling. Cross-section of a control unit that was not temperature cycled showed no disbonds.

The disbonded region did not completely cleave the entire interface of the solder joint, since the parts were still electrically functional. Yet, this partial separation appears to have stress relieved the solder joint, allowing the assemblies to survive hundreds of temperature cycles while still maintaining good electrical interconnection. Despite the fact that these joints were mechanical failures, there was no evidence in the test data of any effect on the device parameters. The R_{dsOn} values were within specification and the percent delta R_{dsOn} was of the same magnitude as compared to the lead-tin eutectic samples. This result underscores the need to evaluate solder joint reliability and integrity by other means than DC electrical testing.

2.3.3 Pb60:In40 Soldered Assemblies

Figure 12 depicts the cross-sections of IRF6635V2 and IRF6644 assemblies soldered with the Pb60:In40 solder. All cross-sectioned test samples again were electrically good units that passed all parameter tests.

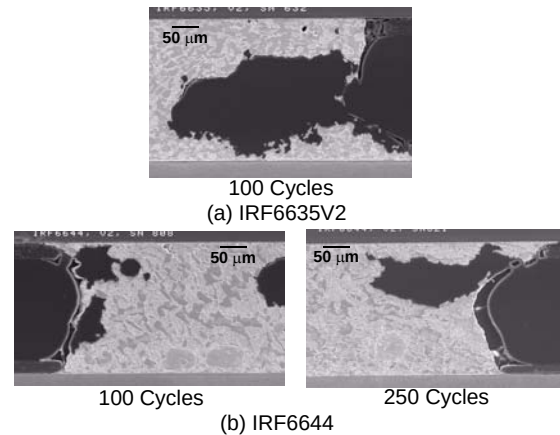


Figure 12 . Cross-Section Analysis: Pb-In Assemblies After 100 & 250 Cycles, -180°C to +85°C

All samples displayed a homogeneous solder joint, indicating complete mixing of the SAC305 and the indium alloy. The alloy composition of the solder joints were again not verified. The samples all showed substantial voiding. The Pb-In assemblies were known to have a high degree of voiding from the outset. However, the voids depicted here do not have a smooth, spherical geometry as might be expected from reflow voids. The outline of the voids is extremely irregular, which suggests that they were deformed and enlarged by solder creep. The extensive creeping of the solder would eventually sever the joint

leading to an RdsOn failure. Several such failures did occur with the IRF6644 assemblies.

3. Thermo-mechanical Stress Simulations

3.1 Model Design

To better understand how the stresses were distributed in the assemblies and how the solder joint geometry affected these distributions, thermo-mechanical stress simulations were performed on several models of the IRF6635 assembly. To simplify the model, the silver epoxy die attach adhesive was omitted and the die was rigidly bonded to the copper lid. The PWB material was assumed to be Nelco 4000 and isotropic. The solder material was taken to be lead-tin eutectic solder. Solder joint heights of 0.004 inch and 0.0105 inches, representing the two extremes of solder joint thickness, were modeled. Two different source and gate pad geometries, representing IRF6635V1 and IRF6635V2, shown in Figure 13 were modelled.

The model was generated in SolidWorks while the thermo-mechanical stress simulations were performed with CosmosWorks Designstar using an FFT Plus Solver. A 0.001inch mesh was used for source and gate solder joints while a 0.004inch mesh was used for all the other portions of the assembly. The zero stress temperature was taken to be 180°C (453K). Stresses were computed assuming the assembly to be in thermal equilibrium at -65°C (218K). Because of concerns over non-linear behavior of material parameters, the thermo-mechanical stresses were not calculated at the lower temperatures of -120°C or -180°C. It was believed that the effects of solder joint geometry would be already apparent at -65°C.

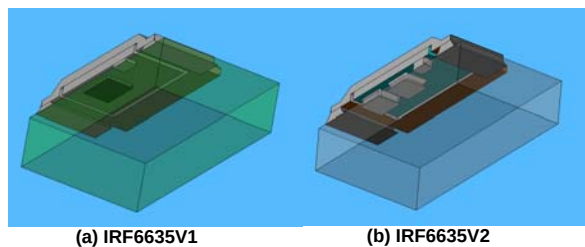


Figure 13 . DirectFET® Assembly Model, Symmetry Cross-Section View (PWB is shown as transparent)

3.2 Simulation Results

Figure 14 show the Von Mises stress over the assembly for the various model configurations. The PWB has been rendered transparent for the sake of clarity. As was anticipated, the areas of highest stress areas were located at the corners of the die and along

the outer edges of source and gate solder joints adjacent to the die interface. The stresses were especially pronounced on the IRF6635 Version 1 assembly with the 0.004 inch solder joint height. The shorter height resulted in greater stress concentrations and steeper stress gradients. The results correlate well with the observed locations of the fatigue cracks in the IRF6635V1 lead-tin solder joints.

The differences between the IRF6635 Version 2 and the IRF6635 Version 1 with the 0.0105 inch solder height were far less significant. The effects of the concave fillets or the smaller interfacial areas were not evident. It is likely that the differences would become more pronounced at the lower temperatures. Further modelling work incorporating low temperature material property data is required.

4. Conclusions

The DirectFET® devices passed temperature cycling through the extreme thermal environments of Mars and deep space with varying degrees of success as measured by DC electrical parameter tests. IRF6635 Version 1 and IRF6644 assemblies soldered with lead tin had the lowest yields. Assemblies soldered with indium regardless of device type or construction appeared to have the highest electrical test yields.

Cross-sectional analysis, however, of assemblies that passed electrical test revealed that their source solder joints had suffered seemingly catastrophic mechanical damage. Lead-tin soldered IRF6635 Version 1 and IRF6644 exhibited substantial grain coarsening and fatigue cracks along the entire length of the solder joints. While the indium soldered assemblies, regardless of device type or device version exhibited large disbonded areas or significant solder creep

The IRF6635 Version 2 assemblies soldered with lead-tin solder had the best electrical test yield and the least evidence of mechanical damage to the solder joints. It is thought that the relatively tall height and relatively small interfacial area of the IRF6635 Version 2 solder joints, enhanced the reliability of these assemblies relative to the other devices. Additionally, the concave shape of the IRF6635 Version 2 solder fillets may have further improved the assembly reliability.

Thermo-mechanical stress analyses of the assemblies demonstrated that the high interfacial stresses were generated near the die to solder interface, the magnitude of which was a function of the source solder joint's height. The effect of the fillet shape or of the solder joint's interfacial area was not confirmed and will require further study.

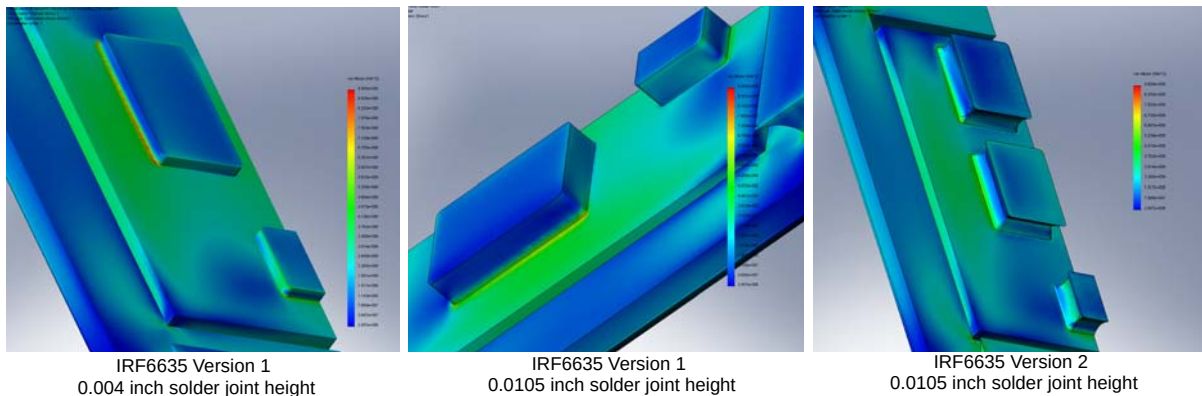


Figure 14 . Simulated Von Mises Stresses: IRF6635 Assemblies at -65°C, Symmetry Cross-Section View

The thermo-mechanical simulation and experimental test results underscore the need for careful selection of assembly materials to minimize CTE stresses. A more judicious choice of PWB materials would improve the reliability of tested assemblies. Additionally, the results of electrical testing and cross-sectional analysis demonstrate the inadequacy of relying solely upon DC electrical testing to determine solder joint integrity and assembly reliability.

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