

Thermosonic Gold Stud Bump Attach for Large ICs on Laminate Substrates

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Abstract

Miniaturization and reliability are the two most critical aspects when designing packaging for an implantable electronic medical device. As sizes of implantable devices shrink, more mature packaging methods such as wire bonding become less feasible due to the additional layout area that is required. A flip chip package that employs gold stud bump interconnects is a proven alternative to both chip/wire assembly and flip chips that rely on wafer-level bump redistribution. Gold stud bumping offers several advantages over wafer-level bumping, such as increased flexibility and cost-effectiveness for prototype and small run environments.

This assembly methodology consists of three primary steps:

- 1) Bumping of the silicon IC using commonly available wire bonding equipment
- 2) Connecting the bumped IC directly to the substrate by thermosonic Au-Au bonding
- 3) Dispensing of an underfill material for environmental protection and mechanical stability

This type of interconnect is common for small devices with low I/O counts, but newer models of flip chip placement equipment are pushing the longstanding limitations of this process. This paper discusses the development and testing of a thermosonic gold stud bump attach process for a large silicon IC (7.5 x 11 mm with 102 I/Os) to an organic laminate PCB.

Objective

This project focused on minimizing the ASIC packaging volume without negatively impacting long-term reliability of the finished device. Specifically, we looked at several ways to improve upon the standard chip-and-wire size limitations for larger ASICs. Current versions of mixed-technology modules implement 25µm diameter gold wire bonding followed by dispense encapsulation or overmolding as a way to integrate bare dice assembly with discrete packaged passive components. As in most microelectronic designs, one of the most critical factors in these types of assemblies is size. Adding wire bonds and protective encapsulants around the ASIC can grow the necessary footprint x-y dimensions by 1.5 mm to 2 mm.

A proven alternative to chip and wire interconnects is flip chip. Many types of flip chip interconnects are used industry wide, with the most popular being wafer level redistribution in the form of solder balls. The drawback to this method is that it can be cost prohibitive, particularly in the initial prototyping and redesign phases. A more flexible method of forming flip chip interconnects uses standard wire bond equipment to stud bump existing perimeter bond pads. Once the pads are bumped, a number of different attach methods are available.

One such stud bump attach method that is commonly used in packaging of small integrated circuit devices and MEMs is thermosonic gold-gold interconnect. This flip chip method is most similar to wire bonding of bare dice, as it relies on thermal energy, force, and ultrasonic scrubbing to create a true gold to gold connection between the substrate and the ASIC.

This direct metal connection creates a stronger, more reliable attach than comparable methods that use epoxies to hold metal interconnects in contact. However, several limitations of the process exist. Applications for this technique are limited to dice with a reasonably spaced bond pad pitch, since this pitch must be mirrored by the substrate trace layout. Also, because the process involves attaching all interconnects simultaneously, it is typically limited to devices with low I/O counts. Increasing the number of interconnects places an additional burden on the assembly equipment and materials, and can lead to diminished effectiveness of the process. The challenging aspect of this project focused on maintaining a robust attach process as device size and I/O count increased.

Design

The test vehicle for this project was designed to replicate a standard large die layout. The design utilized a simple daisy chain die that permitted continuity testing throughout all interconnects in the circuit. The daisy chain test die had final cut dimensions of 7.5 x 11.1 x 0.25 mm with 102 perimeter bondpads integrated into the finished circuit. Bond pad size was 100µm on a 200µm pitch, and aluminum was used for the surface metallization. It is important for the flip chip process that bondpads are evenly placed around the perimeter of the ASIC – if any section of the device is devoid of stud bump interconnects, force may be disproportionately distributed, resulting in uneven bump deformation.

The substrate consisted of a simple 2-layer PCB constructed from a glass-reinforced BT resin core. For the thermosonic gold-gold interconnect process, the choice of PCB core material is important. One key characteristic of the BT material is its high glass transition temperature (Tg) compared to other common PCB materials. The thermosonic bonding process requires a heated work stage for optimal performance, and the higher Tg allows a greater base temperature to be used without degradation of PCB structure. In addition, the rigidity of the interwoven glass prevents flexing of the substrate after attach (which can break the stud bump connections) and provides a solid base that won't excessively dampen the applied ultrasonic power. Other PCB materials such as Mitsui BN300 are available with an even higher Tg, and may provide more process latitude for

difficult stud bump attach applications. Complex multi-layer boards may affect the thermosonic attach process and should be tested for compatibility before implementation.

A high density circuit layout pattern was conceived in order to study the effects of a large metal area on underfill adhesion, moisture sensitivity, warpage, and related process concerns. The PCB construction utilized half-ounce copper traces plated with 0.75 - 1.25 µm of gold over 4.5 - 6.0 µm of nickel. Minimum lines and spaces on the substrate were 100 µm in order to match die bond pad size and pitch. Vias under the die attach area were filled with non-conductive epoxy since there was no need for conductive heat transfer through the package.

Process

One challenge of this project was to work beyond perceived limitations for a thermosonic flip chip attach process. Typical applications for this process are devices that are ~1mm square and have 10-20 bond pad connections. Since this application consisted of a large silicon die with over 100 stud bump connections, we considered a variety of OEMs that offered flip chip equipment with sophisticated capabilities. Panasonic Factory Automation's Advanced Packaging Lab was chosen for their expertise in assembly process development on a variety of equipment including wirebond, stud bump, plasma clean, flip chip, and underfill.

The first step in this development was to create a robust stud bump process that could withstand the aggressive flip chip attach conditions that would be needed for a device of this size. For the bumping material, instead of the typical 99.99% pure gold wire, a 99% gold and 1% palladium alloy was used. This wire composition was selected for its low elongation, which creates minimal tailing during bump formation. An additional coining step was implemented immediately following bump formation in order to create a more consistently flat interconnect surface. To remove impurities from the surface prior to the bonding process, all wafers were plasma cleaned with Argon gas.

The bumping process was assessed primarily by three mechanical attributes: height, diameter, and shear strength. Because of the nominal 100 µm bond pad size, the target diameter for the

stud bumps was 80 μm . This smaller bump size provided for a smash-out of 25% during flip chip attach without expanding beyond the extents of the bond pad and encroaching on the adjacent bump position. Target height for the stud bump formation was 60 μm . After flip chip attach, this height was reduced by approximately 50%. Shear strength was measured on a Dage 4000 multipurpose testing machine. Average gram force for destructive ball shear was greater than 31 grams. After bumping was complete, the wafers were thinned to 250 μm and diced.



Figure 1: Stud bumps on die bondpads after coining.

For the flip chip attach process, the Panasonic FCX501 was recommended, as it is capable of placement force up to 9 kg and is accurate to 10 μm . Due to the relatively low T_g of the organic laminate substrate compared to ceramics (which are commonly used with this type of process), the heated placement head of the FCX501 became an important factor in process development. While the substrate temperature was held stable at 125°C in order to maintain sufficient rigidity, the heated head ramped the die temperature to 250°C prior to placement. A placement force of ~8 kg (0.08 kg per bump) was used to deform the stud bumps to the desired smash height of 25 μm , and ultrasonic power was adjusted as necessary to optimize die shear values. Since force and ultrasonic power settings have a dynamic relationship, a structured design of experiments (DOE) provided the most efficient method to optimize bonding parameters.

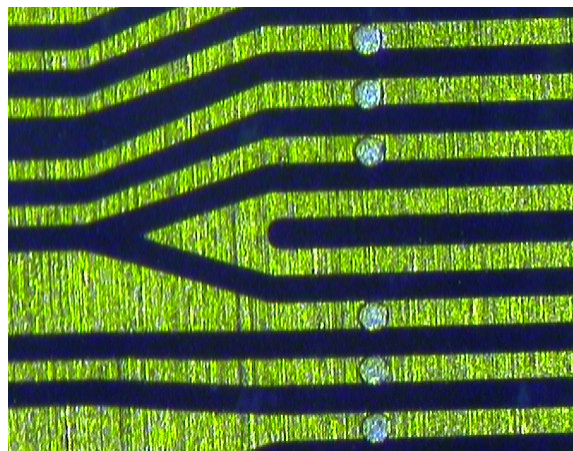


Figure 2: Stud bumps attached to PCB traces after destructive die shear.

Destructive die shear was used as the primary method to evaluate the flip chip attach process. Sample data from flip chip devices using optimized parameters yielded an average shear value of over 2800 gf, or nearly 28 grams per bump. Table 1 below contains sample shear results. Failure mode analysis of the destructively sheared devices showed that all units separated at the die bond pad to stud bump interface, leaving all bumps firmly attached to PCB traces (see Figure 2). This interface was expected to be the weakest point due to the intermetallic nature of the bond between the wire (Au/Pd) and the pad (Al).

Table 1: Sample data after die shear.

Sample	Bump Smash Diameter (μm)	Bump Smash Height (μm)	Die Shear (gf)
1	105	24	2887.3
2	110	23	3298.4
3	110	23	3284.2
4	105	25	2688.5
5	110	24	3035.3
6	110	25	2885.6
7	105	24	2464.2
8	115	24	2429.5
9	112	22	2788.2
10	113	22	2721.3

Other methods that were used to assess flip chip attach include x-ray inspection for placement optimization and cross sectioning for

study of the joint interfaces (see Figure 3). Radiographic inspection found alignment to be acceptable despite a small x-axis offset that was related to PCB design and fabrication. Scanning Electron Microscope (SEM) photo imaging of bump joint cross sections showed good attach at both interfaces (Figure 3).

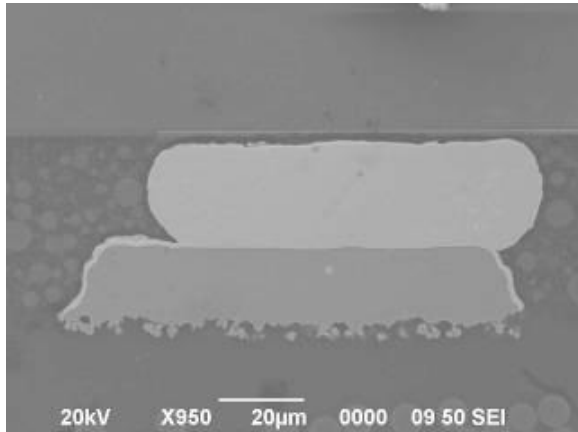


Figure 3: SEM photo of a stud bump cross section after underfill.

After flip chip die attach was complete, devices were underfilled for increased mechanical support and environmental protection. Prior to underfill, the thin BT substrates were handled carefully to prevent flexing, which can stress and potentially sever bump connections. An automated underfill process was accomplished using a single edge dispense pattern and a small particulate material underfill for stud bump applications. The underfill process was evaluated visually for filleting. Additionally, a Scanning Acoustic Microscope was used to ensure that the underfill layer was free of voiding (Figure 4).

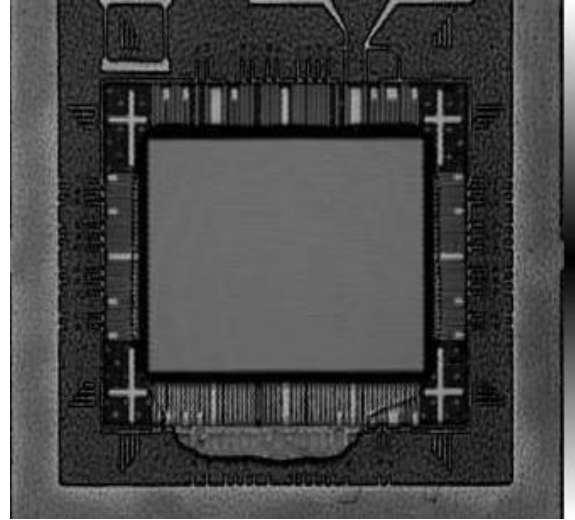


Figure 4: Scanning Acoustic Microscope image showing void-free underfill layer.

Conclusion

Stud bump flip chip packaging holds advantages over traditional wire bonding methods in several significant ways – offering a reduction in electrical resistance along interconnect paths while achieving a packaged footprint that doesn't extend beyond the edge of the die. Stud bump methods create the potential to transfer flip chip technology out of the wafer fab and into the back end semiconductor assembly process. By using common equipment such as advanced wire bonders & liquid dispensers, the stud bump flip chip attach process can make new packaging faster to develop and more flexible for design revisions. Thanks to the expanding capabilities of current flip chip equipment offerings, the gold-gold interconnect process can now be applied to larger, more complex devices without diminishing expected results.

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