

## Formation of Through-Silicon-Vias using Sn Filling Process for 3D Packaging

Sung-Kyu Kim, Kyung-Won Park, Min-Young Kim, and Tae-Sung Oh\*

Department of Materials Science and Engineering, Hongik University  
72-1 Sangsu-dong, Mapo-gu, Seoul 121-791, Korea

\*phone: 82-2-320-1655, Fax: 82-2-333-0127, email: ohts@hongik.ac.kr

### Abstract

*Through-silicon-vias were formed with Sn filling process and their characteristics were evaluated to form three-dimensional-interconnection structure of chip stack packages. Contrary to the conventional Cu vias which require complicate and long Cu electroplating, Sn vias could be formed easily by Sn electroplating and reflow. Sn via-filling behavior did not depend on the shape of the Sn electroplated layer, allowing much wider process window for Sn via formation compared to the conventional Cu via process. Interlocking-joint structure was formed by inserting Cu bumps of 20  $\mu\text{m}$  diameter into Sn vias of 50  $\mu\text{m}$  diameter at 250  $^{\circ}\text{C}$  for 2 min. Melt-joint structure was formed by reflowing Sn bumps of 55  $\mu\text{m}$  diameter on Sn vias of 50  $\mu\text{m}$  diameter at 250  $^{\circ}\text{C}$  for 2 min. Both interlocking-joint structure and melt-joint structure exhibited high chip-shear-forces of 50 N and 30 ~40N, respectively. Comparing microstructures of the interlocking-joint structure and the melt-joint structure with the conventional planar Cu via/bump interface, it is expected that much higher mechanical reliability can be obtained for the interlocking-joint structure and the melt-joint structure formed on Sn vias.*

Keywords: chip stack packages, through-silicon-via, Sn via, electrodeposition, interlocking-joint, melt-joint

### 1. Introduction

With rapid progress of the size reduction and the performance improvement of portable electronic products such as cellular phones, PDA, and digital cameras, three dimensional (3D) stack packages where IC chips are stacked together have been extensively investigated in recent years [1-8]. 3D stack packages, starting their development for fabrication of a memory package by stacking a flash memory and a SDRAM for cellular phone application, have various advantages such as improvement in electrical performance, increase in device functions per unit area of the circuit board, and cost reduction as well as size and weight reduction [9].

In conventional 3D packages, wire bonding has been used to interconnect I/O pads of stacked IC chips to the circuit board. However, such interconnection method using wire bonding is not appropriate for high speed signal propagation between chips, and causes several disadvantages such as limitation to the size reduction and deterioration of the high frequency characteristics [1,8]. As a new interconnection technology for 3D stack packages, chip-to-chip vertical interconnection

technology where through-silicon-vias (TSV) filled with Cu are formed in IC chips has been proposed [5-11]. TSVs can provide shorter interconnection than wire bonding, which can reduce RC delay and power consumption of chip stack packages [5-11].

However, chip stack process using Cu TSVs has various problems. It is easy to form voids inside Cu-vias during electroplating process. A complicate and long electrodeposition process is required to prevent void formation in Cu-vias [5]. Another disadvantage of the chip stack process using Cu-vias is easy failure of the bump/via interface.

To overcome such disadvantages of the Cu-via process, we investigated a new chip stack technology utilizing Sn-via and its bumping structures. Fig. 1 shows the schematic illustration for Sn-via process. First, via holes are formed in a Si wafer by deep RIE. After formation of a  $\text{SiO}_2$  insulation layer, a seedlayer for Sn electroplating is sputtered-deposited. Then Sn is electroplated into the via-holes and reflowed to fill the via-holes. After CMP and back-side grinding of the Si specimen with Sn-vias, Cu bumps are electroplated underneath the Sn-vias and inserted into the Sn vias to form interlocking-bump-joint structure, as shown in Fig. 1(f). To make melt-joint structure, as shown in Fig. 1(h), solder bumps

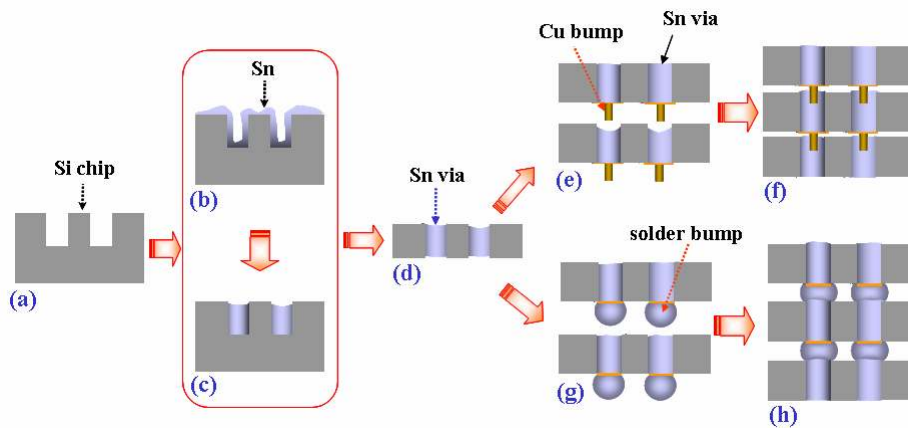


Fig. 1 Schematic illustrations for the Sn-via process: (a) via-hole formation, (b) Sn electroplating, (c) Sn reflow, (d) CMP and back-side grinding, (e) Cu interlocking bump formation, (f) chip stack with interlocking-bump joints, (g) solder bump formation, and (h) chip stack with melt-joint structure.

are formed underneath the Sn-vias by electroplating and chip stacking is accomplished by reflowing the solder bumps. Compared to the conventional Cu-via process, there are several advantages for the Sn-via process; Firstly, it is easy to form Sn vias using Sn electrodeposition and reflow, as it is unnecessary to fill via-holes completely with Sn electrodeposition. Secondly, process time for via formation will be shortened, because of Sn electrodeposition rate faster than that of Cu electroplating. Thirdly, CMP (chemical and mechanical polishing) would be easier as Sn is softer than Cu. Finally, good mechanical stability can be obtained with the interlocking-joint structure and melt-joint structure.

## 2. Experimental Procedure

To observe the Sn-via-formation behavior, we used via-hole specimens of  $50\mu\text{m}$  or  $100\mu\text{m}$  diameter,  $150\mu\text{m}$  depth, and  $150\mu\text{m}$  pitch. Fig. 2 shows the design and SEM micrograph of a via-hole specimen. Via-holes were formed on  $550\mu\text{m}$ -thick Si wafer by using Deep RIE(Reactive Ion Etching).  $\text{SiO}_2$  layer of  $0.1\mu\text{m}$  thickness was formed on the surface of the Si

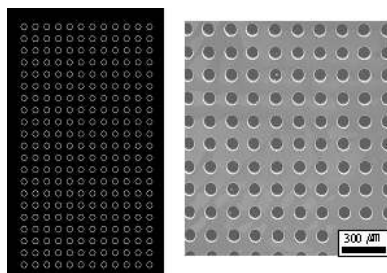


Fig. 2 Design and SEM micrograph of the via-hole pattern of  $50\mu\text{m}$ -diameter and  $150\mu\text{m}$ -pitch.

wafer and via-holes as an insulation layer by using dry oxidation method. As a seed layer for Sn electrodeposition,  $0.1\mu\text{m}$ -thick Ti and  $2\mu\text{m}$ -thick Cu were sequentially sputter-deposited on the surface of the via-holes.

Commercial Sn electroplating solution was used to form the Sn layer into the via-holes. Si wafer was dipped into 10 vol%  $\text{H}_2\text{SO}_4$  for 5~10 seconds just before Sn electroplating to remove the oxidation layer on the surface of the Ti/Cu seed layer. Before Sn electroplating, the Si wafer with via-holes was kept in the electroplating solution under a vacuum of  $1 \times 10^{-2}$  torr for 30 minutes to remove the air inside the via-holes. Sn electroplating into the via-holes was conducted by applying a direct current with a current density of  $2.5 \sim 20 \text{ mA/cm}^2$ . Electroplating time was varied to keep the thickness of the Sn layer electroplated at each current density approximately same. The electroplated Sn layer was reflowed at  $250^\circ\text{C}$  for 1 min to form the Sn-vias. During Sn reflow, we scribed the chip surface with a blade to remove excess Sn from the chip surface.

Cu bumps of  $20\mu\text{m}$ -diameter and  $50\mu\text{m}$ -length were electroplated on a Si wafer. Sn bumps of  $55\mu\text{m}$ -diameter were formed on a Si wafer by electroplating and reflow. The Cu bumps were aligned and inserted into the Sn-vias at  $250^\circ\text{C}$  for 2 min to form the interlocking-joint structure. The Sn bumps were also aligned on the Sn-vias and reflowed at  $250^\circ\text{C}$  for 2 min to form the melt-joint structure. Scanning electron microscopy (SEM) was used to observe the Sn electroplated layer and the Sn-vias formed by reflow process after electroplating.

## 3. Results and Discussion

Fig. 3 illustrates the Sn layer electroplated into

the via-holes at current densities ranging from 2.5 mA/cm<sup>2</sup> to 20 mA/cm<sup>2</sup>. Electroplating time was changed from 11 hr to 1 hr to have approximately same thickness of the electroplated Sn layer at each electroplating condition. Thickness variation of the electroplated Sn layer was observed between the opening and the bottom of the via-hole due to higher plating rate with faster charge and mass transfer near the via mouth than the via-bottom [12]. With increasing the electroplating current density, such thickness variation became larger due to the enhanced current crowding at the via-opening and more significant mass transport limitations towards the bottom of a via [12].

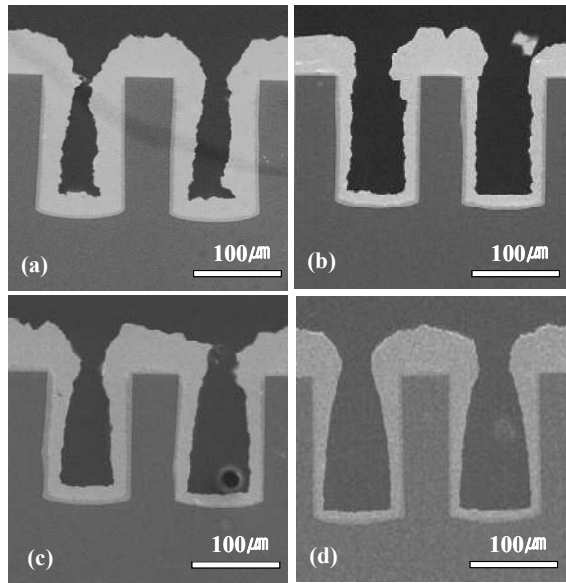


Fig. 3 SEM micrographs of the via holes of 100-μm-diameter electroplated at (a) 2.5mA/cm<sup>2</sup> for 11 hr, (b) 5mA/cm<sup>2</sup> for 4 hr, (c) 10mA/cm<sup>2</sup> for 2 hr, (d) 20mA/cm<sup>2</sup> for 1 hr.

Fig. 4 shows SEM micrographs of the Sn-vias formed by reflowing the electroplated Sn at 250°C for 1 min. Without depending on the shape and the thickness of the electroplated Sn layers shown in Fig. 3, the via-holes were completely filled with Sn to form Sn-vias. Although the volume of the Sn layer electroplated inside a via-hole was not enough to fill the via-hole completely, we could obtain completely filled Sn-vias. That is because the Sn electroplated on the chip surface melted and flew into the via-hole during reflow process by scribing the chip surface with a blade.

As shown in Fig. 5, Cu bumps of 20-μm-diameter and 50-μm-length were electroplated on a Si wafer in order to form interlocking-joint structures by using the Sn-vias. Such Cu interlocking bumps were inserted into Sn-vias to form the interlocking-joint structures by bonding at 250°C for 2 min. The bonding force was changed in a range of 1 ~ 7 N.

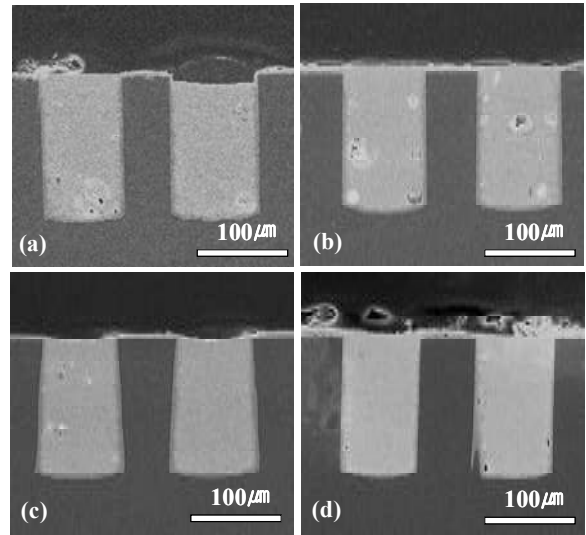


Fig. 4 SEM micrographs of the Sn-vias of 100-μm-diameter formed by reflowing the Sn electroplated at (a) 2.5mA/cm<sup>2</sup> for 11 hr, (b) 5mA/cm<sup>2</sup> for 4 hr, (c) 10mA/cm<sup>2</sup> for 2 hr, (d) 20mA/cm<sup>2</sup> for 1 hr.

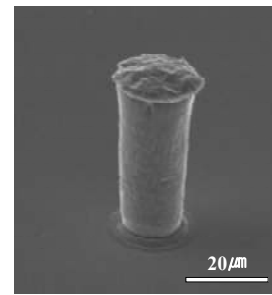


Fig. 5 SEM micrograph of a Cu bump.

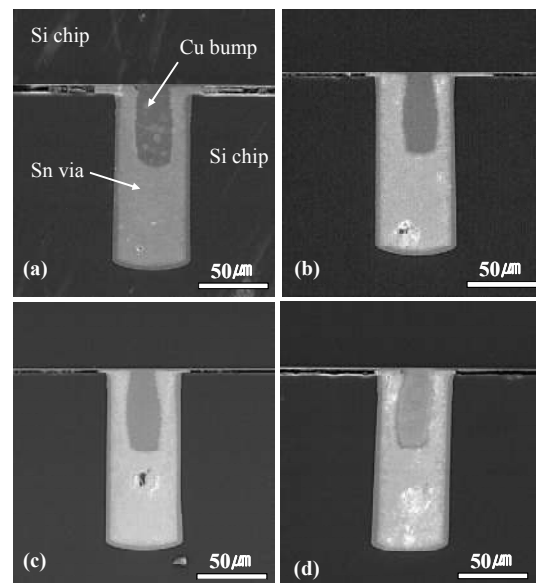


Fig. 6 SEM micrographs of the interlocking-joint structures bonded with bonding forces of (a) 1 N, (b) 3 N, (c) 5 N, and (d) 7 N.

Fig. 6 shows SEM micrographs of the interlocking-joint structures bonded at each bonding force. Cu bumps were well inserted into the Sn-vias regardless of the bonding force. Although we fabricated the interlocking-joint structure at 250°C, it is also possible to process it at a temperature below but near 221°C, the melting temperature of Sn. As plastic deformation of Sn can occur easily at such a temperature, Cu bump will be easily inserted into Sn-via.

Fig. 7 illustrates the chip shear force of the interlocking-joint structure as a function of the bonding force. Except one bonded at 5 N, all other interlocking-joint structures exhibited bonding forces around 50 N. Fracture surfaces of the interlocking-joint structures after chip shear tests were observed in Fig. 8. Cu bump inserted into the Sn-vias were broken during chip shear tests regardless of the bonding forces ranging from 1 N to 7 N. A maximum force required to break the stacked specimens was the same as the force needed to fracture an inserted Cu bump. As the Cu interlocking bumps were broken during chip shear test regardless of the bonding force, the chip shear force of the interlocking-joint structure

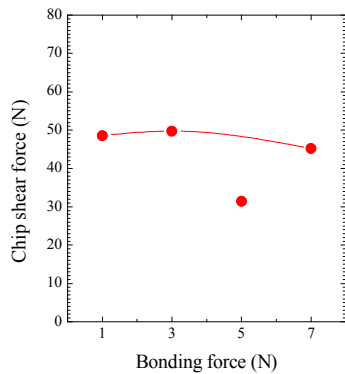


Fig. 7 Chip shear force of the interlocking-joint structure as a function of the bonding force.

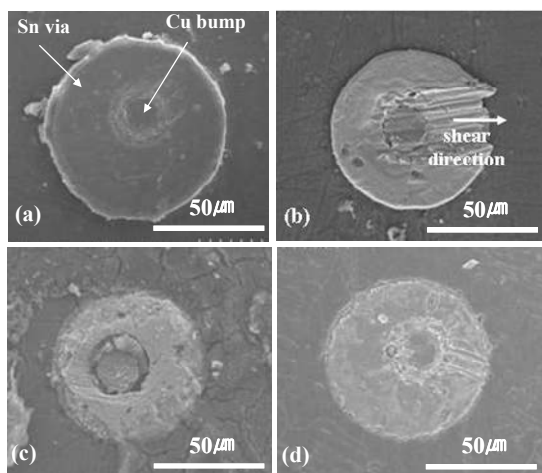


Fig. 8 SEM micrographs of fractures surfaces of the interlocking-joint structures formed with a bonding force of (a) 1 N, (b) 3 N, (c) 5 N, (d) 7 N.

was not dependent upon the bonding force (Fig. 7).

Fig. 9 shows SEM micrographs of the melt-joint structures where Sn bumps were joined to the Sn-vias of 50-μm-diameter by reflowing at 250°C for 2 min with a bonding force ranging from 1 N to 7 N. As the interfacial delamination between a via and a bump is eliminated in this joint structure, high mechanical reliability can be expected. As shown in Fig. 10, chip shear forces in the range of 30 N to 40 N were obtained for the melt-joint structures.

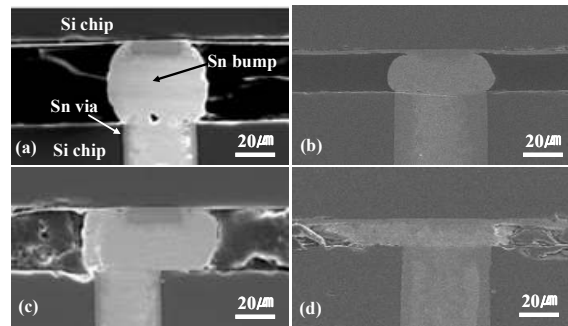


Fig. 9 SEM micrographs of the melt-joint structures bonded by reflowing at 250°C for 2 min with a bonding force of (a) 1 N, (b) 3 N, (c) 5 N, and (d) 7 N.

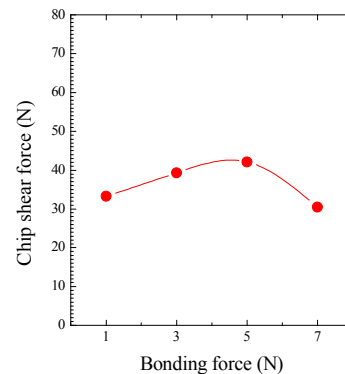


Fig. 10 Chip shear force of the melt-joint structure as a function of the bonding force.

#### 4. Conclusion

To solve disadvantages of the Cu-TSV process, we investigated a new chip stack process utilizing Sn-via and its bumping structures. Contrary to the conventional Cu-via process where long and complicate electrodeposition is required, easy Sn-via formation could be achieved with Sn electrodeposition and reflow. Sn-via filling behavior with reflow was not sensitive to the shape and the thickness of the electrodeposited Sn layer, allowing much wider process window for Sn via formation compared to the conventional Cu via process. Cu bumps were inserted into Sn-vias to form interlocking-joint structures. Chip shear forces of about 50 N were obtained for the interlocking-joint

structures. Melt-joint structure was formed by reflowing Sn bumps with Sn-vias. Chip shear forces ranging from 42 N to 31 N were measured for the melt-joint structures.

#### Acknowledgement

This work was supported by the Center for Electronic Packaging Materials (ERC) of KOSEF.

#### References

- [1] S. F. Al-Sarawi, D. Abbott, and P. D. Franzon, IEEE Trans. Comp. Packag. Manufact. Technol. B, 21(1988) 2.
- [2] M. Hirano, K. Nishikawa, I. Toyoda, S. Aoyama, S. Suiting, and K. Yamasaki, Solid-State Electron., 41 (1997) 1451.
- [3] K. Takahashi, T. Hiroshi, T. Yoshihiro, Y. Yasuhiro, H. Mistake, S. Tomatoes, M. Adair, S. Masahiro and B. Manabu, Jon. J. Apple. Phys., 40 (2001) 3032.
- [4] K. Hara, Y. Eurasia, N. Hashimoto, K. Matsui, Y. Macao, I. Miyazawa, T. Kobayashi, Y. Yokoyama, and M. Fukazawa, IEEE Trans. Adv. Packag., 28 (2005) 357
- [5] K. Kondo, T. Yonezawa, D. Mikami, T. Okubo, Y. Taguchi, K. Takahashi, and D. Barkey, J. Electrochem. Soc., 152 (2005) H173.
- [6] M. Karnezos, F. Carson and R. Pendse, Chip Scale Review (2005).
- [7] K. W. Lee, T. S. Oh, J. H. Lee, T. S. Oh, J. Electron. Mater., 36 (2007) 123.
- [8] C. H. Ryu, J. W. Park, J. S. Park, K. Y. Lee, T. S. Oh, J. H. Kim, IEEE Trans. MWCL, 17 (2007) 855.
- [9] K. Tanida, M. Umemoto, and K. Takahashi, J. Electron. Packag., 8 (2005) 308.
- [10] K. Takahashi, Y. Taguchi, M. Tomisaka, and H. Yonemura, Proc. ECTC, (2004) p.601.
- [11] C. H. Seah, S. Mridha, and L. H. Chan, J. Mater. Process. Technol., 114 (2001) 233.
- [12] B. Kim, C. Sharbono, T. Ritzdorf, and D. Schmauch, Proc. ECTC, (2006) p.838.