

Fabrication and Electrical Performance of Z-axis Interconnections: An Application of Nano-Micro-Filled Conducting Adhesives

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Abstract

This paper discusses epoxy-based electrically conductive adhesives (ECAs) for Z-axis interconnections and their device level fabrication, integration, and electrical performances. In particular, we highlight our current effort on ECAs prepared by incorporating nanoparticles, conducting polymers, low melting point alloys (LMP) etc. SEM and optical microscopy were used to investigate the micro-structure and sintering mechanisms. Volume resistivity of modified adhesives is in the range of 10^{-4} to 10^{-6} ohm-cm. Adhesives formulated with a conducting polymer exhibited tensile strength with Gould's JTC-treated Cu ≥ 3800 PSI, and as low as 1800 PSI for a conducting polymer-LMP based system. A few optimized metal-epoxy adhesives were used for hole fill applications to fabricate Z-axis interconnections in laminates. Conductive joints were formed during composite lamination using the ECA. Around 5,000 to 200,000 through holes in the joining cores, formed by laser or mechanical drilling, and having diameters ranging from 50 μm to 250 μm , were filled with an optimized conducting adhesive. The adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. As a case study, an example of nano-micro filled conductive adhesives used in a z-axis interconnect construction of a 23 metal layer package with a 300 μm pad pitch is given. Teflon-based Taconic materials TPG30 and TLG30 were used for the dielectric layers. Electrically, S-parameter measurements showed very low loss at multi-gigahertz frequencies. The losses were low enough to support typical SERDES up to 15 Gbps over 30".

1. Introduction

The needs of the semiconductor marketplace continue to drive density into semiconductor packages [1]. The high end of this market appears to be standard Application-Specific Integrated Circuits (ASICs), structured ASICs, and Field-Programmable Gate Arrays (FPGAs). These devices continue to need increasing signal, power, and ground die pads, and a corresponding decrease in pad pitch is required to maintain reasonable die sizes. The combination of these two needs is

pushing complex semiconductor packaging designs. Traditionally, greater wiring densities are achieved by reducing the dimensions of vias, lines, and spaces, increasing the number of wiring layers, and utilizing blind and buried vias. However, each of these approaches possess inherent limitations, for example those related to drilling and plating of high aspect ratio vias, reduced conductance of narrow circuit lines, and increased cost of fabrication related to additional wiring layers. One method of extending wiring density beyond the limits imposed by these approaches is a strategy that allows for metal-to-metal z-axis interconnection of subcomposites during lamination to form a composite structure. Conductive joints can be formed during lamination using an electrically conductive adhesive. As a result, one is able to fabricate structures with vertically-terminated vias of arbitrary depth. Replacement of conventional plated through holes with vertically-terminated vias opens up additional wiring channels on layers above and below the terminated vias and eliminates via stubs which cause reflective signal loss.

During the past few years, there has been increasing interest in using electrically conductive adhesives as interconnecting materials in the electronics industry [2,3]. Conductive adhesives are composites of polymer resin and conductive fillers. Metal-to-metal bonding between conductive fillers provides electrical conductivity [4-7], whereas a polymer resin provides better processability and mechanical robustness [8]. Conductive adhesives usually have excess filler loading that weaken the overall mechanical strength. Therefore, reliability of the conductive joint formed between the conductive adhesive and the metal surface to which it is mated is of prime importance. Conductive adhesives can have broad particle size distributions. Larger particles can be a problem when filling smaller holes (e.g., diameter of 60 μm or less), resulting in voids. Several nano and micro filled adhesives have been reported for advanced packaging applications. For examples, Xiao et al [9] describes epoxy or silicone based conductive adhesives joints and their thermal and mechanical stabilities. Jeong et al [10] reported the curing behaviors, solvent evaporation and shrink on

conductivity of adhesives. They [11] also described conductivity of micro filled adhesives upon addition of nanoparticles. Lee HH [12] reported effect of nano-sized silver particles on the resistivity of micro-sized silver flakes, mixed-sized silver particles filled conductive adhesives. Goh et al [13] mentioned the effect of annealing on the morphologies and conductivities of sub-micrometer sized nickel particles used for electrically conductive adhesive. Inoue et al [14] investigates the variations in electrical properties of a typical isotropic conductive adhesive (ICA) made with an epoxy-based binder that are caused by differences in the curing conditions. Coughlan et al [15] described electrical and mechanical analysis of conductive adhesives where the main properties of joint resistance and adhesive strength were examined before and after different environmental treatments. Fu Y [16] describes cluster effects of nano fillers in conductive adhesives. Sancakter et al. [17] reported pressure-dependent conduction behavior with particles of different sizes, shapes, and types, the effects of external pressure on the filler resistance were measured. Jiang et al [18] reported surface functionalized nano silver-filled conductive adhesives. Li [19] reported self-assembled monolayers (SAMs) protected silver nano-particle-based conductive adhesives. Although several composites are available for the advance of semiconductor technology, the authors believe that there is potential scope for improvement of the existing materials, so that low processing temperature, flexible, reliable, integral processes/ material can be developed for large scale production. Furthermore, several studies are limited to materials property and reliability assessment, not described important integration issues.

In the present study, adhesives formulated using controlled-sized particles, ranging from nanometer scale to micrometer scale, were used to fill small holes having diameters ranging from 50 μm to 250 μm for Z-interconnect applications. For example, holes 50-75 μm diameter are suitable for chip carrier interconnects, whereas 100-250 μm are suitable for board level interconnects. A variety of metals including Cu, Ag and low melting point (LMP) alloys have been used to make the conductive adhesive. Nanoparticles of silver were chosen because of their higher electrical conductivity and chemical stability. Nanoparticles were mixed with microparticles to improve the sintering behavior of the adhesives. Addition of a conducting polymer will increase the overall mechanical strength without compromising electrical conductivity. LMP and LMP-coated particles melt during processing and produce a continuous metallic network. The adhesive was applied onto Cu substrates by printing or coating. This work also deals with adhesion issues between adhesive and the substrates to which they are mated. The work was

extended to the development of a z-axis interconnect construction for a laminate chip carrier and printed wiring board (PWB). The structure employs an electrically conductive medium to interconnect thin cores (subcomposites). The cores are processed in parallel, aligned, and laminated to form a composite. The net effect is a composite laminate having vertical interconnections with small/large diameter holes that can terminate arbitrarily at any layer within the cross section of the package. There is no requirement for PTHs to be formed at the composite level. Some of the technical challenges associated with this z-interconnect technology are addressed. This effort is an integrated approach on three fronts: materials development and characterization, fabrication, and design and electrical characterization at the board level.

2. Experimental Procedure

A variety of silver, copper, and low melting point (LMP)-based nano and micro particles and their dispersion into epoxy resin were investigated in order to achieve uniform mixing in the adhesive. In a typical procedure, epoxy-based conductive adhesives were prepared by mixing appropriate amounts of the conducting filler powders and epoxy resin in an organic solvent. For conductivity measurements, a thin film of this paste was deposited on a substrate and cured at different temperatures ranging from 150 $^{\circ}\text{C}$ to 265 $^{\circ}\text{C}$. For reliability assessments, two paste films were laminated together.

For fabrication of a high-density laminate chip carrier, a 0S/1P joining core such as that described in reference [20] was constructed using a copper power plane, 35 μm thick, sandwiched between layers of a dielectric material composed of silica-filled allylated polyphenylene ether (APPE) polymer. Through holes in the joining cores, formed by laser or mechanical drilling, and having diameters ranging from 50 μm to 250 μm , were filled with an optimized electrically conductive adhesive. The adhesive-filled joining cores were cured and cross sectioned to evaluate hole fill quality.

Adhesives were characterized by SEM and optical microscopy to ascertain particle dispersion and interconnection mechanism. A Keithley micro-ohmmeter was used for electrical characterization. Room temperature (25 $^{\circ}\text{C}$) viscosity was measured using a MELVERN C-VOR Rheometer in oscillation mode using 50 Pa stress at 1 Hz. Heat of reaction of adhesives were studied using a differential scanning calorimeter (DSC). Practical adhesion (90 degree peel test) and tensile strength were measured using an Instron (Model 1122) and MTS tensile tester, respectively.

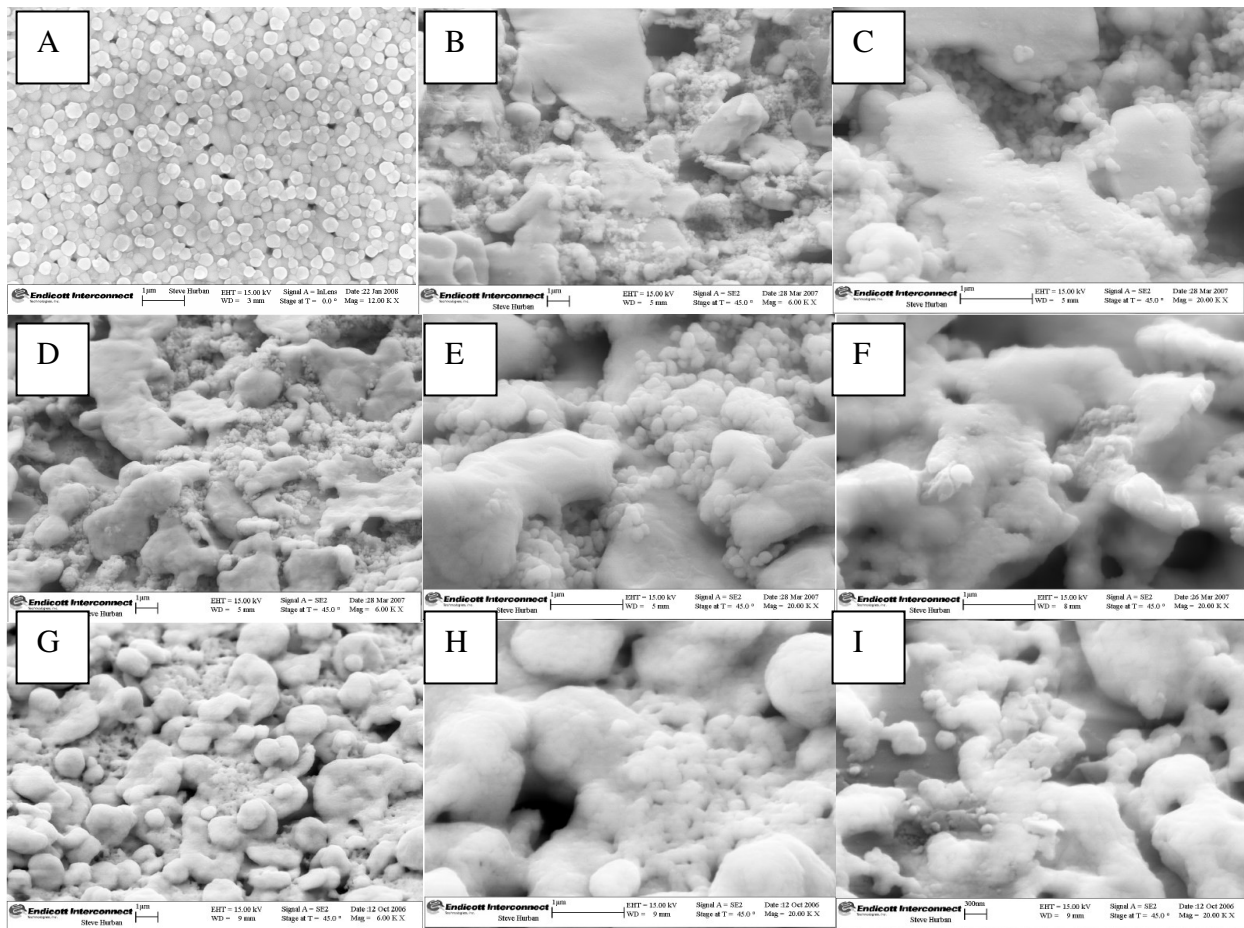


Figure 1: SEM micrographs for the polymer nano and nano-micro-composite filled silver based conducting adhesives; (A) 10-15 nm particle heat treated at 100 °C, (B)-(C) nano-micro composite with 10-15 nm and 5 µm particles sintered at 200 °C, (D)-(E) nano-micro composite with 10-15 nm and 5 µm particles sintered at 225 °C, (F) nano-micro composite with 10-15 nm and 5 µm particles sintered at 240 °C, and (G)-(I) nano-micro composite with 80 nm and 5 µm particles sintered at $(275 \pm 10)^\circ\text{C}$.

3. Results and Discussion

3.1. Nano-Micro filled conductive adhesives

Nanoparticle generally refers to the class of ultra fine metal particles with a physical structure or crystalline form that measures less than 100 nm in size. They can be 3D (block), 2D (plate), 1D (tube or wire) structures. In general, nanoparticle-filled conductive adhesives are defined as containing at least some percentage of nanostructures (1D, 2D, and/or 3D) that enhance the overall electrical conductivity or sintering behavior of the adhesives. It is well known that change in grain size has a direct impact on the electronic properties of a system. In view of this, a systematic investigation of electrical resistance behavior of silver nano and nano-microcomposites has been carried out, and the results of such an investigation are presented here. Sintering temperature can be greatly reduced when

the size of particles is decreased to 5-15 nanometers. Due to the decrease of size, diffusion and growth of the nanoparticles is much easier, and large grains (hundreds/thousand of nanometers) can be produced efficiently. These nanoparticles diffuse with each other and are gradually sintered by neck-formation between the adjacent particles during the thermal anneal process on the substrate. The neck can be smoothed away gradually. The grains of nanoparticles convert into a continuous surface. **Figure 1** shows SEM images of the specimens collected from nano and nano-micro composites with different sintering temperatures, from lower temperature (**Figure 1A-E**) to higher (**Figure 1F-I**). A variety of nanoparticles ranging from 10 nm to 80 nm was used to modify micro adhesive composites. Particle size has a direct impact on particle diffusion/sintering. SEM images indicate that sintering

of a system containing 10-15 nm particles starts at 200 °C (nanoparticles are sintered, some microparticles remain unsintered) and completes at 240 °C (all particles are sintered). For comparison, 80 nm particles have been shown to sinter around 275 °C. In the nano-micro composites, the main components are a mixture of nanoparticles and microparticles. The nanoparticles may contact with the adjacent ones, but the nano aggregation lengths are short, less than 10-fold of the microparticle diameter on average (**Figure 1**). As the sintering temperature increases, particle diffusion becomes more and more obvious. The aggregation length becomes much longer, resulting in the formation of one-dimensional jointed particle assemblies developing into a smooth continuous network (**Figures 1F-I**).

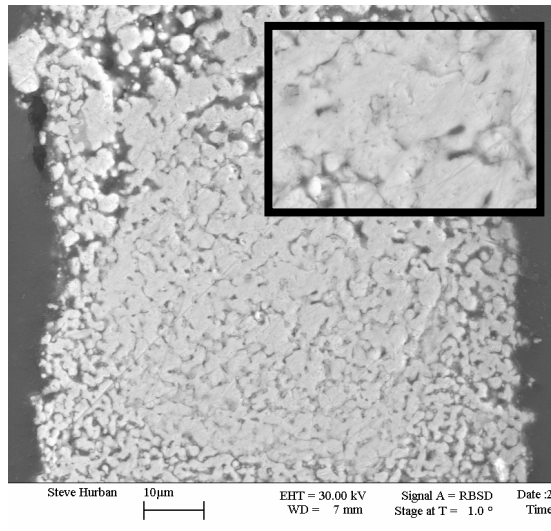


Figure 2: SEM micrograph of sintered adhesive within joining core (Inset at high magnification).

Addition of nanoparticles reduces sintering temperature without compromising electrical conductivity. **Figure 2** show nano-micro composites sintered within micro-via. The observation suggests that the sintering mechanisms are same for the nano-micro composites where micro particles play an important role and the excess amount of microparticle will prevent low temperature diffusion/sintering.

Conducting polymers such as polyaniline are generally doped with protonic acids such as aqueous hydrochloric acid (HCl) to give conductivity on the order of 1 S/cm². Other conducting polymers typically used in organic electronics are poly-3,4-ethylenedioxythiophene doped with polystyrene sulfonic acid PEDOT/PSS, dodecyl benzene sulfonic acid doped polyaniline ~DBSA-PANI and camphor sulfonic acid doped polyaniline, DNNSA-PANI, a

polyaniline doped with dinonyl naphthalene sulfonic acid ~DNNSA. A variety of conducting polymers, blended with appropriate polymers and cured at ~190°C for 2 hours, showed low volume resistivity, in the range of 10⁻⁵ ohm-cm, which is similar to that of micro-filled adhesives. Volume resistivity decreases with increasing curing temperature due to sintering of metal particles. Adhesion between the adhesive and the substrate to which it is mated is critical to the reliability of the semiconductor package. Bond strength of conducting-polymer-modified adhesive joints was evaluated using tensile strength measurements. Tensile strength was measured using an MTS tensile testing machine at a pulling rate of 0.025 inch per minute, and measuring until the joint ruptured. Micro-filled adhesives show high tensile strength with Gould JTC-type Cu foils and show cohesive failure. Conducting polymer doped samples did not show any failure. Here, adhesive (glue) used to attach laminates to test fixtures ruptured prior to the test structures. This indicates conducting polymer modified samples result in highly conducting adhesives having good mechanical strength. Conducting-polymer-based LMP samples showed high mechanical strength. Typically, LMP-based samples show mechanical strength in the range of 600 PSI. Addition of conducting polymer enhances the mechanical strength to 1800-2000 PSI. **Figure 3** shows the tensile strength measurements of conductive adhesives. Conducting polymer silver-filled paste yielded the maximum mechanical strength.

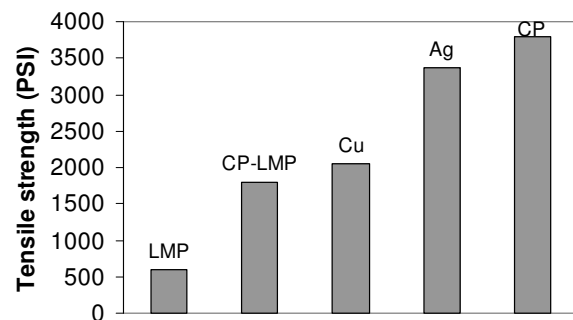


Figure 3: Tensile strength of adhesives (CP: conducting polymer, CP-LMP: Conducting polymer doped liquid melting point (LMP) system, Cu : copper and Ag : silver paste)

Conducting adhesives cured at 200 °C for 2 hours showed low volume resistivity. All silver nano-micro composites showed a resistivity of about 10⁻⁴ to 10⁻⁶ ohm-cm. Resistance decreases with increasing curing temperature due to sintering of metal particles. **Figure 4** shows change of volume resistivity of nano-micro silver paste as a function of curing temperature. There is a significant resistance drop with increasing curing

temperature from 150 °C to 200 °C for nano (80 nm) and nano-micro particles. Change in resistivity with nano-micro system was significant when cured at 200 °C and 275 °C (± 10). Resistivity data indicate that although nano or nano-micro paste sintering starts at lower temperature (100-150 °C for nano and 200 °C for nano-micro), it requires complete sintering to achieve the lowest resistive joints.

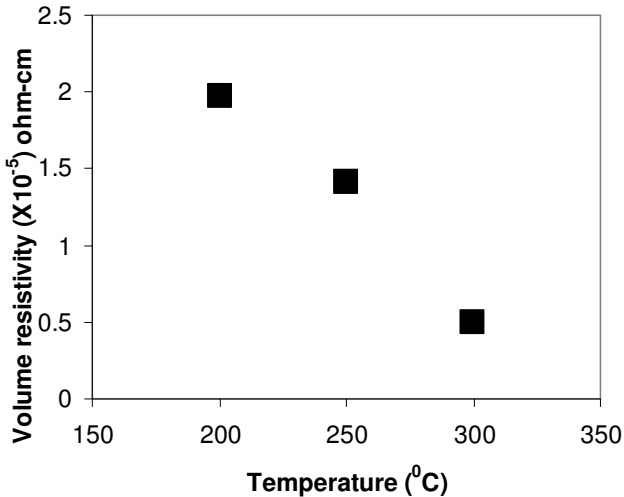


Figure 4: Volume resistivity of nano-micro silver adhesive as a function of curing temperatures

3.2. Core Fabrication

A few optimized metal-epoxy adhesives were used for hole fill applications to fabricate Z-axis interconnections in laminates. Conductive joints were formed during composite lamination using the ECA. Z-axis interconnection was achieved using joining cores, that is, cores with no signal planes, but incorporating a thermoplastic, or uncured thermoset dielectric material for purposes of dielectric to dielectric joining, and ECA-filled vias for purposes of metal-to-metal joining with adjacent signal cores. Around 5,000 to 200,000 through holes in the joining cores, formed by laser or mechanical drilling, and having diameters ranging from 50 μm to 250 μm , were filled with an optimized ECA. The adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. High temperature/pressure lamination was used to cure the adhesive in the composite and provide Z-interconnection among the circuitized subcomposites. A variety of joining core and subcomposite structures such as 0S/1P, 0S/2P, 2S/1P, 2S/2P were used for hole fill applications. The cores can be structured to contain a variety of arrangements of signal, voltage, and ground planes. In addition, signal, voltage, and ground features can reside on the same plane. **Figure 5** shows optical photographs of a joining core (0S/1P) having paste-filled holes.

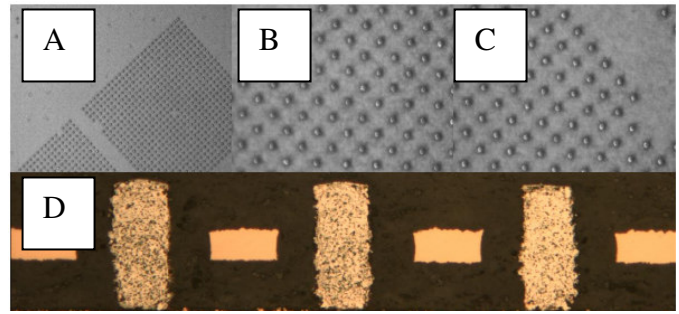
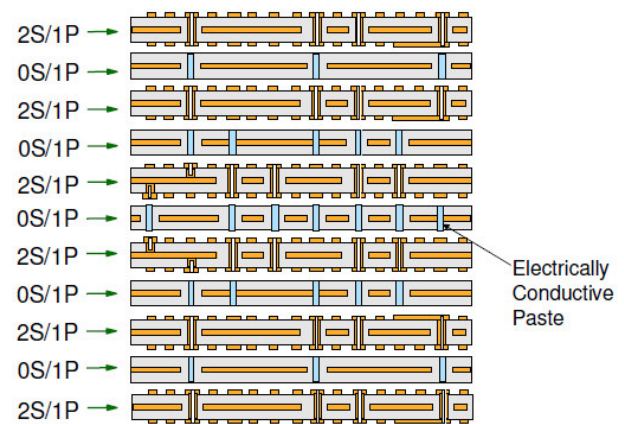


Figure 5: Optical photographs of adhesive filled joining core (A-C) top view, and (D) cross sectional view.

Fabrication of core building blocks.....



...followed by core lamination.

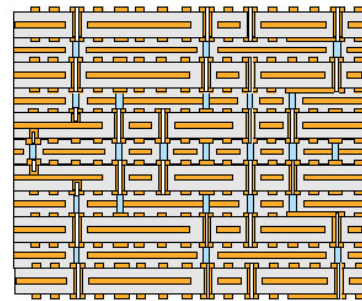


Figure 6: Parallel lamination of subcomposites (cores) to form a printed wiring board having 12 signal wiring planes and a stripline transmission line structure.

3.3. Full-Z Board Fabrication/ case study:

Integral to the methodology described in this paper is the use of core building blocks that can be laminated in a manner such that electrical interconnection between adjacent cores is achieved. As a case study, this micro array based z-interconnection methodology was used to fabricate a package for a board device having a pad pitch of 375 μm . Two basic building blocks are used for

this case study (**Figure 6**). One is a 2S/1P core. The power plane (P), a 35 μm thick copper foil, is sandwiched between two layers of a dielectric. The dielectric is used because of its favorable electrical, mechanical, and thermal properties. The dielectric constant and loss tangent of the dielectric at 10 GHz are 3.0 and 0.0038, respectively.

The signal (S) layers are comprised of copper features generated using a subtractive process. A line thickness of 35 μm was achieved with minimum dimensions for line width and space of 75 μm each. Minimum land-to-line spacing was also 75 μm . Mechanical-drilled through vias had a diameter of 200 μm . The diameter of plated pads around the through vias was 300 μm .

The second building block in this case study is a 0S/1P core, or joining core. This core is constructed using a copper power plane, 35 μm thick, sandwiched between layers of a dielectric material. Through holes in the core are filled with an electrically conductive adhesive. A 23 metal layer structure with twelve signal layers composed of eleven subcomposites (six 2S/1P cores and five 0S/2P cores) is shown in **Figure 6**.

The adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. A photograph of a composite laminate structure is shown in cross section in **Figure 7**. Proper preparation of the subcomposites is crucial to obtaining robust, reliable micro array joining between dielectric layers and between the conductive paste and the opposing copper pad. Sufficient flow of the dielectric materials must be achieved during lamination to allow for complete encapsulation of circuitized features and good dielectric-to-dielectric bonding.

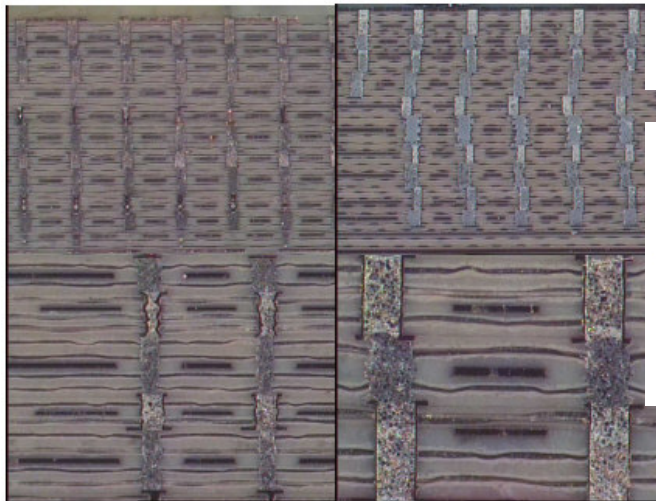


Figure 7: Photographs of z-interconnect laminates shown in cross section.

3.4. Electrical performances:

Electrically, S-parameter measurements showed (**Figure 8**) very low loss at multi-gigahertz frequencies. The measured insertion loss for narrow, short lines and wide, long lines are similar. The Z-interconnect stack-up and low dielectric constant, organic dielectric allowed wide, 50-ohm, lines. The Z-interconnect paste has little effect on the signal, except to add a small via length to the signal. The performance is similar to a solid copper barrel. The Z-interconnect paste does not degrade the signal significantly. We also ran some simulations to generate eye diagrams using raw data measured from the full-Z TV. **Figure 9** shows eye diagrams for Z and non-Z interconnect joints. We considered eye diagram simulation using measured S-parameters from 6 inch length net for four Z-interconnect joints and compared with no Z-interconnect joints. It is clear from eye diagram simulation that z-interconnect does not degrade 10Gbps data.

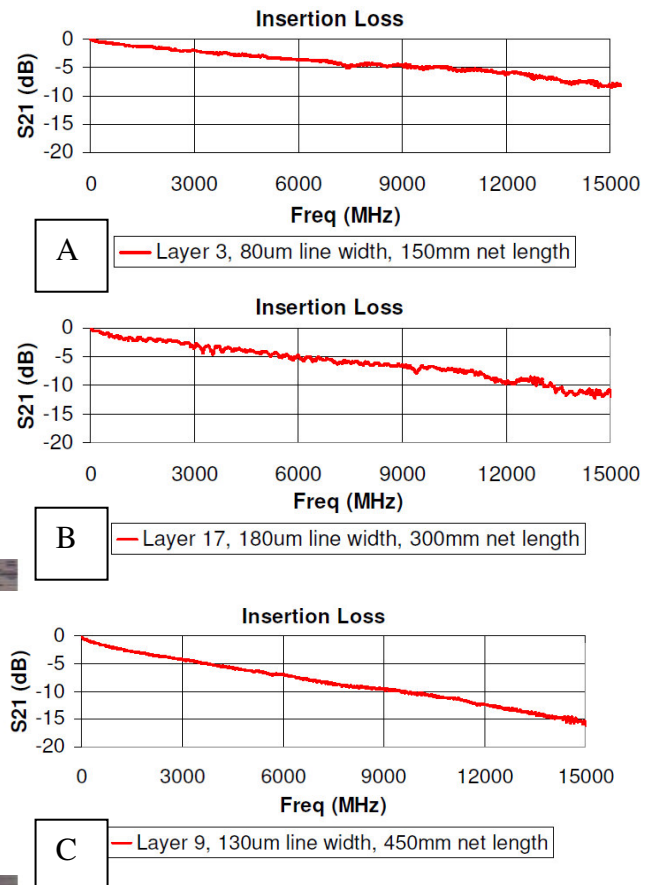


Figure 8: Insertion loss as a function of frequencies (A) narrow line (80 μm), (B) wide Stripline (180 μm), and (C) medium Stripline (130 μm).

Figure 10 is a plot of insertion loss for a net that has no Z-interconnect joints and a net that has 4 joints. Below 10GHz, the difference is negligible, above 10GHz there's a slight degradation due to the additional via length, which is the same as copper plated through-holes. **Figure 11** shows insertion loss of back drilled board and Z board for a given 60 cm net. Z-board shows lower loss at higher frequencies.

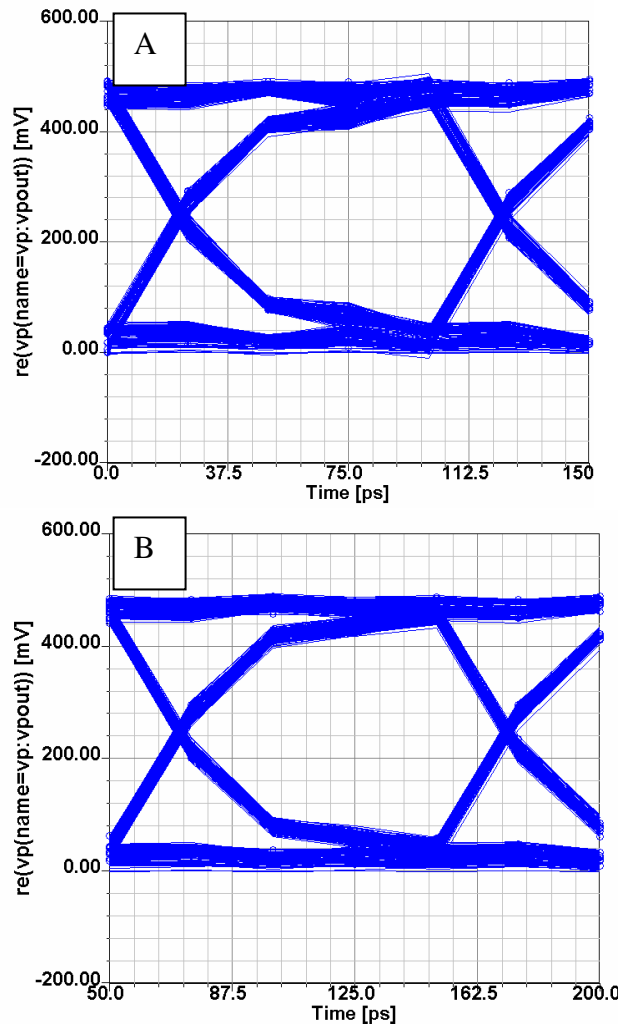


Figure 9: Eye Diagram Simulation using measured S-parameters, 6'' net length (A) non Z-interconnect joints and (B) four Z-interconnect joints.

4. Conclusions

A variety of nano and micro filled Cu, silver and LMP-based conducting adhesives were used for a Z-axis interconnection application. High aspect ratio, small diameter holes anywhere in the range of 50 to 300 microns was successfully filled. Addition of nanoparticles reduces sintering temperatures of micro-filled conducting adhesives. Conducting-polymer-based adhesives were mechanically better than micro- and

LMP-filled adhesives. All adhesives maintained high electrical conductivity and tensile strengths. The adhesive-filled joining cores were laminated with circuitized subcomposites to produce a composite structure. High temperature/pressure lamination was used to cure the adhesive in the composite and provide stable, reliable z-interconnections among the circuitized subcomposites.

A Full-Z interconnect with sub-composites and joining layers can be built. Conductive paste showed good signal transmission to 25GHz. Z-interconnect construction allows wide (7.4 mils) and narrow (3.6mils) lines in the same stack-up. Wide lines (7.4 mils) in organic full Z-interconnect board have signal loss less than 0.6 dB/inch at 10GHz, and less than 1.0 dB/inch at 16GHz. A full-Z taconic board can carry 25Gbps at least 12". Very low-loss multi-GHz, controlled-impedance transmission lines can be built using Z-interconnect with organic dielectric materials.

Z-interconnect can be used in single and multi-chip applications. By designing an organic package without electrical stubs and without through holes, high wiring density and excellent electrical performance can be achieved. Novel means of providing vertical electrical interconnection in organic substrates can help semiconductor packaging keep pace with the needs of the semiconductor marketplace.

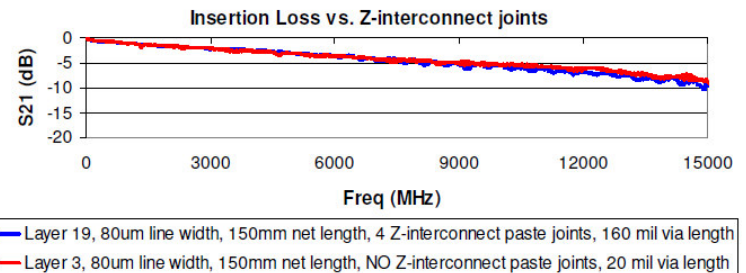


Figure 10: Insertion loss of nets with different numbers of Z-interconnect joints

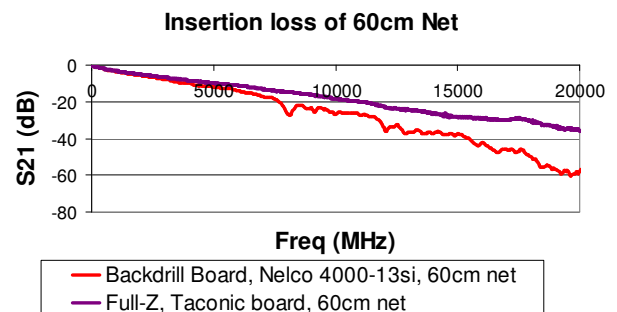


Figure 11 : insertion loss of back drilled board and Z board.

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