

Inter-Wafer Inductors with Magnetic Core for 3D Power Delivery

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Abstract

One method of 3D power delivery architecture was proposed to vertically integrate a cellular array of voltage regulator modules (VRMs) on a thinned wafer with the microprocessor wafer using wafer-to-wafer bonding and through silicon vias (TSVs), with the inter-wafer inductor in between. In this work, an inter-wafer inductor design with magnetic materials is investigated using 3D hyper-integration technology. The inductance and the inductance to winding resistance ratio of inter-wafer inductors are evaluated based on the requirements of a prototype DC-DC converter. A two-leg coupled 3D inductor is designed and simulated using Maxwell 3D electromagnetic simulator to determine its quality factor and inductance to winding resistance ratio. The influence of the inter-wafer inductor inductance to resistance ratio on the efficiency of the DC-DC converter is analyzed. Fabrication processes for an inductor suitable for 3D integration with a CoFeAlO based core are presented.

Keywords: Inter-wafer Inductors, 3D Hyper-integration, Soft Magnetic Cores, Power Delivery

I. Introduction

Power delivery is becoming a major issue in deep sub-micron microprocessors due to the rapid increase in power, clock frequency and the continuous decrease in the operation voltage. For example, the Intel Dual-core Xeon can dissipate 150 watts at a 1.25 V core supply, while operating at a 3.4 GHz clock frequency [1]. These values necessitate a large current delivery to the microprocessor.

The conventional method of power delivery, as shown in Fig. 1, consists of a voltage regulator module (VRM) mounted on the system board and is distributed via board traces to the chip. This creates a requirement of large numbers of power and ground pins on the chips, and the use of large numbers of decoupling capacitors to filter noise. As future technologies drive supply voltages lower, currents will be driven higher, and parasitics will become more and more problematic. These parasitics will become a fundamental limitation in the ability to deliver power to future generations of ICs [2].

Therefore, new solutions for power delivery are sought. One possible solution is to design a DC-DC converter that can be integrated on a microprocessor [3]. The on-chip power delivery circuit could be used to reduce both the interconnect and the pin count required to

support the power needs of the microprocessor. However, on chip passives, especially inductors, tend to be of very poor quality. The poor quality of the inductors is due to the high resistivity of the wires used, the lossy substrate, and the limitation to an air core.

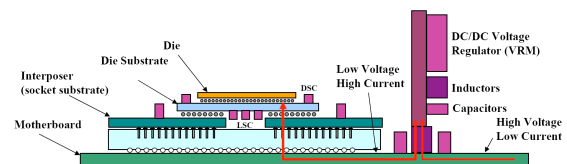


Figure 1: Schematic view of conventional power delivery system. The VRM, Inductors, and Capacitors are mounted away from the microprocessor, and power routed via board traces [3].

Another possible solution is to integrate a power delivery system into a stack of IC system (e.g., processor and memory) by 3D hyper-integration [3], which provides short interconnects between the VRM and the IC system while different materials and processes are separated on different wafers. Wafer-level, back-end-of-the-line (BEOL) compatible, 3D Hyper-integration is perhaps the most attractive 3D approach for high performance applications with

its potential for low cost, high-volume production [4].

One of the Rensselaer approaches to monolithic wafer-level 3D hyper-integration technology uses two fully processed wafers aligned face-to-face or face-to-back and bonded using a dielectric adhesive under conditions compatible with CMOS processing [5]. One of the advantages to this technology is the dielectric adhesive accommodates wafer distortions and interface topographical imperfections. In addition, a separate handling wafer is not required because the wafers are thinned after bonding to a host wafer.

In one 3D power delivery approach, a wafer-level 3D hyper-integration technology, a VRM cellular array on the thinned top wafer can be vertically integrated with the processor using wafer-to-wafer bonding and through silicon vias (TSV). A passive layer consisting of inter-wafer inductors and capacitors is bonded in between, as shown in Fig. 2. The VRM will accept a high input voltage, and therefore require fewer power and ground pins. Different supply voltages required by the 3D integrated system can be supplied by the VRM cells, from below one volt to several volts. The high-performance inter-wafer inductors and capacitors can be fabricated separately from the microprocessors, and thus can use optimized materials and processing that may be incompatible with CMOS. Therefore, magnetic thin film and high-k materials can be used to reduce the size of passive components and improve the performance of the VRM.

In this paper, inter-wafer inductor design with magnetic material is investigated using

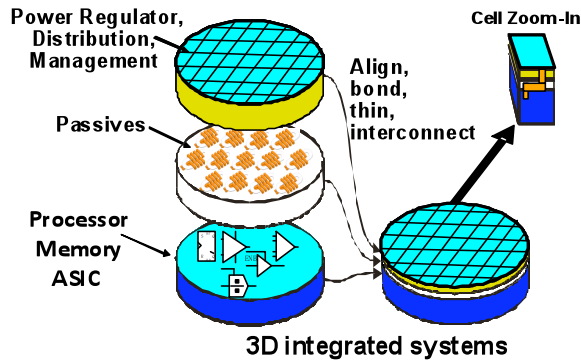


Figure 2: Schematic view of 3D power delivery system, with the Microprocessor on the bottom, a passive layer bonded in the middle and a cellular array of VRMs on the top layer.

wafer-level 3D hyper-integration technology. The inductance and inductance/resistance (L/R) ratio of inter-wafer inductors are evaluated based on the requirements of a DC-DC converter. A wafer-level 3D inter-wafer inductor with a magnetic core is designed and simulated using Maxwell 3D electromagnetic simulator to determine its quality factor and L/R ratio. The influence of the L/R ratio on the efficiency of a DC-DC converter is analyzed. The feasibility of fabricating the inductor and key process steps are investigated.

II. DC-DC Converter Considerations

The DC-DC converter selected for our analysis is the Buck converter that will convert from high voltages to low on chip voltages. As it can only step down in voltage, it is less sensitive to shifts in duty cycle, as it can utilize a whole half cycle for control. An example of a Buck converter topology are shown in Fig. 3.

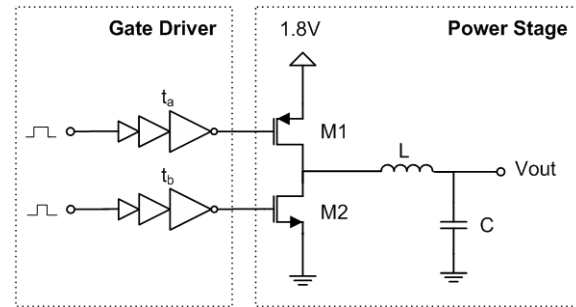


Figure 3: Output stages of an example Buck Converter, designed to step down from 1.8V.

In the Buck converter, and in power delivery systems in general, the efficiency of the VRM is closely linked to the performance of the inductor. Efficiency is defined in equation 1. Essentially, the efficiency is the relation of output power to total power consumed by the system. The key to preserving efficiency is minimizing P_{loss} , which is the sum of the power consumed by the MOSFET switching devices, and the low pass filter, as shown in equation 2 [6].

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \quad (1)$$

$$P_{loss} = P_{cond} + P_{switch} + P_{ind} + P_{cap} \quad (2)$$

Power loss due to the MOSFET is a combination of conduction loss P_{loss} and dynamic switching loss P_{switch} . Filter power loss includes the losses from the inductor P_{ind} , which is due to the series resistance and the stray capacitance of the inductor windings. The losses from the capacitor P_{cap} are due to the effective series resistance of the capacitor, which are usually small enough to be neglected.

$$P_{cond} = R_{on} \cdot I^2 = K_{cond}(I_{load}^2 + \frac{1}{3}\Delta I^2) \quad (3)$$

$$P_{switch} = K_{switch}LV_{in}^2f_s + K_{driver}V_{in}^2f_s \quad (4)$$

$$P_{ind} = \left(I_L^2 + \frac{D^2(1-D)^2V_{in}^2}{3f_s^2L^2} \right) \frac{L}{L/R} \quad (5)$$

In equations 3, 4, and 5, I is the load current, R is the series resistance of the inductor, D is the duty cycle and the various K 's are measurable constants related to capacitances and voltages of MOSFET devices. In the VRM power loss equations, the switching frequency, the load current, the inductance, and the L/R ratio are the major parameters that impact power conversion efficiency that can be controlled by design.

The inductance limits the ripple current, while the ratio L/R includes the effect of the inductor parasitic resistance, which produces conductive losses. The inductance value depends on both the geometry of the inductor and the magnetic core material that is used. The parasitic resistance, and therefore the L/R ratio, depends critically on the switching frequency, due to the skin effect in the copper inductor windings and eddy currents in the magnetic material at high frequency. The resistance can be reduced by increasing the width of the winding wire, increasing the resistivity of the magnetic material, or by laminating the magnetic material to cut the path of the eddy currents. A number of soft magnetic materials have been investigated for application in inductors [7]. High resistivity and high relative permeability are the two most important factors in choosing a magnetic material. In addition, high saturation flux density, low coercivity force, and high ferromagnetic resonance frequency also need to be taken into account for when choosing magnetic materials, but are higher-order performance limiters.

Soft magnetic materials were considered for compatibility with 3D integration as well as

their performance. The alloy was chosen as a benchmark magnetic material to characterize inductor performance. [8] By varying the proportion of oxygen in the alloy, the resistivity and the relative permeability of the material can be modified. For the base CoFeAlO alloy, the value of relative permeability is 1024 and the value of core resistivity is $520 \mu\Omega\cdot\text{cm}$. This material is incompatible with CMOS processes due to its iron content, which is why 3D integration is a promising technology for the use of these inductors.

III. 3D Inter-wafer Inductor Design

For the design of a 3D inter-wafer inductor, a 3D model of the proposed inductor, shown in Fig. 4, was made using SolidWorks. This model was then imported into Ansoft's Maxwell 3D simulator, where the material properties, currents, and other parameters in the model were set. The inductors were simulated by sweeping frequency, permeability and magnetic core conductivity to calculate magnetic fields, inductance, parasitic resistance, and magnetic coupling. The data were then fed to a MATLAB program that calculated the efficiency. This allowed the influence of the 3D inter-wafer inductor on DC-DC converters to be explored. This analysis process was repeated with feedback from MATLAB to further optimize the inductor performance.

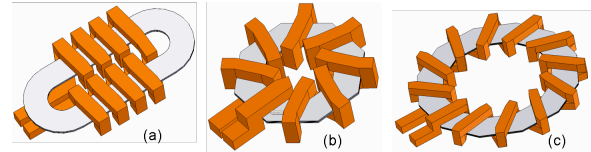


Figure 4: 3D inductor designs with Cu windings around a CoFeAlO core. An oval (a), octagon (b), and dodecagon (c) structure shapes are shown.

Different inductor structures are proposed in this research and the basic structure considered in this paper is composed of copper windings around a magnetic core in the shape of an oval, an octagon, or a dodecagon, as shown in Fig. 4. The width of the copper winding cross section is $20 \mu\text{m}$, the magnetic material is CoFeAlO, and the core has been laminated into $1.5 \mu\text{m}$ layers with $0.1 \mu\text{m}$ silicon dioxide in between to reduce the eddy current loss.

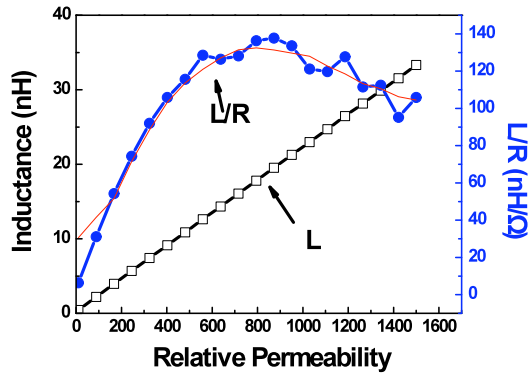


Figure 5: Inductance L and L/R as a function of permeability at a frequency of 50 MHz.

The permeability and resistivity of the magnetic material have significant impact on the inductance and L/R ratio of an inductor. By varying the proportion of oxygen in CoFeAlO , the permeability and resistivity can be changed over a wide range of values. Fig. 5 shows that L is simply proportional to permeability which can be predicted by the toroid inductor model, while L/R has an optimal permeability when the other parameters are fixed.

For low values of permeability, the inductance is low, which makes the ratio L/R low. For high values, the magnetic flux density becomes large and eddy currents in the magnetic material can be induced despite the resistance of the magnetic material. The peak value varies with conductivity as shown in Fig. 6 because a high magnetic core conductivity allows for large eddy currents even when a small field has been applied. Decreasing the conductivity can significantly increase L/R for a fixed permeability. From this analysis, a magnetic material can be selected with an optimal permeability and conductivity.

Inductance and the L/R ratio are slightly different as the L/R depends on many design parameters. After considering the feasibility of physical realization for a desired efficiency a L/R ratio can be selected. For 80% efficiency, the L/R ratio typically should be around 100 nH/Ω to 150 nH/Ω. This value can be obtained with 3D inter-wafer inductors.

In order to investigate the effect of the 3D inter-wafer inductor on the performance improvement in a DC-DC converter, the inductor power loss of the DC-DC converter with a 3D inter-wafer inductor is compared with one with a 2D on-chip inductor as shown in Fig. 7. The data for

2D on-chip inductor is obtained from our previous work of monolithic fully integrated DC-DC converters [3]. It can be found the power loss from using a 2D on-chip inductor is more than three times larger than that of a 3D inter-wafer inductor. Using this 3D inter-wafer inductor we can have a maximum efficiency of up to 87% and minimum power loss at 25 nH and 50 MHz switching frequency, as shown in Fig. 8.

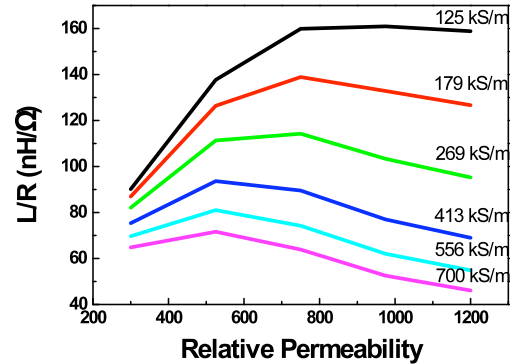


Figure 6: The effect of magnetic core conductivity from 125 kS/m to 700 kS/m on L/R is shown in this graph. The importance of maintaining a high magnetic core resistivity is demonstrated, since the impact of resistivity increases as relative permeability increases.

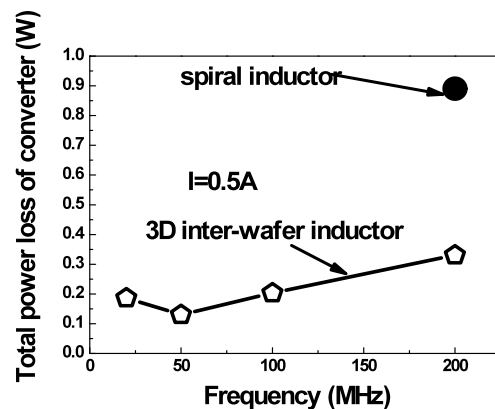


Figure 7: The total power loss of the inductors. The 3D inductor consumes roughly 3 times less power than a corresponding spiral inductor.

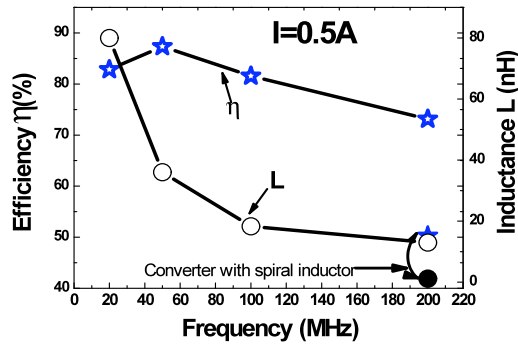


Figure 8: Efficiency comparison of 3D inductor to spiral inductor.

IV. 3D Inter-wafer Inductor processing

The 3D inter-wafer inductor was designed based on previously developed face-to-face wafer-level 3D technology. Using this technology with thick Electrochemical Deposition (ECD) copper, magnetic materials, and thick dielectric layers, the inductor can be fabricated. The dielectric material chosen for the inter-wafer inductor was Cyclotene-63 from Dow Chemical (divinylsiloxane-bis-benzocyclobutene or BCB), which was chosen for its dielectric constant and its compatibility with wafer bonding. A schematic representation of the inductor test structure is shown in Fig. 9.

The inductor fabrication steps include:

- BCB deposition and etching
- Copper filling into the etched features and chemical-mechanic polishing (CMP) to planarize the features
- Passivation deposition
- Deposition and etching of second BCB layer
- Magnetic core deposition
- Copper fill
- Repeat the first three steps for top copper windings.

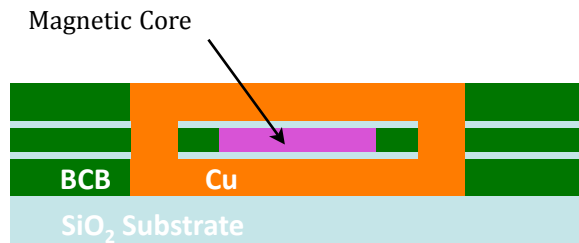


Figure 9: Cross section of inductor test structure.

To begin a successful BCB etch, the BCB was spun onto an oxide substrate to achieve a ten micron layer. The BCB was then fully cured for one hour at 250 on a hot plate to prepare for the next steps. Due to the requirement of an oxygen rich plasma to etch BCB, the etch selectivity of BCB to Photoresist is 1:1. Therefore, a nickel hard mask of 100 nm was sputtered using a DC magnetron sputterer. To avoid damaging the BCB surface, a relatively low power of 500 W was used. The Nickel mask was then patterned and etched with a solution of dilute aqua regia (3 HCl : 1HNO₃ : 2 H₂O). The solution etched the Nickel at a rate of 100 nm/min [9].

The 10 μm BCB layer was a key challenge of this process, as dry etch techniques left residues on the oxide surface. Proper etching is heavily dependent on flow rates, etching power, and chamber pressure. In this work an : plasma in a 9:1 ratio at 300 W was used. A pressure of 30 millitorr and a high flow rate was used to prevent exhausting the and slowing or stopping the etch. Using this recipe, an etch rate of 0.5 μm/min was determined. An Etched via is shown in Fig. 10.

Several methods have been explored for magnetic core deposition, which is a very challenging process to meet the desired dimensions and properties needed for the inter-wafer inductor. The fabrication is in progress and the results will be reported in the conference presentation.

To deposit the copper layers, first a Tantalum barrier layer is sputtered using a DC magnetron sputterer at 750 W for 10 min. Then a

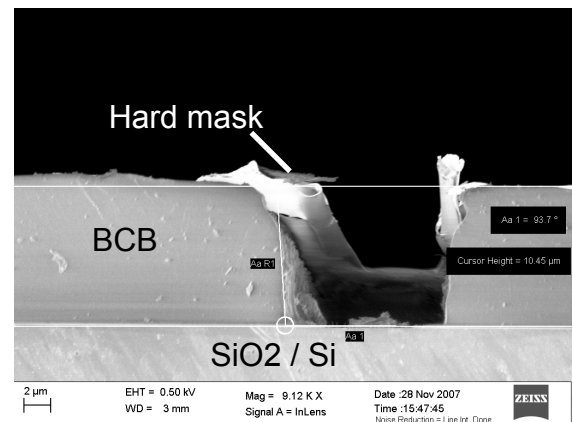


Figure 10: SEM Image of Etched BCB Via, with nickel hard mask on a Silicon Dioxide substrate. A vertical via profile can be seen.

copper seed layer is sputtered at 1.5 kW for 15 min. After the copper sputter, the wafer is placed in a Copper ECD chamber. The wafer is plated in a solution from Ethone at a current density of 15 mA/cm².

5 Summary and Conclusions

This paper analyzed the efficiency of DC-DC converters when paired with a 3D wafer-level hyper-integrated inductors. The inductors were designed with Solidworks, simulated with the 3D magnetic simulator Maxwell, and the efficiency was calculated using MATLAB. The power loss of a 3D inductor was shown to be three times that of an on-chip spiral inductor. CoFeAlO was chosen as a good soft magnetic material for use in the inductors magnetic core. The key parameter of inductance to winding resistance was tested, and its dependence on permittivity and resistivity of the magnetic core. Key process steps were designed to etch BCB at a 10 μ m thickness, as well as the growth of 10 μ m thick copper films.

3D power delivery can overcome the problems of conventional power delivery. 3D power delivery allows use of materials incompatible with CMOS processing like iron alloys. These incompatible materials can have a significant impact on the inductance. 3D integration of the DC-DC converter cellular array will allow tight control over power delivery, as well as reducing parasitics.

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