

A New Idea to Manufacture High Density Packaging Substrate

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Abstract

In the roadmap of electronic packaging, high routing density and economical manufacturing cost are two important goals. Unfortunately, these two goals are not easy to be achieved simultaneously. A new idea to manufacture high density packaging substrate is introduced in this paper. By using temporary carrier in our manufacturing process, a highly precise alignment and extremely thin dielectric layer can be processed. This process can be used to make high density packaging substrates. This kind of substrates has high routing density and light weight. Furthermore, this kind of substrates also provides flexible properties because of its extremely thin thickness.

A series of data show the performance of this substrate: 45 μm via pitch, 15 μm width line and space, and 8 μm thick dielectric layer. According to these data, the routing density is highly increased, and this property can make our substrates meet the technical roadmap economically. For example, fanning out a flip chip substrate with 3 rows of bump pads can be completed in only 1 routing layer instead of 2 or 3 layers. The materials and process steps are decreased. In this way, it is possible to achieve low cost packaging. In addition, based on the common design rule of flexible printed circuit boards, the bending radius of curvature is 10 times of the thickness of substrates. Decreasing thickness can make substrates flexible. Therefore we tested the flexibility of our substrate and also got good results. Moreover, a multi-chips SIP system prototype is made to demonstrate our substrates. This SIP system used a 7-layer substrate totally with 2042 pads, and the substrate size is only 39mm*39mm.

Key words: packaging substrate, SIP, flexible substrate, routing density, temporary carrier

Introduction

The improvement of semiconductor packaging technology is getting faster and faster. Increasing variety and shrinking sizes are the major trend. The most important driving force is the portable electronics. In these applications, system in packaging (SIP) is a very suitable technology to meet their requirements. Actually, some digital cameras and smart phones have introduced this technology.

According to the roadmap of ITRS, higher routing density, higher pin counts and thinner thickness are targets of packaging substrates. Especially for SIP, More integration needs more complex packaging substrates. In this paper, we have shown the keys to improve routing density are economical and precise alignment, and make our packaging substrates by this concept.

To achieve good alignment in packaging substrates process, engineers need to overcome the distortion of the substrate size and equipment limits. A common distortion of organic substrate is recorded about 200 ppm. Most engineers will consider step and repeat exposure method which uses a relatively short alignment baseline, i.e. stepper, to get a precise alignment. Although engineers can achieve good alignment in this process, they have to take the risk to lose the through put.

Process

In this paper, we have discovered a new process to improve alignment. The process flow is shown in Fig.1. A substrate process is done on a rigid temporary carrier to overcome the distortion of substrate. In the first step, we choose a carrier. The guideline is using flat and rigid carriers to overcome the distortion of organic substrates. The materials of this carrier can be silicon, glass, metal or ceramics. We also calculate the mechanical properties of the carrier and the substrate material to confirm efficacy.

Next, we coat polyimide as the dielectric layer of our substrates on this carrier. In this step, we have to modify the adhesion between the carrier and the first polyimide layer. The adhesion strength is modified to make the substrate not peel off from the carrier during processing but easily separates from there after being cut. The method to modify adhesion between the carrier and the first polyimide layer is a surface treatment before polyimide coating. This surface treatment changes the free energy of carrier surface, and makes the adhesion strength change. In this coating step, we use spin coating to coat this polyimide layer. In addition, other coating methods like spray or extrusion die coating can be used too. Because of the perfectly flat surface of our carrier, a

thin and uniform dielectric layer can be made. This is another benefit of solid carriers in the coating process. The properties of our dielectric layer can be found in table.1.

The third step is the metal patterning process. We use metal lift-off process. Thus photoresist is processed first, and then a metal layer is coated on the surface by physical vapor deposition. At last, photoresist is stripped off from the surface and correct metal patterns are left. Other metal patterning processes like etching and semi-additive process can be used too, but they have their own disadvantages. The undercut during etching and loading effects of electroplating are their known drawbacks. Metal lift-off process avoids these issues and can get fine lines. The limit size of our metal patterns is 5 μm . However, our design rules are set on 15 μm for the reason of criteria of trace resists. The properties of our metal layer can be found in table.1.

The final step is via process. We use laser drilling process in our via process. Laser drilling can process any kind of organic materials. Therefore we have a lot of candidates in our dielectric materials. In this case, we used a low Dk polyimide material as the dielectric layer. The properties of this dielectric layer can be found in table.1.

We also developed the photo via process, but mechanical properties of photo sensitive polyimide were not good enough for packaging substrates. Most of them were easily cracked. Therefore, this process still needs to be co-developed with material suppliers.

By repeating metal patterning and via process several times, we can get a multi-layer substrate. Then we

cut the edge of the substrate to release the substrate from the temporary carrier. Owing to the adhesion strength between our substrate and carrier is well modified; the substrate does not peel off from the carrier during processing but easily separates from there after being cut. In addition, the carrier is not destroyed during cutting; therefore it can be recycled for next use.

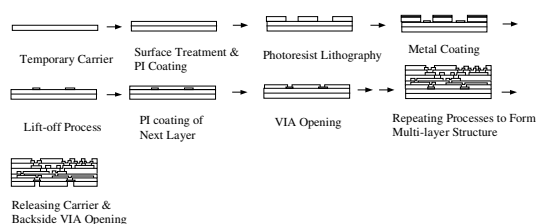


Figure 1. Process of the substrate

Routing Density

Referring to table.1, our substrates have shown an outstanding performance in routing density, thickness and flexibility. It is known that fanning out flip chip pads needs the highest routing density. From the roadmap of ITRS, flip chip area array pitch will reach 110 μm in near term. It is a crucial challenge to packaging substrates. Although engineers can increase routing layers to meet layout requirements, but the cost of substrates increases simultaneously. Fig. 2 is an illustration of a layout example in our design rule. Because of our precise alignment, the covered via land and captured via land are just 30 μm , plus our 15 μm line and space rules, the total pitch to fan out 3 rows flip chip array is just 105 μm in one routing layer. In the conventional design rule, the captured via land is 70~80 μm , engineers usually need 3 layers to fan out this flip chip array. Our substrate obviously saves layout layers. Therefore, owing to the high routing density, our substrates can economically meet the future trend.

Table.1 Design rules of the substrate

Metal Line/Space	15 μm /15 μm Min.5 μm /5 μm
Metal Thickness	3 μm
Dielectric Layer Thickness	8 μm
VIA size	20 μm
Covered VIA Land	30 μm
Captured VIA Land	30 μm
Min. VIA Pitch	45 μm
Coreless	Yes
Adhesive	No
MIT Test of Trace (R=1mm)	>100000 times
MIT Test of VIAs (R=1mm)	>100000 times
Dk	2.9

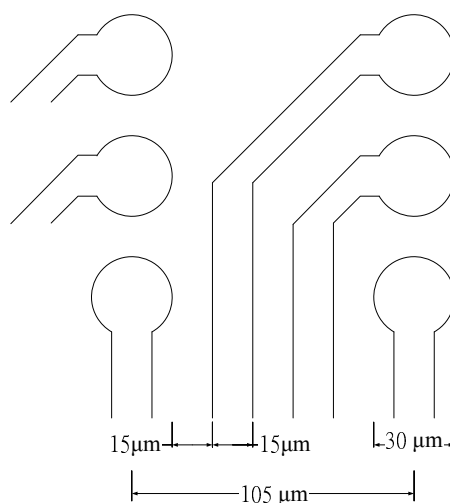


Figure 2. Layout example in our design rules

Thickness and Flexibility

Owing to the perfectly flat surface of the carrier, the dielectric layer of the substrates is very thin. The thickness of the dielectric layer is just 8 μm . It is good for miniaturization of electronic products. For example, a real case of our 6-layer substrates is only 74 μm thick. By comparing to conventional 6-layer

substrates, their thickness are more than 200 μm , our substrates have shown a significant improvement in thickness.

From the known design rules of flexible circuit boards, the radius of curvature to be bent should be larger than 10 times of the thickness of the flexible circuit board. In-other words, if the substrates are thin enough, every substrate can be bent. Therefore, we wanted to test the flexibility of our substrates. This bending test used MIT standard bending tester. Testing conditions were listed as follows: the bending angles are ± 90 degrees and the radius of curvature is 1 mm. Although the common design rules of flexible circuit board suggested avoiding vias in the bending area, we still tried this kind of samples. At this time, we tested two kinds of substrate samples: 1-layer patterns of 30 μm wide trace and 2-layer patterns of series of 20 vias. Fig.3 is an illustration of these two samples. The thickness of the samples were 40 μm and the real bending area was 4 mm long to match the size of the tester. Both of these two samples passed 100000 times bending. It was a crucial testing criterion for dynamic bending applications. This result showed excellent flexibility of our substrates.

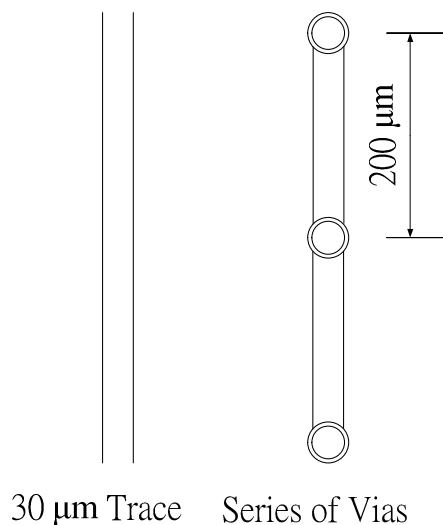


Figure 3. Illustration of two bending samples

In conventional applications, flexible circuit boards are used as connectors, thus it is not necessary to place vias in the bending area. However, vias in bending area can possibly be applied in SIP or flexible electronics. Fig.4 is a hypothetical processor module in 3D packaging. In this module, bending the substrate at the area of memories can save the packaging footprint. It is necessary to cross layers at this bending region in this case. Thus engineers have to place vias in this bending area. Although the applications of vias in the bending area are not so popular, it really expands our imagination. We believe it is an important advantage for our substrates in 3D packaging.

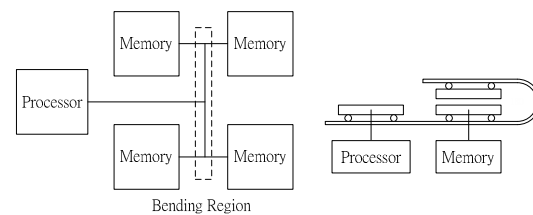


Figure 4. Hypothetical processor module in 3D packaging

Reliability

Reliability is very important to packaging substrates, especially for a new process. Therefore, we had reliability tests to prove its practicability. In our tests, twenty substrate samples were tested. Every substrate had 4 testing patterns of inter-digital and 4 testing patterns of vias' series. The 4 testing patterns of inter-digital were used for checking metal migration under voltage bias and the 4 testing patterns of vias' series were used for checking the reliability of vias under long term operation. For simulating the conventional design, the layout rules of these patterns were set on 30 μm line width, 30 μm space width and

20 μ m via opening size. Testing module is shown in Fig.5. All tests followed JEDEC No.22. We set testing conditions on 85°C/85% RH, and pass criterion was 1000 hours. After testing, the results showed the resists of all interdigital patterns kept larger than 1 G Ω and the operation of all vias' series kept normal after 1000 hours. Our substrates were confirmed to pass the reliability test.

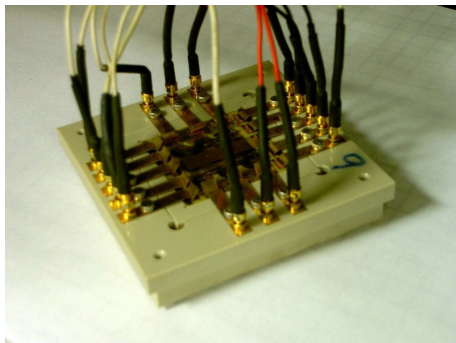


Figure 5. Reliability testing module

SIP system

For demonstrating practicability of our substrates, a multi-chips SIP system prototype was made. Fig.6 is its photograph. This SIP system including 5 flip chips, 17 CSP components, 6 connectors and 261 SMD passives used a 7-layer substrate which had totally 2042 pads. Even so, the substrate size was just 39mm*39mm and its thickness was only 85 μ m. Fig.7 shows thin thickness and good flexibility of the substrate. We successfully made the substrate and assembled dummy components on it to develop the whole packaging process. All interconnections of the substrate passed electric tests. Now, we are developing this system which is assembled with real components. A full function SIP system is our next target.

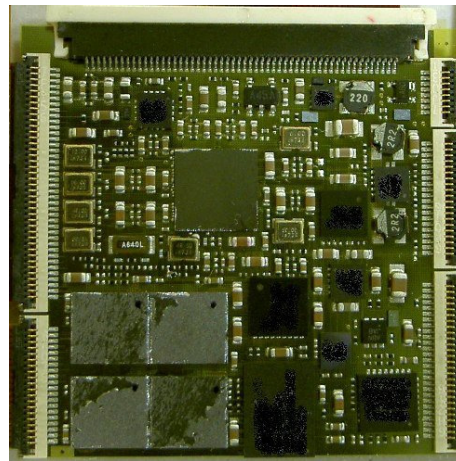


Figure 6. Demonstrating SIP system



Figure 7. Bending the 7-layer SIP substrate

Summary

We introduce a new method to produce packaging substrates. Substrate made by this method can achieve high routing density, thin thickness and good flexibility. Furthermore, the reliability results and a demonstrating SIP system have shown it is suitable for real applications. Owing to the performance of our substrates, a more complex and compact SIP system can be made. We are developing a full function SIP system to explore new applications.

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