

3-D VLSI Structure for High Power and High Speed Computation

Y. Liu¹, L. Schaper¹, S. Burkett²

University of Arkansas¹

University of Alabama²

Bell 3217, University of Arkansas

Fayetteville, AR 72701

yx1003@uark.edu

Abstract

The University of Arkansas has performed extensive research on a novel 3-D packaging technology by die stacking. This method has the potential to address the cumulative yield problem of 3-D stacking and is designed to handle high heat flux and provide high speed interconnections. TSVs filled with copper are manufactured by DRIE and reverse pulse plating to provide signal paths between active devices and the back side of individual layers. Copper posts and dams capped with tin are plated on the back side of most layers. After preselecting known good die, copper posts and dams are joined to the matching pads on adjacent layers by copper/tin intermetallic. Vertical electrical connections are realized by posts and vias. Mechanical support is provided by both copper dams and posts. Micro-fluid channels are formed by each pair of die layers and dams in between. Coolant is circulated in the channels to remove 20 W of heat from each layer.

The thermal test vehicle comprises four TSV die layers. Three of the layers have posts and dams for interlayer interconnection. Thin film heat dissipation resistors are placed in each layer to simulate device power dissipation. Resistive temperature sensors are embedded in every layer to monitor the performance of the cooling mechanism. Daisy chains are also included for reliability test. Up-to-date experimental results will be presented in this paper.

Key words: 3-D VLSI, TSV, High heat flux, Copper post

Introduction

A 3-D VLSI technology by chip stacking has been researched extensively at the University of Arkansas in order to solve the problems of wafer stacking technology including cumulative yield issues, CTE mismatch from heterogeneous materials, difficulties of heat removal from individual layers, and lack of methods to distribute power to individual layers. TSVs are formed in each silicon layer to route signals and distribute power in the vertical direction through an individual chip. Tin capped copper posts and dams are built and used to connect every pair of adjacent layers and form micro-scale fluid channels, in which coolant is circulated to remove heat. [1],[2] A drawing of this scheme is shown in Figure 1.

Thermal Test Vehicle

The Thermal Test Vehicle has been designed to prove the feasibility of the UA approach. It comprises four layers. Figure 2 shows two 3-D views of the thermal test vehicle. The bulk silicon is hidden in order to show the structures embedded in each layer. In order to connect to the printed circuit board, solder balls are placed on the backside of the first layer. Copper posts and dams are built on the back side of the other three layers. The second, third and fourth layers are bonded with a flip chip bonder at 300°C with applied pressure, sequentially one on top of the

other. Thin film copper heat dissipation resistors are placed in each layer to simulate device power dissipation. Resistive temperature sensors are also embedded in every layer to monitor the performance of the cooling mechanism. Daisy chains are included for reliability testing.

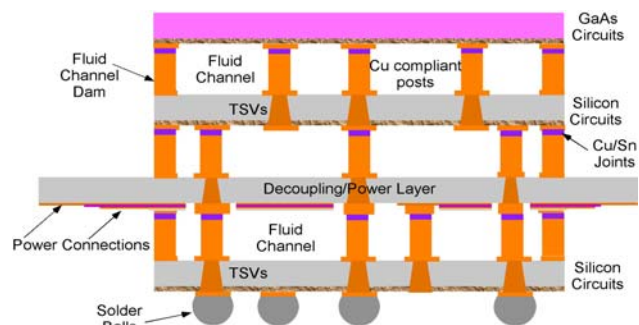


Figure 1. Conceptual schematic of U of A system [2]

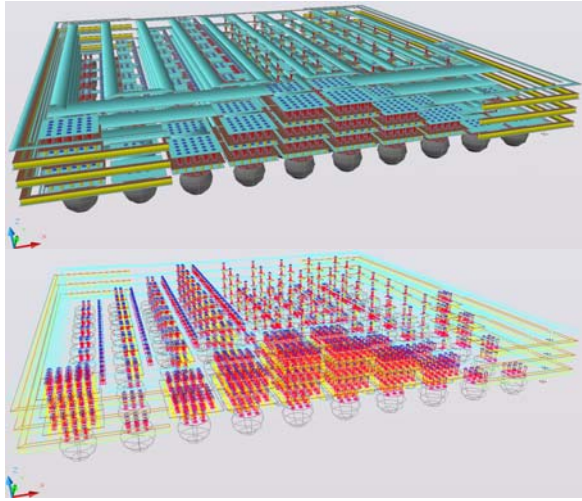


Figure 2. Thermal test vehicle

Process Overview

Blind TSVs are etched into a silicon wafer, insulated with SiO_2 , and lined with sputtered titanium and copper. Vias are then filled by blanket reverse pulse plating. Next the front side copper overload and seed layers are etched back and the front side circuit is formed by sputtering titanium and copper and pattern etching. After front side processes, the wafer is bonded to a carrier wafer, flipped over and thinned from the back side. Further RIE etching can be used to expose the via base, and PECVD silicon oxide is deposited as an insulation layer. For contact purposes, the oxide is pattern etched to open the areas on top of the vias. Backside traces are plated after deposition of adhesion and seed layers. Compliant copper posts, as well as copper dams, are plated on the traces by using thick photoresist molds. Next the posts and dams are planarized with photoresist remaining in place and pattern plated with tin on top of all posts and dams. After metallization, the process and carrier wafer stack is diced into $10.9 \text{ mm} \times 10.9 \text{ mm}$ chips. The thick photoresist is then stripped by an organic solvent. Meanwhile, the process chip is debonded from the carrier chip. The seed layer is then etched back and the known good die are picked. All four different layer chip designs are built on the same wafer.

Tin capped copper posts and dams are joined to the matching pads on adjacent layers by a copper/tin intermetallic material. Vertical electrical connections are realized by posts and vias. Mechanical support is provided by both copper dams and posts. Micro-scale fluid channels are formed by each pair of die layers and dams in between. Coolant is circulated in the channels to remove 20 Watts of heat from each layer.

Front side process

STS deep reactive ion etch (DRIE) is used to form blind vias in a silicon substrate. The photoresist is then removed by Piranha cleaning. A layer of PECVD silicon oxide is deposited to insulate all surfaces including the side walls and bases of the vias. Next the wafer is lined by sputtering a titanium barrier layer and a copper seed layer. It is necessary to achieve a tapered via profile in order to form conformal linings in the vias. However, the Bosch process typically provides straight via side walls. Therefore, a modified Bosch process comprising seven modules of different etching / passivation time ratios has been applied. The via profile is shown in Figure 3. [3]

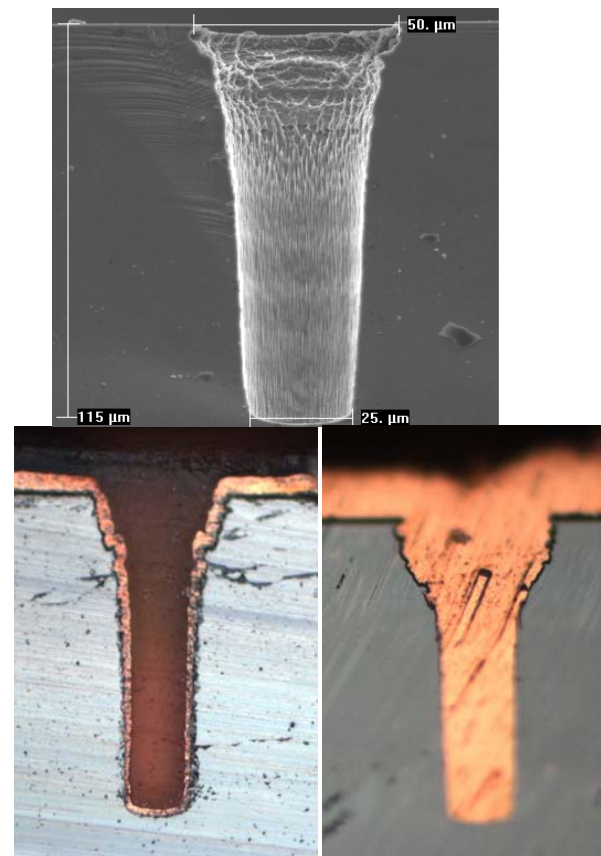


Figure 3. Tapered via profile, conformal lining and void free filling [4]

The wafer is then reverse pulse plated to fill the vias from bottom to top without creating any voids. The vias are masked and the front electroplated copper, sputtered seed and barrier layers are etched.

Because the wafer needs to be thinned to $110 \mu\text{m}$, and a 250°C PECVD step is necessary to insulate the back side, the thinnest possible adhesive

layer between process and carrier wafers is needed. Therefore further decreasing the height of the bumps on the vias is necessary. The wafer is briefly etched after stripping the photoresist, so that the bumps are less than 5 μm high.

Again a titanium barrier layer and a 2- μm copper layer followed by 600 Å titanium protection layer are sputtered and pattern etched to form the front side circuit.

Adhesive Bonding

The back side processing, especially the PECVD and descum steps, also place many requirements on the bonding process. Air bubbles, voids, or moisture can lead to cracking of the wafer during these heated processes in vacuum.

In order to address this problem, a new method of adhesive wafer bonding has been developed at the University of Arkansas and is illustrated in Figures 4 and 5. This method uses a regular vacuum oven and a hydraulic press. The process wafer is spin-coated with 8 μm of HT-250 adhesive from Brewer Science and baked at 160 °C and 220 °C for 2 minutes, respectively. It is stacked with the carrier wafer in atmosphere and placed on a glass plate. Three Sn/Pb spacers thicker than the wafer stack are placed around the wafer stack. Another glass plate is then gently placed on the spacers and weight is stacked upon it. After loading, the oven is sealed and vacuum is applied under low temperature (Figure 4). The oven is heated to the melting temperature of HT-250. Because the melting temperature of Sn/Pb (183°C) is below the melting temperature of HT-250, the spacers will collapse. The weight will compress the wafers and apply bonding pressure (Figure 5).

The scanning acoustic microscopy (SAM) image in Figure 6 shows the bonding achieved by this method. The white areas are voids caused by insufficient pressure, which is limited by the volume of the oven and thus the size of the weight that can be accommodated. However, because vacuum is applied before HT-250 melting and maintained until the wafers are bonded, there should be negligible air in the voids. Therefore, a subsequent 2.5 ton compression in a hydraulic press at 230°C can eliminate the voids. Meanwhile, the inconsistent height of copper bumps above the vias will be remedied because the bumps are coined under this pressure. Figure 7 shows the SAM picture of the same wafer after the 2nd heating in a hydraulic press.

To note, experiments showed that if both process wafer and carrier wafer are coated with HT-250, the first reflow in a vacuum oven is enough to create void free bonding. However, because of the CTE mismatch between polymer and silicon, an

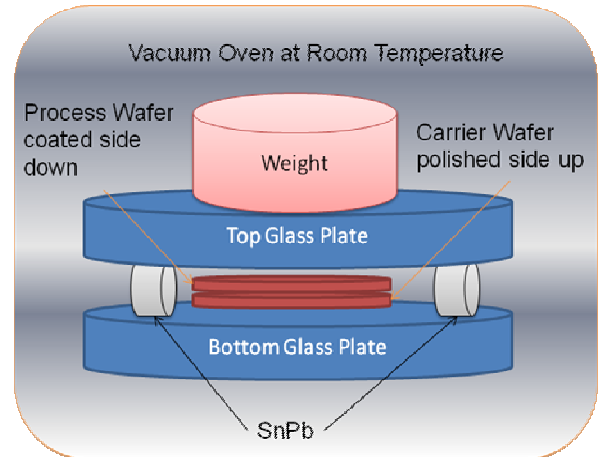


Figure 4. Wafer Stack at Room Temperature in Vacuum Oven

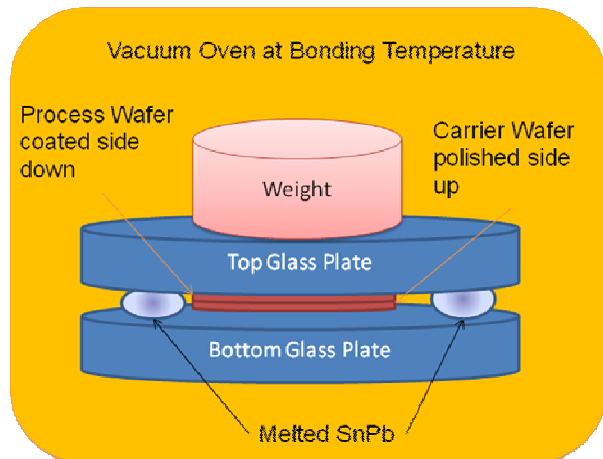


Figure 5. Wafer Stack after Reaching Bonding Temperature in Vacuum Oven

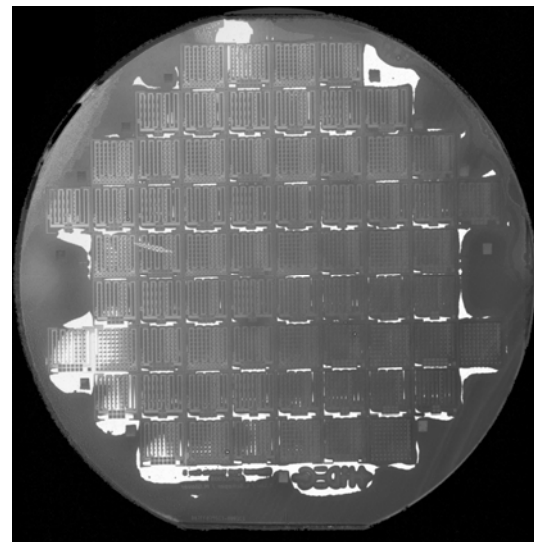


Figure 6. SAM Picture after 1st bonding

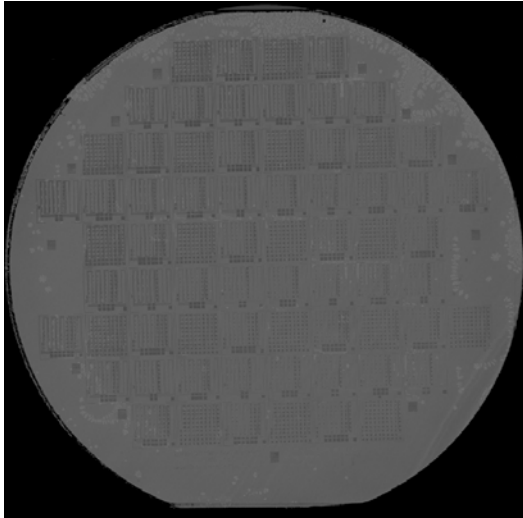


Figure 7. SAM Picture after 2nd bonding and compression

adhesive layer that is too thick may crack the thin process wafer during backside processes. That is why a thin adhesive layer has been used.

Backside process

After bonding, the wafer is thinned by mechanical grinding and polishing. A Logitech PM5 Lapping System and Logitech PLJ7 vacuum lapping jig as well as alumina slurry are used. Historical data has shown that no matter which direction the wafer is mounted on the vacuum jig, the bottom half of the wafer is always ground faster than the top half. Considering the symmetric position of the wafer stack on the lapping jig and the rotation of the jig, the reason could be that the pressure on the bottom half is greater than on the top half due to the existence of the primary flat. Therefore, weights are placed on the lapping jig to compensate for the planarity error. By adjusting the position of the weights, $\pm 2 \mu\text{m}$ or less error in thickness over an entire 125 mm diameter wafer can be reproducibly achieved. Because the DRIE etches large features deeper than small ones, arrays of $50 \mu\text{m}$ vias are placed across the wafer as grinding stops. When these arrays are exposed, the ground surface is approximately $10 \mu\text{m}$ away from the top of the $30 \mu\text{m}$ diameter vias and grinding should be terminated. The wafer is then polished to remove mechanical defects and reach a reasonable smoothness necessary for backside film deposition and patterning. The final $10 \mu\text{m}$ of silicon are removed by pattern etching using RIE to form depressions or trenches around the via locations.

Since HT-250 adhesive absorbs moisture during steps such as grinding, polishing, and SAM inspection for bonding quality, and moisture will

crack the process wafer in the subsequent PECVD step, the wafer stack is dehydration-baked in a vacuum oven at 110°C over night.

Thin as it is, the process wafer is sensitive to thermal shock and moisture after back grinding. In the following steps such as depositing silicon oxide by PECVD and sputtering Ti/Cu barrier/seed layers, a slow temperature ramp up and down must be used. It is also necessary to perform a dehydration bake after plating copper traces and nickel/gold, or even when a wafer stack remains in atmosphere for several days, since the descum step of the subsequent KMPR photolithography may also cause wafer cracking from absorbed water vapor.

Post Fabrication

To fabricate the tall ($100 \mu\text{m}$) copper posts and dams, HMDS is applied to promote adhesion between photoresist and copper and KMPR photoresist (MicroChem Corp.) is spun on the wafer. Double coating is implemented in order to achieve uniform $100 \mu\text{m}$ thick photoresist films. The trace thickness and depth of the trenches formed by RIE have also been found to be a major influence on the quality of the KMPR molding layer. The number of pin holes increases when thicker traces are plated or trenches exist.

Following KMPR application, the wafer is baked, exposed, and post exposure baked. After being developed in an ultrasonic bath, the wafer is then treated with oxygen plasma to remove the photoresist residue at the bottom of the post pattern. Next the posts are DC copper plated, planarized by mechanical grinding with KMPR in place, and pattern plated with tin. The resulting posts are shown in Figure 8.

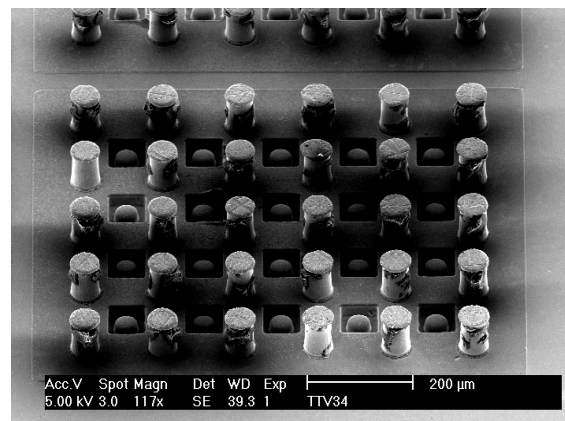


Figure 8. Copper posts built on thermal test vehicles

Chip debonding and photoresist strip

Normally, the HT-250 adhesive needs to be debonded by applying a shear force at 250 °C. However, the KMPR could not be removed after experiencing this temperature. Photoresist stripping thus became a problem.

Fortunately, experiments showed that the diced chip stacks can be debonded in heated solvent under ultrasonic agitation. This can be done while stripping the KMPR, resulting in chips ready for assembly.

Assembly

The assembly process has been reported at IMAPS 2007 [5]. The thin chips will be a challenge for the flip chip assembly process. In the design stage, the difficulty has been anticipated. Therefore, the mask has been designed in such a way that no post is to be bonded anywhere without support from the bottom. In other words, all the posts of the 3rd and 4th layer are designed to be stacked on top of the posts of the previous layer. More experimental results will be reported at a later time.

Conclusions

The University of Arkansas is developing a 3-D VLSI process for high power and heterogeneous material systems. Several key technologies such as via formation, via filling, wafer bonding, wafer thinning, post fabrication, and flip chip bonding have been developed. In order to increase the overall yield, many steps have been significantly modified during thermal test vehicle fabrication.

Acknowledgements

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