

Investigation on Statistical Distribution of Electromigration Lifetimes in Flip Chip Solder Bumps

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Abstract

Electromigration of flip-chip solder bump is one of the emerging issues resulting from the rapid down-scaling of features in semiconductor. While the lifetime statistics of solder EM is normally governed by lognormal distribution, extrapolations exist and need to be addressed to correctly assess the true reliability performance at operating conditions that are usually significantly different from the highly accelerated lifetime tests. In this case study, lifetime data of flip-chip packages with Ni Under Bump Metallurgy (UBM) and SnAg solder bump were used to investigate the origin of standard deviation, sigma. For the different testing conditions, the calculated sigma values showed a large variation from 0.78 to 1.66. The impact of extrinsic factors such as temperature, current density and failure mode on sigma will be analyzed, and it showed that the standard deviation induced by temperature and current density was 0.29–0.38 and 0.43, respectively. The impact of the intrinsic factors such as grain size and crystal structure on the EM damage evolution was discussed qualitatively as well. The statistical behavior of solder EM was determined to be quite different from that of the interconnect EM. These results showed that better understanding of the standard deviation is important in assessing the true EM lifetime of solder bumps.

Key words: Electromigration, Statistics, Reliability, Solder, Flip-Chip

Introduction

Electromigration (EM) phenomenon in flip chip solder connection is one of the emerging issues induced by the continuing increase in power and down scaling of IC packaging features. Although the electromigration phenomenon has been intensively studied at the silicon level for interconnect lines since the late 1960s, it is far less understood in solder bumps. Electromigration in solder joints can be quite different from that of the interconnects due to the differences in material systems and structures. Previous studies [1-5] have shown that EM induced failures occur mainly by void growth at the interface between the under bump metallurgy and the solder alloy. The corresponding lifetime statistics usually follow a lognormal distribution in the form of

$$pdf(t) = \frac{1}{\sigma\sqrt{2\pi}} \exp\left[-\frac{(\ln t - \ln t_{50})^2}{2\sigma^2}\right] \quad (1)$$

where pdf is the probability density function, t is the time and t_{50} the median-time-to-failure (MTTF).

For electromigration, MTTF was found to be dependent on the current density, the temperature and the diffusion behavior of the interface as described by Black's equation [6]

$$MTTF = A j^{-n} e^{\frac{Q}{kT}} \quad (2)$$

To obtain data within a reasonable amount of time, high accelerated lifetime test (HALT) is normally conducted with current densities and temperatures significantly higher compared to operating conditions. Therefore, extrapolations are necessary to assess reliability at operating conditions. Furthermore, the sample size of EM studies is usually

on the order of $10^1 \sim 10^2$, representing a failure percentile up to $\sim 1\%$ when the first sample failed. The industry requirement is normally on the order of 0.01% or lower. Hence, the extrapolation needs to take into account how to assess on-chip reliability from the EM-tested sample population. The following equation, based on Black's initial work on EM [1969], describes the dependence of time-to-failure under operating conditions, TTF_{oper} , on experimental parameters:

$$TTF_{oper} = MTF_{stress} (I_{stress} / I_{oper})^n \exp \left[\frac{E}{k} \left(\frac{1}{T_{stress}} - \frac{1}{T_{oper}} \right) + N\sigma \right] \quad (3)$$

where MTF_{stress} is the median-time-to-failure as obtained in an EM experiment, I_{stress} , I_{oper} and T_{stress} , T_{oper} are the currents and temperatures used during the EM test and under operating conditions, respectively, E is the activation energy, k is Boltzmann's constant, N the number of standard deviations and σ the lognormal standard deviation. The parameter n represents the current density exponent, which as been determined experimentally to be $1 \sim 2$ [5, 7]. The variable N is determined by the desired failure percentiles. For 0.01%, N equals to 3.719. As can be seen from (3), the standard deviation is not a trivial parameter since the extrapolated EM lifetime depends exponentially on it. There are extrinsic and intrinsic origins of the standard deviation. The extrinsic sources are the deviation of experimental parameters from the set nominal values, such as current density and temperature. The intrinsic sources are the variation of the microstructure of the samples under test. Most studies on solder EM by now have focused on describing the solder EM performance by MTF, and the exponential influence of sigma is generally neglected.

In this work, a case study was conducted to understand the magnitude and sources of the standard deviation in solder EM test. A flip-chip package with Pb-free solder bump was stressed under various temperatures. The damage evolution inside the solder bump was monitored by a Wheatstone bridge circuit. The lifetime statistics was drawn and MTF and standard deviation was obtained. In the meantime, possible sources of standard deviation were identified. Their impact on the magnitude of standard deviation was discussed and correlated to the experimental value.

Experimental

EM tests were performed on 97.5wt%Sn-2.5wt%Ag (Sn-2.5Ag) solder bumps in flip chip

package with ceramic (alumina) substrates. The structures of the solder bump tested are shown in Figure 1. The Sn2.5Ag solder bump had a nominal diameter of $130\mu\text{m}$ and height of $60 \sim 80\mu\text{m}$. The passivation opening was $55\mu\text{m}$. The under bump metallization (UBM) had a $0.25\mu\text{m}$ -TiW/ $18\mu\text{m}$ -Cu UBM, and the other had a $0.1\mu\text{m}$ -Ti/ $2\mu\text{m}$ -Ni. Thickness variation of Ni UBM was $\pm 1\mu\text{m}$. On the substrate side, the solder pad was Cu with $5\mu\text{m}$ electrolessly plated Ni(P).

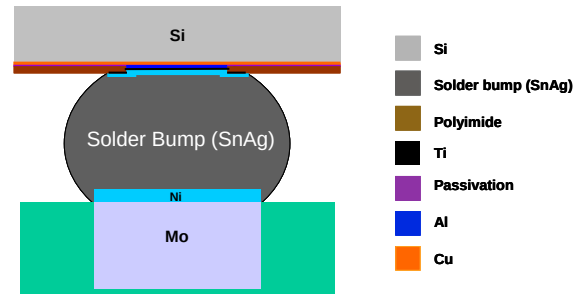


Figure 1. Structure of the Solder Bump Tested

To reduce the measurement errors, a Wheatstone bridge circuitry was used to detect the small resistance change in solder bumps during electromigration tests. A fixed resistor R_1 , and a variable resistor R_2 formed one branch of the bridge circuit as shown in Figure 2. Both values are in the order of 10^3 ohms. The other branch contains two pairs of solder bumps, R_3 and R_4 , whose resistance is about several milli-ohms. In each pair of the joints, the cathode bump refers to the solder bump in which the direction of electron current is from the substrate to the die, and the anode bump refers to the bump with the opposite direction of electron current.

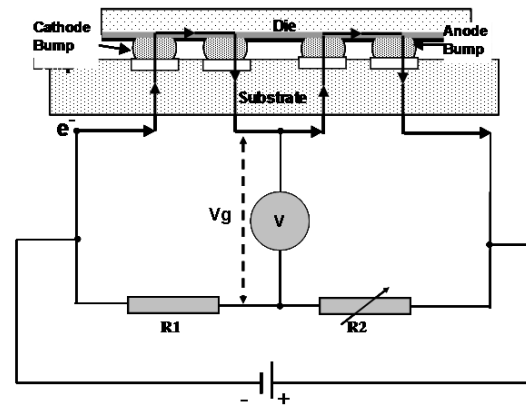


Figure 2. Cross-section of solder bump pair under test and test circuitry

When starting the EM test, the off-balance voltage V_g in the Wheatstone bridge circuit was set to zero by adjusting the variable resistor R_2 . The value of V_g was directly correlated with the net resistance change of solder bumps [8]. In the test setup, R_1 and R_2 are kept constant and $R_1 \approx R_2 \gg R_3 \approx R_4$. Therefore, the correlation of solder bump resistance change to V_g can be simplified to

$$V_g = 0.5I(R_3 - R_4) \quad (4)$$

During electromigration testing, the samples were heated in an oven. The Joule heating induced by the applied current was checked by attaching a thermocouple to the top of the die and compared with the temperature of the ambient temperature of the oven. Due to the relatively large current supplied in the EM test, Joule-heating was found to increase the test temperature by about 20~30°C over the ambient. Finite element thermal analysis showed that the temperatures of the solder bumps under test were 10~15°C higher than that of the die top. Three EM tests were performed with ambient temperature 90°C, 105°C and 120°C, respectively. For the 90°C and 105°C runs, the current density was $3.5 \times 10^4 \text{ A/cm}^2$. For the 155°C run, the current density was $4.1 \times 10^4 \text{ A/cm}^2$. The current density was calculated by dividing the applied current by the area of passivation opening on the silicon chip. All test conditions are listed in Table 1.

Table 1 Test conditions of the EM test

Temperatures	Ambient (Oven) (°C)	90	105	120
	Die Top (°C)	110	122	155
	Solder Bump (°C)	120	132	170
Current Density (10^4 A/cm^2)		3.5	3.5	4.1

After electromigration testing, selected packages were cross-sectioned and polished to the mid-plane of the tested bumps for failure analysis. Backscatter electron imaging mode of scanning electron microscopy (SEM) was applied to examine the morphology of the solder bumps. Energy-dispersive x-ray spectroscopy (EDS) was used to determine the composition of the intermetallic compounds.

Results

A typical V_g trace from EM test is shown in Figure 3. The V_g trace increased from 0 to ~30mV smoothly before showing a sharp jump. The 30mV change corresponded to ~60mΩ change in bump resistance which is 10x the original value. This suggested that the bump structure had been significantly destructed. For the analysis in this study, 30mV was selected as the failure criteria, while it is noted this value is different from those used by the recently published JEDEC standard, JEP154.

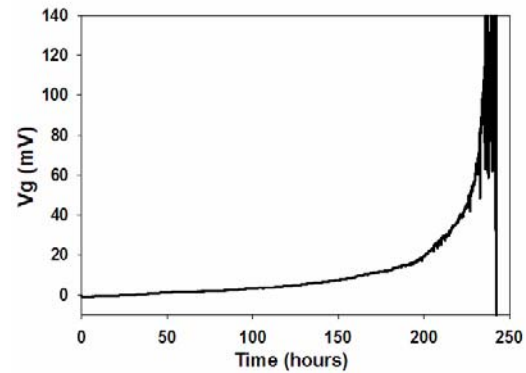


Figure 3. Typical V_g trace in EM test

The log-normal cumulative distribution functions of failure (CDF) of the test structures are summarized in Figure 4. The distribution parameters are listed in Table 2.

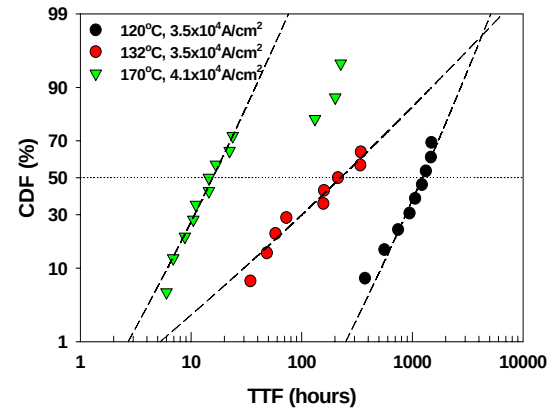


Figure 4. Statistical distribution of electromigration lifetime of solder bumps

Table 2 EM lifetime statistics parameters

Temperature (°C)	Current Density j (10^4 A/cm^2)	t_{50}	σ
120	3.5	1879	0.78
132	3.5	583	1.66
170	4.1	25.1	0.87

Discussion

From Table 2, it can be seen that the standard deviation, σ , of t_{50} ranged from 0.78~1.66. Standard deviation obtained from EM studies on other solder alloy systems showed a range from 0.4~1.3 [9-11]. The values are significantly higher than those measured in chip-level Cu or Al interconnects which are typically 0.2~0.3. A large σ will considerably reduce the extrapolated lifetime. For example, the extrapolated 0.01% lifetime, $t_{0.01}$, reduces from 33% to only ~0.2% of t_{50} when σ increases from 0.3 to 1.66. Therefore, the source of the standard deviation needs to be understood for proper lifetime prediction.

Extrinsic Factors

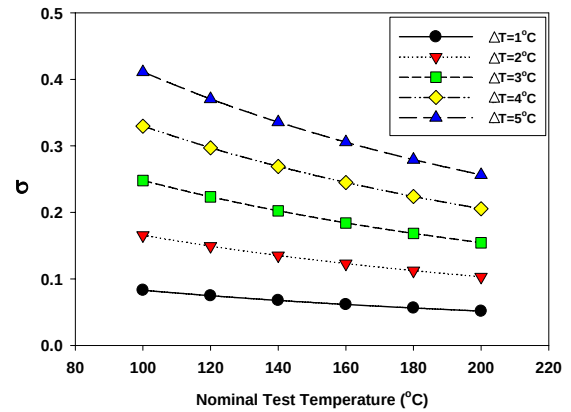
The experimental setup and manufacturing process of the samples can introduce a large magnitude of deviation in the lifetime data. However, such variations can be readily removed or minimized once the source is known. In solder EM studies, two factors have the most direct impact on lifetime, namely the testing temperature and current density.

Temperature: For back end of the line (BEOL) interconnect EM tests, the test current is relatively low, in the range of 1mA, and heat dissipation is on the order of milli-watts. The Joule heating-induced temperature difference between samples is less than 1°C with little convection in the atmosphere. In solder EM test, due to the large current (~1A), the heat dissipation is in the order of Watts. Furthermore, all the heat is generated in an area containing just a few bumps. Consequently, the observed temperature variation between samples can be 5°C or more, even with precautions including forced air convection and external heat sink. The induced σ by the temperature difference can be estimated as:

$$\sigma = \frac{Q}{k} \left(\frac{1}{T} - \frac{1}{T + \Delta T} \right) \quad (5)$$

where Q is the activation energy in eV, k is the Boltzmann's constant, T is the test temperature and ΔT is the maximum temperature difference between samples. Figure 5 illustrates the change of σ with test temperature and the temperature difference between samples. From Figure 5, it is estimated that the σ induced by 5°C temperature differences is 0.29~0.38 in this study.

Decreasing the test current is the most direct and effective way to reduce the variation in σ induced by temperature since the power dissipation decreases parabolically with current. However, it also means that the test time will be elongated due to lower current density. A trade-off needs to be made to minimize σ while maintaining reasonable test duration.

**Figure 5. Temperature effect on standard deviation**

Current Density: In solder EM test, the current supplied to the all test structures is normally very stable with a variation lower than 1%. Nonetheless, the current density may vary considerably in critical area from sample to sample due to the current crowding effect. As shown in Figure 6, electron current divergence occurs when the electrons flow in the thin film interconnects on the die side and approaches the edge of solder bump. The electrons enter the solder bump at the passivation opening edge, creating a localized high current density which is much higher than the nominal current density in the bump. This phenomenon is called current crowding. The magnitude of the current crowding is mainly affected by the thickness of the thin films (interconnect in the silicon chip and UBM) adjacent to the bump. The thinner the films are the larger the crowded current density will be. In this study, the thin film in contact with the bump was the electroplated Ni, whose thickness varied from 1~3 μm with an average of 2 μm .

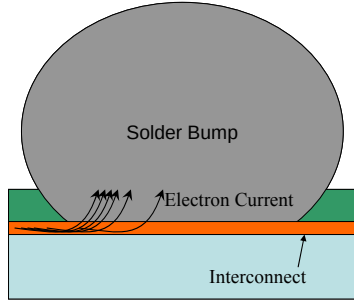
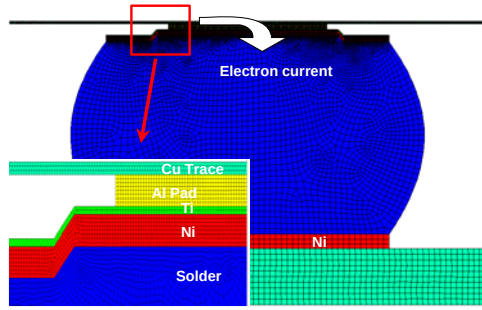
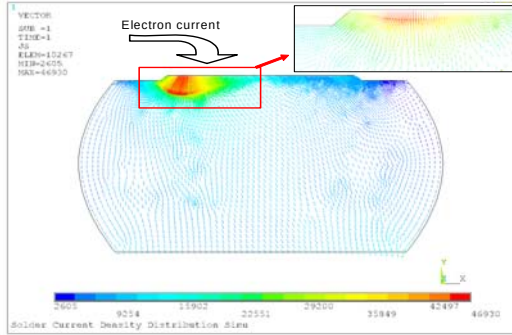


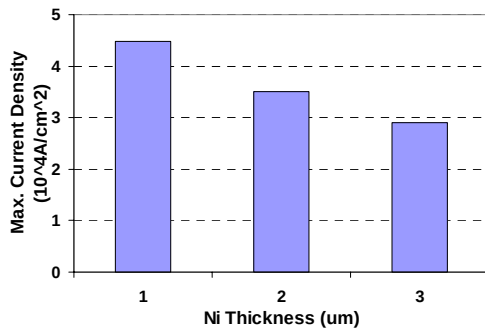
Figure 6. Current flow pattern at the solder-interconnect interface



(a)



(b)



(c)

Figure 7. FE model and current distribution of the solder bump

To estimate the current density variation induced by current crowding, finite element analysis was conducted. Two-dimensional finite element models were built as shown in Figure 7(a). The simulation results of the current distribution in the solder bumps are shown Figure 7(b). As the results show, the current crowding region was very close to the edge of the passivation opening where the current deviated from the interconnect line into the solder. The current density in the current crowding region was about 4~5 times higher than the average density.

Figure 7(c) plots the maximum current density, j_{max} , in the solder bump as a function of Ni thickness. It is clear that j_{max} substantially decreased substantially as the Ni thickness increased. As a result, the j_{max} in the solder bump with 1 μ m of Ni UBM was found to be 54% larger compared with those with 3 μ m of Ni UBM. This corresponded to 137% difference in expected EM lifetime. The induced σ is 0.43.

Failure Mode: In Figure 4, there seemed to be two groups of failures in tests at 132 and 170°C with one showing shorter lifetime than the other. It was suspected that a bimodal EM failure might exist in this case. Bimodal failure has been used to describe the extrinsic early failures in the Cu interconnect electromigration tests [12-15]. The total probability density function for a bimodal failure is

$$pdf = xpdf^{ex} + (1 - x)pdf^{in} \quad (6)$$

where pdf_{ex} and pdf_{in} are the probability function of the two failure modes, extrinsic and intrinsic. The failure in the extrinsic mode is normally induced by process defects that facilitate the EM damage evolution. Usually, the proportion of the early failures is quite small, only a few percent of the population since this mode is 'abnormal'. In this study, however, the percentage of each failure mode is comparable. For that reason, we would rather call it 'alternative failure mode'. The data was then fitted with bi-lognormal distribution as shown in Figure 8 and the parameters are listed in Table 3.

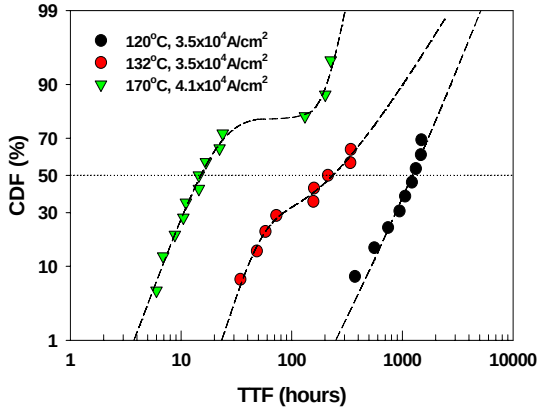


Figure 8. EM lifetime statistics with bi-lognormal distribution

Table 3 Lifetime statistics with bimodal failure

T (°C)	j (10 ⁴ A/cm ²)	Mode 1		Mode 2		Mode 1 Percentage
		t ₅₀	σ	t ₅₀	σ	
120	3.5	n/a	n/a	1879	0.78	0
132	3.5	47.7	0.36	683	1.15	14%
170	4.1	14.7	0.57	240	0.3	54%

After fitting the data to bimodal distribution, the standard deviation is largely reduced. The origin of the bimodal behavior may be accounted to the different failure modes. Previous work has shown that the damage mechanism may change with temperature [3].

Intrinsic Factors

The electromigration is fundamentally a diffusion phenomenon driven by electron current. The diffusion process in solder EM is much more complicated than that in interconnect EM since flip-chip solder bump is a complicated metallurgical system with multiple components such as UBM (metal multi-layer thin films), solder alloy (binary or ternary) and intermetallic compound (IMC).

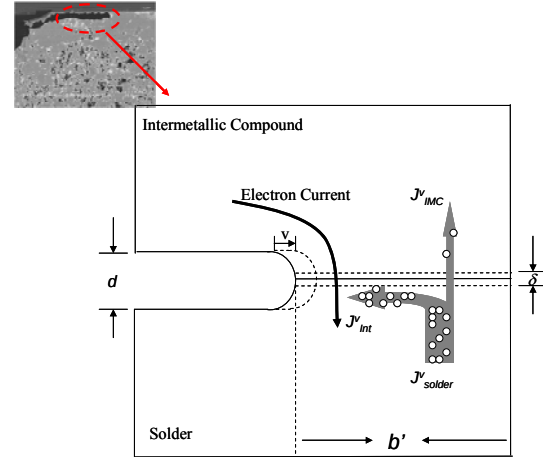


Figure 9. Pancake-shape crack growth at the UBM/solder interface

A lot of work has shown that the failure normally occurs at the interfaces of the above constituents [1-4, 8-11]. Zhang *et al* proposed a model to describe the propagation of a pancake-shape void along the Cu UBM-Sn solder interface under the influence of electron current, as shown in Figure 9 [16]. The void growth was supported by the vacancy flux along the interface, J_{int}^v , which is the difference between the vacancy flux in the solder, J_{solder}^v , and in the IMC, J_{IMC}^v . The growth rate of the void can be estimated as

$$v = \frac{ej}{kT} (D_{solder} Z_{solder}^* \rho_{solder} - D_{IMC} Z_{IMC}^* \rho_{IMC}) \frac{b'}{d} \quad (7)$$

where D_{solder} and D_{IMC} are the diffusivity of Cu in the solder and IMC, Z_{solder}^* and Z_{IMC}^* are the effective charge numbers, ρ_{solder} and ρ_{IMC} are the densities. While Z^* and ρ are relatively fixed with given material, the diffusivity D are more likely to be affected by the microstructure. For example, the grain size of Cu-Sn IMC and bulk Sn may both change considerably within the temperature range and time frame of the EM test due to the fast reaction between Cu and Sn as well as the re-crystallization temperature of Sn. The grain size change will affect the ratio of grain boundary to bulk grain and thus affect the diffusion behavior. Furthermore, both the Sn-Cu IMC and Sn have anisotropic crystal structure. The diffusivity along different directions in the grain is quite different. Warburton *et al* reported that the diffusivity of Cu in Sn can be orders of magnitude different along a and c axis of Sn (Figure 10) [17]. With the continuing shrinkage of bump size, there will be fewer and fewer grains in the bump and the

bump will become more and more anisotropic. Report [18] has shown that bumps may not have the same crystal orientation even within the same package. Therefore, the variation in EM lifetime induced by microstructure difference may not be negligible.

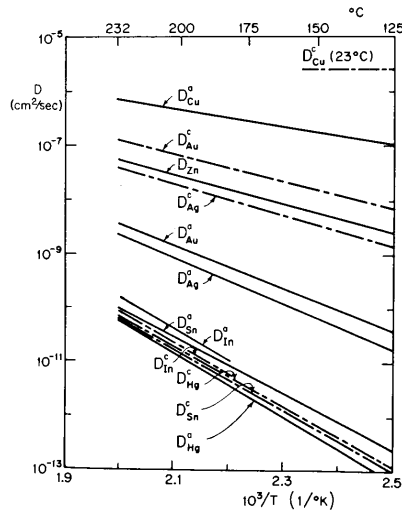


Figure 10. Diffusivity of various elements in Sn

Conclusions

In this study, a case study was carried out to investigate the origin and estimate the level of standard deviation of EM lifetime statistics. Lifetime data was obtained from a flip chip solder system with Ni UBM and SnAg solder. The standard deviation under various test conditions was found to be 0.78~1.66 which is significantly larger than that of interconnects. The impact of three extrinsic factors, temperature, current density and failure mode were discussed. The temperature difference between the samples was measured to be at least 5°C due to Joule heating effect and the induced σ was estimated to be 0.29~0.38. The current density was found to be greatly affected by the Ni thickness due to current crowding effect and could induce a σ of 0.43. The strong sensitivity of current density to the structural parameters of the solder bump system suggested that the statistics of solder EM may depend extrinsically on the design of products and manufacturing process of the silicon. The impact of the intrinsic factors such as grain size and crystal structure on the EM damage evolution was discussed qualitatively as well. Understanding of the sources of the variation will help to minimize the extrinsically induced variation and improve solder EM performance.

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