

Modification to Darveaux Solder Joint Fatigue Life Prediction Method for Flip-Chip Solder Joints

Bahareh Banijamali and Ilyas Mohammed

Tessera
3099 Orchard Dr.
San Jose, CA 95134
bbanijamali@tessera.com

Abstract

For decades, BGA solder joint fatigue in thermal cycling has been studied by different researchers. Finite element modeling techniques have been used for years to calculate inelastic strain energy accumulated during thermal cycling. Fatigue life prediction methods then are used to measure and predict accumulative fatigue. For years, different stress-based, strain-based, damage accumulation-based, inelastic energy-based theories were proposed and studied by researchers. Robert Darveaux proposed a damage accumulation-based inelastic energy-based theory in 2000 that is being commonly used in industry. Darveaux method measures number of cycles for cracks to initiate and propagate through the joint based on average inelastic energy density accumulated during thermal cycling. However, crack initiation and crack growth constants he calculated are for BGA joints.

In this paper, Darveaux fatigue life prediction method is modified for flip-chip solder joints where solder joints are smaller with finer ball pitches, and Darveaux constants for BGA solders can not be applied. Furthermore, this modification is detailed and illustrated on Tessera's 130um bump pitch flip-chip package comparing solder fatigue life for solder-only, C4-bump and μ PILRTM flip-chip technologies.

Keywords: μ PILRTM, copper micro pins, flip-chip, pitch.

Introduction

Flip-chip technology has been introduced in recent years to address the need for tighter and tighter pitches which allow for ever increasing I/O density in smaller and smaller footprints. For flip-chip assembly, a large coefficient of thermal expansion (CTE) mismatch between die and package induces device bending and high stress to interconnect layers through the bumps. Underfill has been employed to decrease the thermal stress caused by CTE mismatch and to improve solder bump reliability.

A C4 bump process has historically served as the main interconnect method in flip-chip packaging. The minimum flip-chip C4 bump pitch used in industry recently is 150um and 200um. But with bump pitches shrinking, the solder bump based C4 process faces challenges in terms of reducing both the pitch and the underfill process. Tessera μ PILRTM copper pins provide an alternative flip-chip interconnect method. A schematic picture of flip-chip package using μ PILR is shown in Figure 1 [1-7].

Solder joints and interconnects connecting μ PILR packages to Si, PCB boards or to other packages (PoP) are susceptible to breakage from solder fatigue or brittle fracture. Fatigue mechanism is dominant in temperature cycling or cyclic bending when there is fatigue accumulation. Brittle fracture is caused by extreme bending or impact in drop which is the primary concern in hand-held devices especially for lead free solders (lead free solder materials have better performance in temperature cycling while being more brittle and stiff in drop).

BGA solder joint fatigue in thermal cycling has been studied by different researchers. Finite element modeling techniques have been used for years to calculate inelastic strain energy accumulated during thermal cycling. Fatigue life prediction methods then are used to measure and predict accumulative fatigue. For years, different stress-based, strain-based, damage accumulation-based, inelastic energy-based theories were proposed and studied by researchers. In 2000, Robert Darveaux proposed a damage accumulation-based inelastic energy-based theory that is still commonly in use by industry [8-12]. The Darveaux method measures the number of cycles

necessary for cracks to begin and spread through the joint based on average inelastic energy density accumulated during thermal cycling. However, the crack initiation and crack growth constants he calculated are for BGA joints.

In this paper, the Darveaux fatigue life prediction method is modified for flip-chip solder joints, where the solder joints are smaller with finer ball pitches, and the Darveaux constants for BGA solders are not applicable. Instead, modified crack initiation and growth constants are proposed for flip-chip solder joints. Furthermore, the Darveaux constants were modified and applied to Tessera uPILR flip-chip solder joints, which are formed through a combination of copper pins and solder. This modification is detailed and illustrated on a 130um bump pitch flip-chip package. Finally, solder fatigue life for solder-only, C4-bump and uPILR flip-chip technologies are compared.

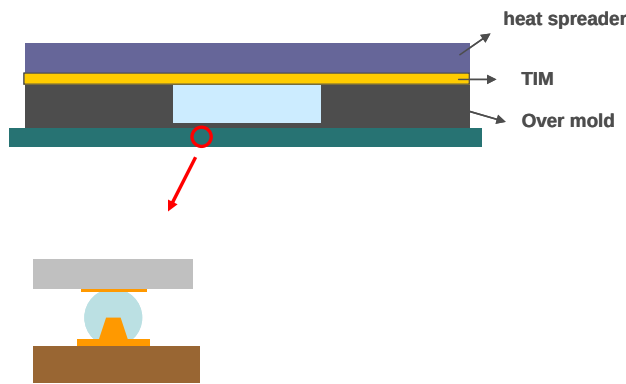


Figure 1. Schematic of flip-chip package configuration

Flip-chip modeling and simulation

The 40x40mm package shown in Fig 1 is considered, and includes a 20x20x0.75mm die, a 40x40mm thin substrate with a thickness of 0.255mm. A cover lid is attached on top of die and over mold by a thermal interface (TIM). Flip-chip interconnect consists of μ PILR copper bumps and lead-free solders shown in Figure 2 and has bump pitch of 130um. Package attributes are given in Table 1.

3D models are constructed using the commercial software ABAQUS to perform the package thermo-mechanical simulation and analysis. Owing to the symmetry of the package, only one quarter of the package is modeled to increase computational efficiency and decrease cost. The package is assumed to be stress-free at over mold cure temperature of 165C. Furthermore, sub-modeling

technique is used. A detailed model for the copper bumps, solder masks, solders, copper pads and low-k dielectric material greatly affects the accuracy and rate of convergence of the solution. Therefore, detailed local models are solved at selected locations on the global model.

Table1. Attributes used for flip-chip simulation

Feature	Dimensions (mm)
package	40x40
die	20x20x0.75
substrate	40x40x0.255
TIM	40x40x0.05
Heat spreader	40x40x1.0

Material properties

Material properties of package compounds, Young's modulus and CTE, are temperature dependent. Table 2 shows these properties at room temperature.

Table 2. Material properties of package compounds at room temperature

Feature	Young's modulus (GPa)	CTE ppm/C°
Substrate dielectric	9.5	19 (T _g =156)
Si	130	2.8
Solder (Sn3.5Ag)	51	22.4
Copper	130	17
UF-1	10	25
Solder mask	2.9	68
OM-1	24.5	10(T _g =148)

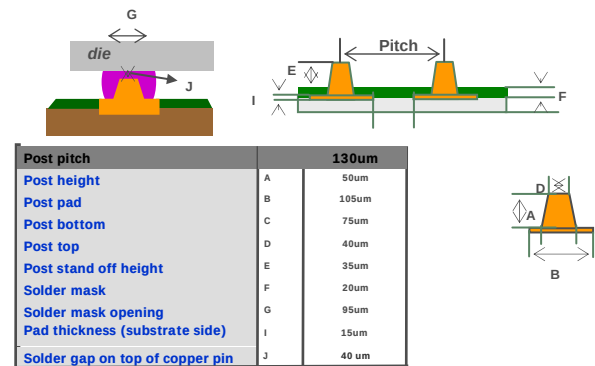


Figure 2. μ PILR attributes used in flip-chip simulation (BP=130 um)

Modified Darveaux fatigue life prediction theory

To predict fatigue life based on simulation, one needs first to calculate inelastic strain energy density per cycle and then use Darveaux fatigue life prediction theory. However, Darveaux fatigue life prediction parameters given in [9] are for board level solders and cannot be employed for smaller size flip-chip solders.

Here, first Darveaux method is explained and then a modification is proposed for flip-chip solders. Following Darveaux theory, after inelastic energy density per cycle is calculated, number of cycles for crack initiation and crack growth rate are calculated using

$$No = K_1 \Delta W_{ave}^{K_2} \quad (1)$$

$$\frac{da}{dN} = K_3 \Delta W_{ave}^{K_4} \quad (2)$$

When ΔW_{ave} is viscoplastic strain energy density per cycle, and K_i parameters are Darveaux parameters given in [9]. A modeling procedure consistent to Darveaux theory should be applied in order to use his fatigue life prediction parameters. Note that, the accuracy of relative predictions is in the range of +/- 25% and the accuracy of absolute predictions could be off by a factor of 7 (in the worst case when modeling procedures inconsistent to Darveaux theory is being applied). In addition, the parameters given are for eutectic solder, and for a lead-free solder, characteristic life will be higher and solder will go through more temperature cycles.

The characteristic life is then obtained by

$$\alpha_w = No + \frac{a}{da/dN} \quad (3)$$

where “a” is the joint diameter at the interface.

As previously discussed, the Darveaux theory needs to be modified for flip-chip solders. Here, a modification is proposed that is still consistent to Darveaux modeling procedures and allow us to use his K_i parameters.

Based on Darveaux theory, the BGA solder with the most fatigue should be meshed to have 3 layers of elements each 0.0005 inch at it's fatigue region (at pad interface for most cases). Then the finite element simulation is applied for 3-4 cycles till growth of inelastic energy is constant and average

viscoplastic energy density per cycle is calculated for elements in fatigue region (2 or 3 rows of elements with 0.0005inch thick each) using

$$\Delta W_{ave} = \frac{\sum \Delta W \cdot V}{\sum V} \quad (4)$$

Where ΔW_{ave} is the average viscoplastic strain energy density accumulated per cycle, ΔW is each element's viscoplastic strain energy density accumulated per cycle and V is the volume of each element [9]. ΔW_{ave} is then used in Equations (1-2) to calculate number of cycles for crack initiation (No) and crack growth rate (da/dN).

For smaller size flip-chip solders where solder height is small, meshing the region with most fatigue to have 3 layers of elements each 0.0005 inch is not accepted (it's too big and almost includes 1/2 or 1/3 of the whole solder). Therefore Darveaux theory needs to be modified.

Here, we propose a modification based on still using Darveaux K_i parameters but following the following steps:

1. The flip-chip solder with the most fatigue is meshed to have 3 layers of elements at it's fatigue region, each layer should have thickness of

$$t_{FC} \approx 0.0005'' \cdot \frac{h_{FC}}{h_{BGA}} \quad (5)$$

2. Finite element simulation is applied for 3-4 cycles till growth of viscoplastic energy is constant. Average viscoplastic energy density per cycle is calculated for elements in fatigue region (2 or 3 rows of elements with t_{FC} thick each) using equation (4).
3. Modified viscoplastic energy is calculated using

$$(\Delta W_{ave})_{mod} = \Delta W_{ave} \cdot \frac{t_{FC}}{t_{BGA}} \quad (6)$$

4. The same K_i parameters given for BGA balls are used [9]. Only note that the 0.0005'' thick element in [9] is equivalent to 3 layers of elements, each t_{FC} thick, for flip-chip solder.
5. Crack initiation and crack growth rate are calculated using $(\Delta W_{ave})_{mod}$ in equations (1-2).
6. The characteristic life is then obtained using equation (3).

Note that the parameters given are for eutectic solder, and the accuracy of relative predictions is in the range of +/- 25% and the accuracy of absolute predictions could be off by a factor of 7 (if modeling procedures is inconsistent to what is proposed here), numbers given for absolute prediction should be carefully used. For lead-free solder, characteristic life will be higher and solder will go through more temperature cycles.

Next the Modified Darveaux theory is applied to the flip-chip package shown earlier.

Simulation and results

In this section, we use the Modified Darveaux theory to compare solder fatigue and characteristic life of solder for a variety of package interconnect solder joint technologies shown in Figure 3; μ PILR with solder bump die, μ PILR with Cu pillar bump die and solder-only joints. The sub-modeling technique is used and both global and local models are shown in Figure 5. Detailed local models include 2x2 ball pitch portion of the package at package corner and stresses, inelastic strains and energy are obtained after cooling down package from over mold cure temperature 165C to room temperature and through temperature cycles of -55C/+125C. The package is assumed to be stress-free at 165C.

This study focuses only on the application of Modified Darveaux fatigue life prediction theory and compares solder fatigue for μ PILR with solder bump die, μ PILR with Cu pillar bump die and solder-only joints in thermal stressing.

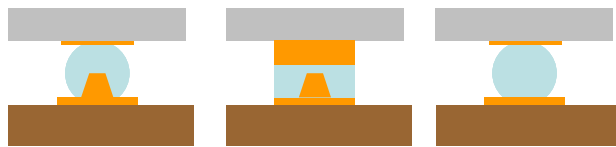


Figure 3. μ PILR with solder bump die, μ PILR with Cu pillar bump die and solder-only joints used in flip-chip simulation (BP=130 μ m).

The results in Table 3 indicate that adopting μ PILR with solder bump die flip-chip technology creates less solder inelastic strain and fatigue than μ PILR with solder bump die joints. Although applying C4-bump helps decrease stress in solder, rate of fatigue growth is still higher for μ PILR with solder bump die technology. μ PILR with solder bump die solder and solder-only joints go through similar inelastic strains and energy, and have comparable reliability in thermo cycling. Although,

the presence of the μ PILR pin has an insignificant effect on the interconnect strain in temperature cycling, it does enable higher density PCB routing, finer pitch capability and lower profile vs. traditional flip-chip technologies.

Furthermore, solder fatigue life prediction was performed where solder bump reliability was compared using the Modified Anand solder material properties and the Modified Darveaux fatigue life prediction theory. Fatigue region used in the fatigue life prediction is shown in Figure 4 for each type of flip-chip technologies where “a” is the joint diameter at fatigue interface (final crack length).

For example for μ PILR flip-chip technology shown in Figure 3, solder ball height is 90 μ m and is meshed to have three layers of elements, each 0.005mm thick at it's fatigue region. From Finite element simulation,

$$\Delta W_{ave} = (W_{ave})_{3rd-cycle} - (W_{ave})_{2nd-cycle} = 72.67 \text{ psi}$$

Modified viscoplastic energy is then calculated using

$$(\Delta W_{ave})_{mod} = \Delta W_{ave} \cdot \frac{0.005}{0.0127} = 28.61 \text{ psi}$$

K_i parameters from Darveaux fatigue life prediction theory [9] are $K1=71000$ (cycles/psi^{K2}), $K2=-1.62$, $K3=2.76$ (10^{-7} in/cycles.psi^{K4}) and $K4=1.05$. Note that three layers of elements for μ PILR flip-chip solder at fatigue region are 0.015mm which is equivalent to one layer of elements in [9]. Finally Crack initiation and crack growth rate are 310 (cycles) and $93.367e-7$ (in/cycles) respectively using $(\Delta W_{ave})_{mod}$ in equations (1-2). The characteristic life is 1010 (cycles) by using equation (3) where “a” is the joint diameter at the interface as shown in Figure 4.

Table 4 lists the eutectic solder characteristic life for each type of flip-chip technologies. Although these numbers are for eutectic solder but they could still be used as a measure to compare solder fatigue life and fatigue growth for lead free solders for each type of flip-chip technologies. Note that the accuracy of relative predictions using Darveaux theory is in the range of +/- 25%. Table 4 shows that μ PILR with solder bump die solder will withstand more thermo cycles than μ PILR with Cu pillar bump die solder. Experimental reliability data is not complete at this time but will be available and published soon.

Table 3. Maximum inelastic strains and energy in solder after cooling down the package from over mold cure temperature of 165C to room temperature and after temp cycles of -55/+125 C (BP=130 μ m).

	Max plastic strain @ -55C	Max plastic strain @ 125C	Max plastic strain @ -55 C	Max plastic strain @ 125C	Max plastic strain @ -55 C	Max plastic strain @ 125C
μ PILR with solder bump die	0.0159	0.0385	0.0569	0.0828	0.1069	0.1331
Solder-only	0.0165	0.0288	0.0517	0.0773	0.1000	0.1255
μ PILR with Cu pillar bump die 24 μ m solder tip 34 μ m Cu-post	0.0063	0.0644	0.0962	0.1368	0.1761	0.2167

	Max plastic energy @ -55C	Max plastic energy @ 125C	Max plastic energy @ -55 C	Max plastic energy @ 125C	Max plastic energy @ -55 C	Max plastic energy @ 125C
μ PILR with solder bump die	0.824	1.575	2.287	3.154	4.00	4.939
Solder-only	0.856	0.663	1.195	2.085	2.836	3.762
μ PILR with Cu pillar bump die 24 μ m solder tip 34 μ m Cu-post	0.341	0.220	0.992	1.572	3.597	4.635

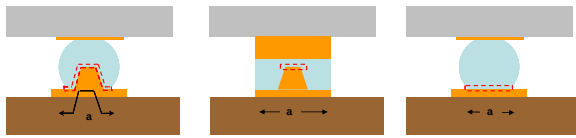
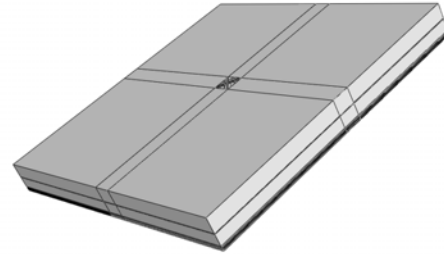


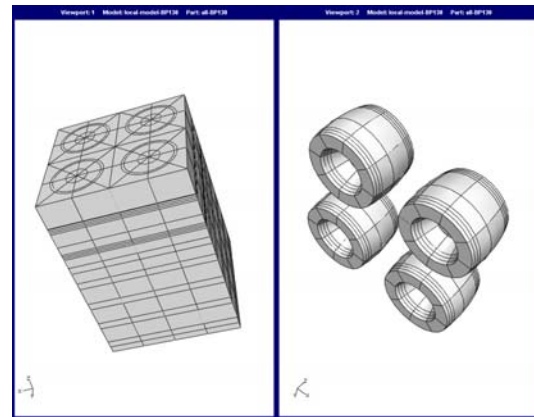
Figure 4. Fatigue region used in Darveaux fatigue life prediction for each type of flip-chip technologies where “a” is the joint diameter at fatigue interface (final crack length).

Table 4. characteristic life of eutectic solder after cooling down the package from over mold cure temperature of 165C to room temperature and after temp cycles of -55/+125 C (numbers given are for eutectic solder only, Sn3.5Ag will stand more cycles). The accuracy of relative predictions using Darveaux theory is in the range of +/- 25% and absolute predictions could be off by a factor of 7.

	Number of cycles till crack starts	Crack growth per cycle (u.in/cycle)	Characteristic life for Eut (cycles)
μ PILR with solder bump die	310	9.34	1010
Solder-only	1079	4.16	1985
μ PILR with Cu pillar bump die 24 μ m solder tip 34 μ m Cu-post	88	21.18	364



(a)



(b)

Figure 5. (a) Global model includes only one quarter of the package, and the local model region is partitioned in the global model; (b) Local model includes 2x2 ball pitch portion of the package at package corner

Conclusions

Darveaux fatigue life prediction theory was modified for flip-chip solders. In addition, solder reliability and fatigue life for three different flip-chip technologies; Tessera μ PILR flip-chip technology with solder bump die, μ PILR with Cu pillar bump die and solder-only joints were studied and compared. Results show that μ PILR with solder bump die, creates less solder inelastic strain and fatigue than μ PILR with Cu pillar bump die solder joints. For given package attributes, μ PILR with solder bump die and solder-only joints go through similar inelastic strain and energy, and have comparable reliability in thermo cycling. Although, the presence of the μ PILR pin has an insignificant effect on the interconnect strain in temperature cycling here, it does enable higher density PCB

routing, finer pitch capability and lower profile than traditional flip-chip technologies.

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