Drop Impact Dynamic Response Study of JEDEC JESD22-B111 Test Board

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Abstract

Mobile and handheld electronic devices are prone to being dropped. This drop event may result in failure of solder joints inside these devices. The need for RoHS compliant boards coupled with the demand for reliable electronics has resulted in the development of the JEDEC Standard JESD22-B111 to standardize the method of drop testing surface mount electronic components. However, there has been little study on the effects of additional mass on the board and rigidity of the board on drop test reliability. This paper examines the drop impact dynamic responses of the JEDEC JESD22-B111 board. Of interest are the effects of an attached cable and rigidity of the board on the peak acceleration at different locations of the board. Fifteen 0.5 mm pitch CSPs were assembled on the board using $SnAg_{3.0}Cu_{0.5}$ *lead free solder. The drop test was conducted using a Lansmont M23 TTSII Shock Test system. A half-sine shock impact pulse of 1500 G with 0.5 ms duration was applied to the drop table where the test vehicle was mounted. Two accelerometers were used to monitor the peak acceleration with one placed on the drop table and the other on the board at the component location. Statistical analysis showed that both the rigidity of the board and a cable attachment have an effect on the peak acceleration at individual component locations. Results show that the peak acceleration differs significantly at different component locations and the peak acceleration at some component locations are much higher than on the drop table. A cable attached to the board is shown to influence both peak acceleration and symmetry. A correlation between the peak acceleration and the number of drops until component failure was assessed.*

Keywords: Drop test, acceleration, dynamic response, reliability, lead free solder

1. Introduction

Handheld electronic devices are becoming ubiquitous across the world. These devices, such as cellular phones, personal digital assistants (PDAs), and MP3 players are prone to be dropped in the device's usable lifetime. This drop event may lead to full or partial failures of the solder joints inside the device. Recently the European Union (EU) Restriction of Hazardous Substances (RoHS) and other countries' lead-free directives banned the use of lead in consumer electronics products. Among those developed lead-free solder materials, SnAgCu alloy was considered by the electronics industry to be the standard alternative to eutectic tin-lead solder [1].

There has been a significant amount of research done in the last few years on drop impact reliability [2, 3]. The JEDEC standard JESD22-B111 [4] for the board level and related standards [5, 6] for subassembly level have been developed for handheld electronics drop testing. Much research has been dedicated to dynamic responses such as strain conditions [2, 7, 8] and validating finite element analysis (FEA) and numerical models [7, 9, 10]. In drop impact studies, an accelerometer was typically placed on the drop test table [8, 11] to monitor peak acceleration and duration of the impact pulse or on the center of a test board to measure board-level acceleration pulse [12, 13]. However, the dynamic board response at all component locations has not been adequately studied.

The rigidity of the test board and how the board was mounted on the drop table may significantly affect the peak acceleration at the component level given the same input pulse on the drop table. There has been little study on the effects of additional mass due to a cable attachment and/or the rigidity of the board on drop test reliability. The purpose of this study is to investigate the effect of an attached cable and the rigidity of the board on the peak acceleration at different component locations of a JESD22-B111 compliance test board. A correlation between the peak acceleration and the number of drops-to-failure was assessed.

2. Design

Experiments were designed to investigate the effects of two different input factors on the peak acceleration at different locations of a test board. The input factors were: 1) with or without a cable attached to the board, and 2) the rigidity of the board. No cable is attached to the board during the drop testing if the post-drop resistance measurement method [14] is used to detect failure of solder joints, whereas a cable is attached in the in-situ high-speed data acquisition method [13] or the event detection method [15]. At the treatment of with a cable, the cable was connected to the test vehicle by soldering individual wires directly into plated through-holes on the short side of the board.

The rigidity of the board has four levels: 1) blank board, 2) populated board with no edge-bond, 3) populated board with acrylic edge-bond, and 4) populated board with epoxy edge-bond. The blank board means a bare board without components assembled. The populated board with no edge-bond means a board with components assembled, but no edge bonding applied. The components, the test vehicle, and edge bond materials were the same as used in our previous study [1]. Figure 1 shows an example of an edge-bonded Chip Scale Package (CSP).

Figure 2 shows the drop test setup. The test vehicle was mounted in a horizontal position with the components facing downward, which is the most severe orientation [9]. Fifteen 0.5 mm pitch CSPs were assembled on a JESD22-B111 compliance test board using Sn3.0Ag0.5Cu lead free solder. The test board is an eight-layer FR4 material board with a size of 132 mm by 77 mm and a thickness of 1 mm.

The drop test was conducted using a Lansmont M23 TTSII Shock Test system. A half-sine shock impact pulse of 1500 G with 0.5 ms duration was applied to the drop table where the test vehicle was mounted. Two accelerometers were used, with one accelerometer placed on the drop table to monitor the peak acceleration and duration of the input pulse, and the other on the component location to measure peak acceleration at that location as shown in Figure 2.

There are 15 component locations on a board. The peak acceleration at each location was measured. Thus, there are 120 treatments total (2 levels of the use of cable times 4 levels of board rigidity times 15 component locations). Each experimental treatment was replicated twice. Therefore, a total of 240 drops were conducted. To reduce the expected degradation effect on the board rigidity due to continued bending, eight boards were used in this experiment, two for each level of board rigidity. The order of testing with and without cable was alternated between the two boards for each rigidity level.

Figure 1: An example of an edge-bonded CSP.

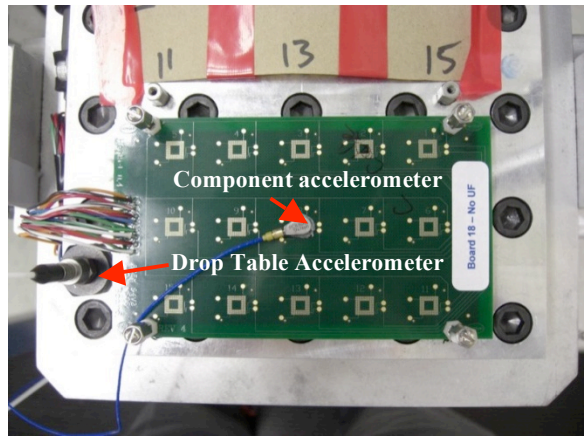

Figure 2: Test vehicle with one accelerometer on a component location and the other on the drop table.

3. Data Analysis

3.1 Local Acceleration Results

Figure 3 shows an example of the acceleration responses of both the drop table and a component location at the test vehicle during a 1500 G drop. The half-sine response was that of the drop table, and the larger cyclic response was a component location at the test vehicle. It is clearly shown that the acceleration experienced by the test vehicle was completely different from that at the drop table. The test vehicle vibrated after the impact and experienced higher peak acceleration than the drop table. The peak acceleration at the test vehicle occurred at a later time than at the drop table.

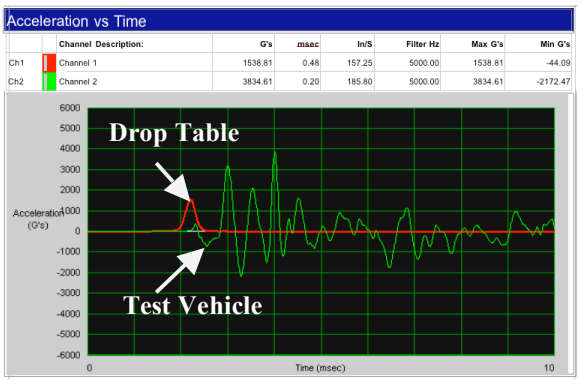

Figure 3: Dynamic acceleration responses of drop table and test vehicle.

An overview of the placement of each component on the board in relation to the cable is shown in Figure 4. The average peak acceleration at the 15 component locations for blank board, populated board with no edge-bond, populated board with epoxy edge-bond, and populated board with acrylic edge-bond are shown in Figures 5 - 8, respectively. The peak acceleration of each component location without a cable attached is shown in the left side and the peak acceleration with a cable is shown in the right side of Figures 5 – 8. A bold horizon line in these four figures represents the input acceleration of 1500 G. The results indicate the significant effect of the cable on local accelerations. In every case, the cable reduces the overall peak acceleration and disrupts symmetry. The reduction of the peak acceleration may be due to the additional mass from the cable. The mass of the attached cable also shifts the center of mass of the test board, which disrupts the symmetry of acceleration behavior. It is also evident that the populated boards experience less acceleration than the blank board due to increased rigidity and mass.

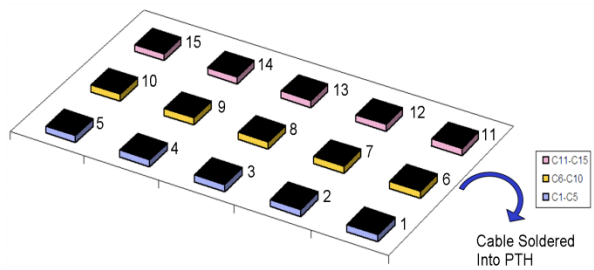

Figure 4: Cable in relation to component locations.

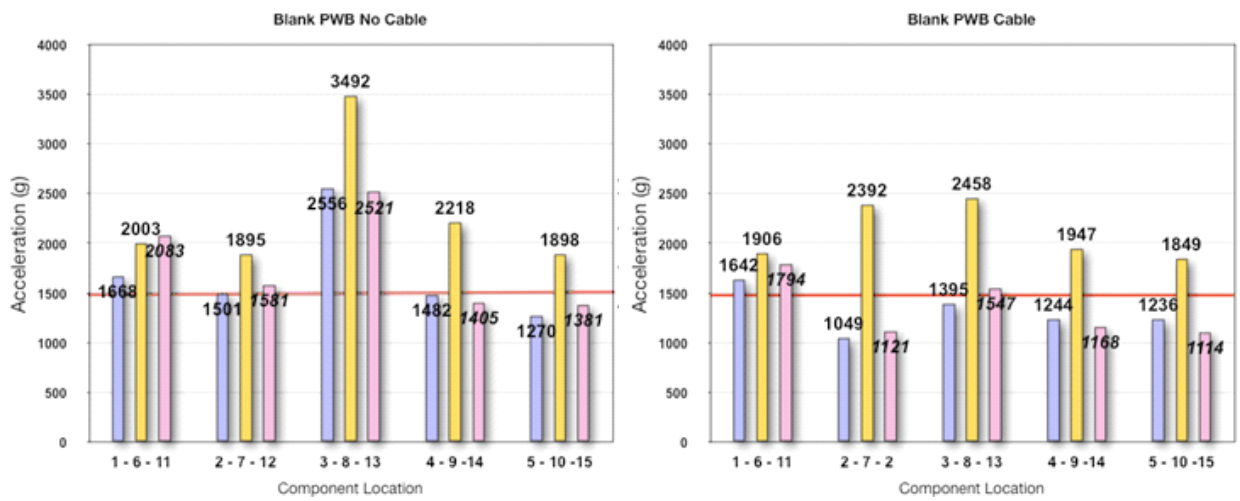

Figure 5: Accelerations on blank board with no cable and with cable.

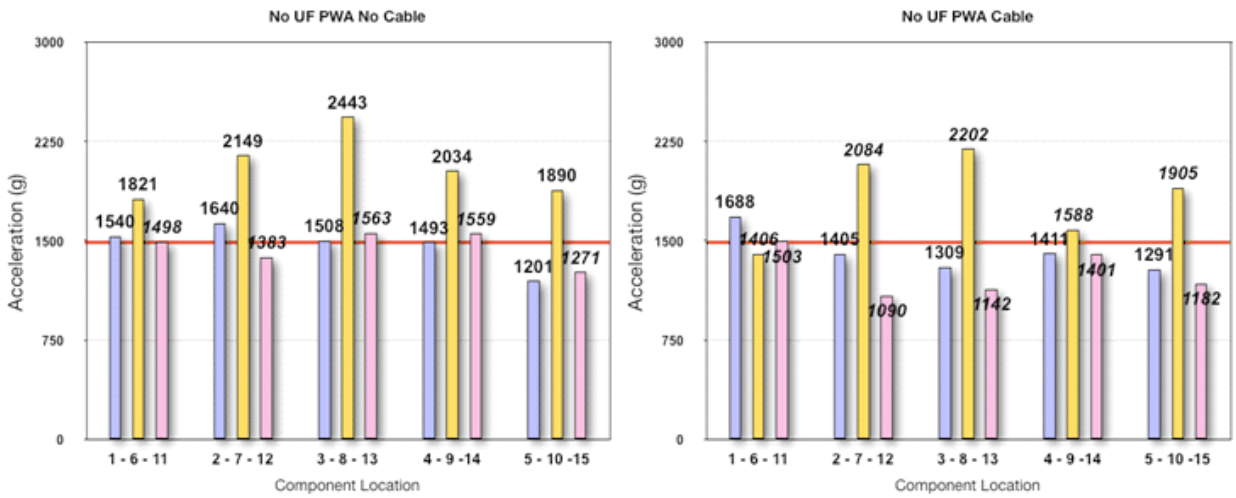

Figure 6: Accelerations on populated board with no cable and with cable.

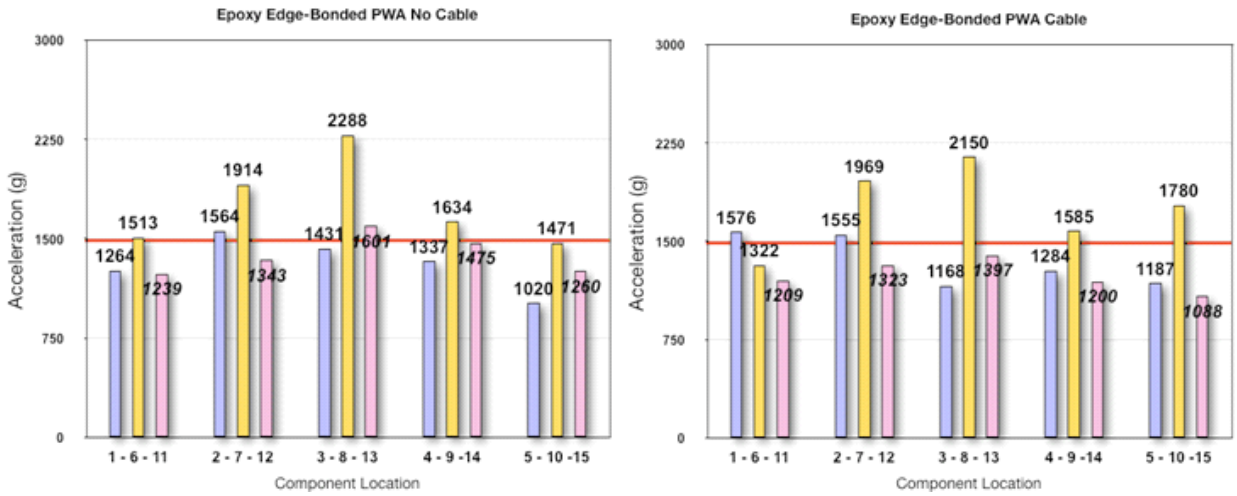

Figure 7: Accelerations on epoxy edge-bond populated board without cable and with cable.

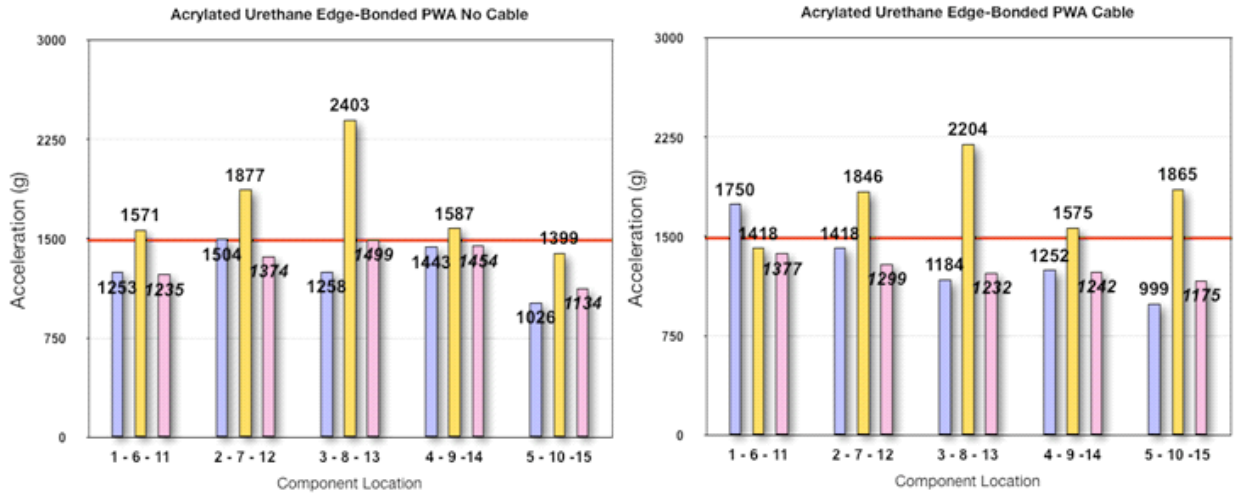

Figure 8: Accelerations on acrylic edge-bond populated board with no cable and with cable.

3.2 Statistical Analysis

Analysis of variance (ANOVA) was used to determine the effects of a cable and board rigidity on the peak acceleration at individual component locations. Figure 9 shows the effect of the cable. The component locations filled with dark color are the locations in which the cable has a statistically significant effect on peak acceleration on that location. The figure shows that component locations 2, 3, 4, 6, 8, 9, 12, 13, and 14 all experienced significantly different accelerations when a cable was attached compared to when no cable was attached.

Figure 10 shows the effect of board rigidity on the peak acceleration at different locations. It shows that the rigidity of the board has statistically significant effect on locations 3, 6, 8, 9, 11, 13, and 14. In these locations, the populated board experienced significantly less peak acceleration than the blank board. However, there is no statistically significant difference in peak acceleration between the populated board without edge bond and the populated board with edge bond across all tested locations. There is also no significant difference in peak acceleration at every location of the board between the epoxy edge-bond and acrylic edge-bond. Previous studies have found that drop test reliability of solder joints without edge-bond is much poorer than solder joints with edge-bond [1, 14], however, no significant difference exists in peak accelerations between these two cases at any component location.

To understand the effect of a cable and the rigidity of a board on the peak acceleration according to JEDEC defined symmetry group locations, as shown in Figure 11, another ANOVA was analyzed. The peak acceleration at different group locations is shown in Figure 12. It is interesting to note that the group location E has lower peak acceleration than group locations C and D, although JEDEC specifies group location E having greater strain [4].

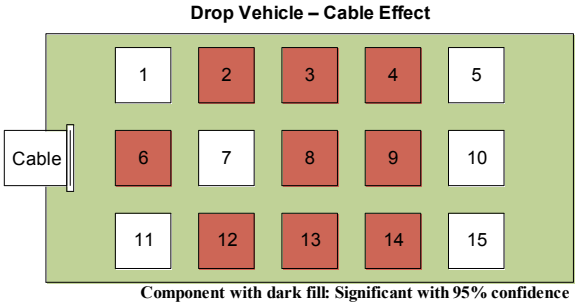

Figure 9: Effect of a cable on peak acceleration of different component locations. The component locations filled with dark color are the locations in which the cable has a statistically significant effect on peak acceleration on that location.

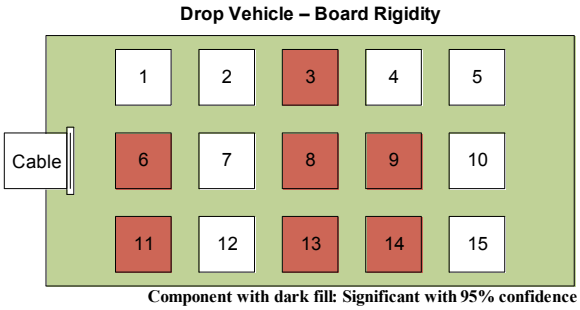

Figure 10: Effect of the rigidity of a board on peak acceleration of different component locations. The component locations filled with dark color are the locations in which the rigidity of a board has a statistically significant effect on peak acceleration on that location.

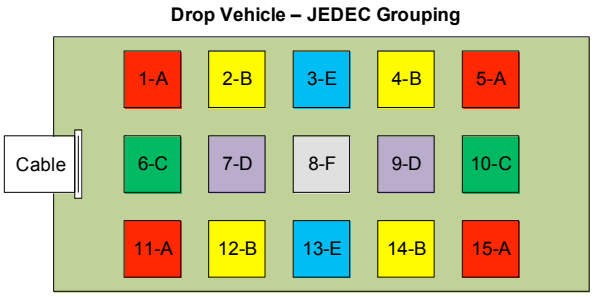

Figure 11: JEDEC defined symmetric component location groups.

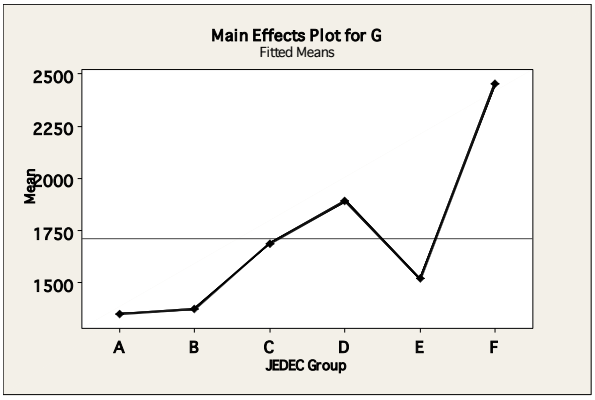

Figure 12: Main effects of peak acceleration by JEDEC board group.

3.3 Relationship between Reliability and Component Location

To assess whether a high peak acceleration results in the failure of solder joints in a drop impact test, the number of drops-to-failure for boards with edge-bonding at each component location group defined by JEDEC [2] was analyzed. All data of

drops-to-failure at each component location have been reported in our previous study [1].

Because many repetitive drops are required to completely fail drop tested devices, many studies stop the drop testing process after a preselected number of failures occur, or after a certain number of drop impacts. Statistically, the data gathered from this testing type is known as right-censored. In the case of reliability analysis with right-censored data, a predetermined number of failures would typically be used to obtain an accurate estimate of a failure trend [16]. In this study, both the censored and non-censored data were analyzed using Minitab's Reliability/Survival Analysis functions. Since the number of drops-to-failure follows the Weibull distribution, cumulative failure plots were generated for both the 1500 G with 0.5 ms duration impact and the 2900 G with 0.3 ms duration impact, as shown in Figures 13 and 14, respectively. Reliability analysis was performed for each component location group based on the JEDEC board grouping (A-F).

Figure 13 shows that group E and F failed at the fastest rate at 1500 G. Note that Group F has a different shape than the other groups. This may be due to a relatively low ratio of failed data to censored data. Groups A, B, C, and D have similar failure rates, with B showing the fastest failure rates of those four component groups. This does not correlate with the peak acceleration experienced by the location of component group. JEDEC group D, which experienced the second highest peak acceleration, had the slowest failure rate in the 1500 G impact. Conversely, JEDEC group E, which experienced relatively low peak acceleration, had the second fastest failure rate in the 1500 G impact. Figure 14 shows a much more consistent pattern of failure rates under 2900 G impact. This is most likely attributed to the higher ratio of failed to censored data. Again, groups E and F have the highest failure rates of all the groups. This analysis indicates that a high local acceleration does not necessarily correlate to a low number of drops-to-failure.

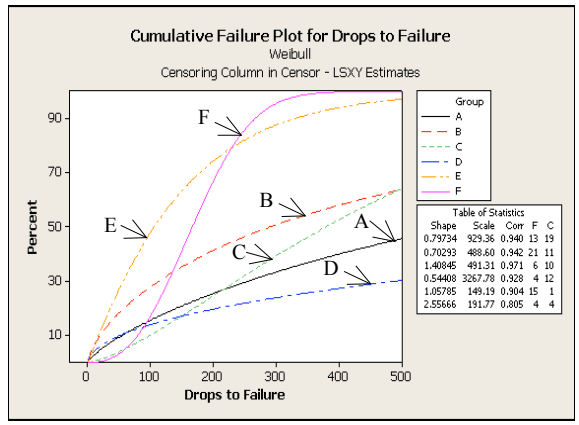

Figure 13: Cumulative failure plot for drops to failure of each group at 1500 G.

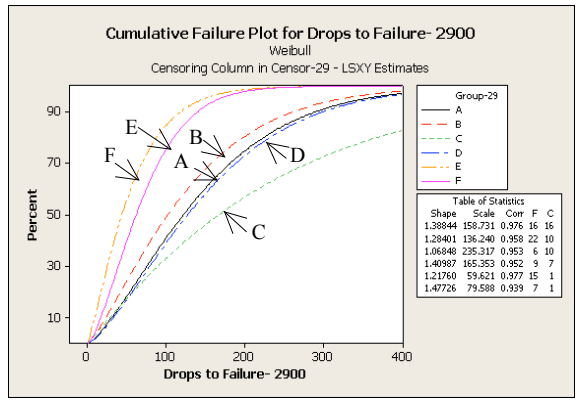

Figure 14: Cumulative failure plot for drops to failure of each group at 2900 G.

4. Conclusions

The following conclusions can be drawn from this research:

1. A cable or other additional mass attached to a drop test board significantly affects the peak value and symmetry of acceleration at many component locations on the board.
2. Higher local peak acceleration does not directly correlate to a lower number of drops-to-failure in that location.
3. The peak acceleration at every component location on the populated board without edge-bond is similar to that on the populated board with acrylic edge-bond or epoxy edge-bond, therefore the board rigidity is similar, but the drop test reliability of solder joints without edge-bond is much poorer than solder joints with edge-bond.

Acknowledgements

The authors would like to thank Mr. Jasbir Bath, Mr. Dennis Willie, Mr. David A. Geiger, and Dr. Dongkai Shangguan of Flextronics, Dr. Brian J. Toleno and Mr. Dan Maslyk of Henkel Technologies

for technical support. The first author gratefully acknowledges the financial support from National Science Foundation through Cal Poly's honors program.

References

[1] A. Farris, J. Pan, A. Liddicoat, B. J. Toleno, D. Maslyk, D. Shangguan, J. Bath, D. Willie, D. Geiger, "Drop Test Reliability of Lead-Free Chip Scale Packages", *Proc. of 2008 IEEE ECTC*, pp. 1173-1180.

[2] Y.S. Lai, P.C Yang, C.L. Yeh, "Effects of Different Drop Test Conditions on Board-Level Reliability of Chip-Scale Packages", *Microelectronics Reliability*, Vol. 48, No. 2, Feb. 2008, pp. 274-281.

[3] J. Zhao, F. Liu, X. Zhou, H. Zhou, J. Jing, M. Zhao, "Improvement of JEDEC Drop Test in SJR Qualification through Alternative Test Board Design," *Proc. of Electronic Components and Technology Conference*, May 2007, pp. 946-950.

[4] JEDEC Standard JESD22-B111, "Board Level Drop Test Method of Components for Handheld Electronic products", JEDEC Solid State Technology Assoc, 2003.

[5] JEDEC Standard JESD22-B104-C, "Mechanical Shock", JEDEC Solid State Technology Assoc, 2004.

[6] JEDEC Standard JESD22-B110A, "Subassembly Mechanical Shock", JEDEC Solid State Technology, 2004.

[7]C.-L. Yeh, T.-Y. Tsai, Y.-S. Lai, "Transient Analysis of Drop Responses of Board-Level Electronic Packages using Response Spectra Incorporated with Modal Superposition," *Microelectronics Reliability*, Vol. 47, No. 12, 2007, pp. 2188-2196.

[8] C.-L. Yeh, Y.-S. Lai, C.-L. Kao, "Evaluation of Board-Level Reliability of Electronic Packages under Consecutive Drops," *Microelectronics Reliability*, Vol. 46, No. 7, 2006, pp. 1172-1182.

[9] J.E Luan, T.Y. Tee, E. Pek, C.T. Lim, Z. Zhong, J. Zhou, "Advanced Numerical and Experimental Techniques for Analysis of Dynamic Responses and Solder Joint Reliability During Drop Impact", *IEEE Transactions on Component and Packaging Technologies*, Vol. 29, No. 3, Sept. 2006, pp. 449 – 456.

[10] E. Wong and Y. Mai, "New Insights into Board Level Drop Impact," *Microelectronics and Reliability*, Vol. 46, No. 5-6, May 2006, pp. 930-938.

[11] Y.S. Lai, P.F. Yang, C.L. Yeh, "Experimental Studies of Board-Level Reliability of Chip-Scale Packages Subjected to JEDEC Drop Test Condition", *Microelectronics Reliability*, Vol. 46, No. 2, 2006, pp. 645-650.

[12] L. Zhu and W. Marcinkiewicz, "Drop Impact Reliability Analysis of CSP Packages at Board and Product Levels through Modeling Approaches," *IEEE Transactions on Components and Packaging Technologies*, Vol. 28, No. 3, 2005, pp. 449-456.

[13] D. Chong, K. Ng, J. Tan, P. Low, J. Pang, F. Che, B. Xiong, L. Xu, "Drop Impact Reliability Testing for Lead-Free & Leaded Soldered IC Packages", *Proc. of 2005 IEEE Electronics Components and Technology Conference*, pp. 622-629.

[14] B. Toleno, D. Maslyk, T. White, "Using Underfills to Enhance Drop Test Reliability of Pb-free Solder Joints in Advanced Chip Scale Packages", *Proc. of 2007 SMTA Pan Pacific Symposium*, 2006.

[15] T. Mattila, P. Marjamaki, J. Kivilahti, "Reliability of CSP Interconnections Under Mechanical Shock Loading Conditions", *IEEE Trans. on Components and Packaging Technologies*, Vol. 29, No. 4, Dec. 2006, pp. 787-795.

[16] G. Wasserman, "Reliability Verification, Testing, and Analysis in Engineering Design", New York: Marcel Dekker, 2003