

WLCSP Mechanical Reliability - High Speed Pull Testing (Lead-Free Solder Alloys and Electroless Nickel UBM)

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ABSTRACT

Electroless Nickel/Gold is widely considered the lowest cost Under-Bump-Metallization (UBM) in the electronics packaging industry. Its implementation has been driven by the need to further reduce the costs of manufacturing. Recent results have shown that the use of an electroless nickel UBM can also increase the mechanical reliability of electronic devices when used with lead-free solders [1-2]. This mechanical strength of the solder interconnect is especially important in portable electronic devices, where WLCSP solder bumps are used in high numbers. Mechanical testing of WLCSP solder joints has shown that the intermetallic layer that is formed between the lead-free solder bump and the UBM is often brittle and can lead to premature failure [3-4]. Because electroless nickel UBMs form different intermetallics with the solder compared to either sputtered or electroplated UBMs, the mechanical strength of the solder joint is also expected to be different.

Small variations in the composition of SnAgCu based solder alloys have been shown to result in significant differences in mechanical reliability [5]. The rate of intermetallic formation and distribution are highly dependent on the solder alloy composition, the UBM composition, and reflow profile. In this study, three solder alloys (SAC-105, SAC-305, SAC-405) were investigated in combination with e-Ni/Au and Ni/Pd UBMs. The strength of the solder interconnect was evaluated using high speed solder pull testing [6].

Keywords: Electroless Nickel, WLCSP, Cold Ball Pull, Wafer Bumping, Reliability, High Speed Pull

INTRODUCTION

As solder based interconnects become more prevalent in consumer based electronics, the mechanical reliability of these joints are of particular importance. There are several recent factors that have contributed to this new focus on mechanical reliability, including the following three factors:

1) The transition from lead-based solders to lead-free solders. With the worldwide mandate to phase out all lead-based solders, the search for new solders which are electrically, thermally, chemically, and mechanically reliable has undertaken a new importance. The standard lead-based solders were well tested, and in general, were highly reliable. During the early stages of the transition away from lead-based solders, the implementation of ternary alloys of SnAgCu (SAC) has dominated the industry. This choice was partially based on the similarity in both processing parameters and thermal reliability to those of the lead alloys. One of the properties which is not as reliable as the lead alloys, is the intermetallic strength of the reflowed solder interconnect. The search for alternative alloys, with better mechanical

strength, has led to studies where, a) the concentration of Ag and Cu are varied within the SAC alloy, b) a fourth component is added to the SAC alloy (Ni, Bi,...), c) alternative UBMs are investigated (e-Ni/Au, e-Ni/Pd, Al/NiV/Cu, copper pillar, etc...), and d) the reflow profiles are optimized.

2) The use of WLCSP sized solder bumps with no under-fill. The smaller flip chip sized solder joints used in many devices have the additional feature that an under-fill material is typically placed between the substrate and the integrated circuit to act as a mechanical medium to strengthen the solder joint, and thus increase the mechanical reliability of the interconnect. For many flip chip based devices, the main reliability criterion is solder fatigue resulting from CTE miss-match during thermal cycling. With the transition to the larger bumps (200-300 μm) used in WLCSP solder joints, the manufacturing goal is to assemble the integrated circuit to the substrate with as few processing steps as possible i.e. no under-fill. The larger bumps are required to increase the substrate to die standoff, and therefore reduce the affects of solder embrittlement due to thermal

cycling. Results in the field have shown that the failure mode has shifted to another mechanism, i.e. intermetallic solder failure due to mechanical shock, impact, and vibration.

3) A steady increase in the production of portable and hand-held electronics. The miniaturization and subsequent portability of consumer electronics, such as cell phones, digital cameras, MP3 players, and laptop computers, has caused a re-evaluation of the reliability criteria used to qualify bumping processes. While thermal, chemical, and electrical reliability are still important, the mechanical strength of the solder joints has become highly visible. One of the main causes of field failures is physical dropping of the portable device which results in a fracturing of the solder joint. This dropping causes a different type stress on the solder joint compared to thermal cycling.

The search for testing techniques that can be used in the fab to both detect process variations in the bumping operation and also be used to screen new solder alloys and UBMs, has lead to the development several new techniques (see Table 1.) The choice of test technique depends somewhat on where you are in the manufacturing chain. To the supplier of UBM and bumping services (contract and captive), one would like to be able to test at the wafer level and test the parts as part of the either final test or inspection steps.

When a solder interconnect fails in the field, there are a number of materials and interfaces that are susceptible to failure (see Figure 1 and Table 2). All of these modes have been observed by the industry and are dependent on the specific manufacturing processes, the equipment used, and the materials used. In practice, the most prevalent modes of failure for WLCSP devices are: a) solder, b) solder & intermetallics, and c) intermetallics.

Table 1. Mechanical Test Methods for Evaluating WLCSP Solder Bumps.

Mechanical Testing Method	Test Format	Cost	Prep and Test Time
Solder Ball Shear	Wafer	Low	Short
Die Shear	Assembled	Medium	Long
High Speed Ball Shear	Modified Die	Low	Long
Drop Testing	Assembled	Very High	Very Long
Tumble Testing	Device	High	Long
Vibration Testing	Assembled	Medium	Long
Bend Testing	Assembled	Medium	Long
Cold Ball Pull	Wafer	Low	Short
High Speed Ball Pull	Wafer	Low	Short

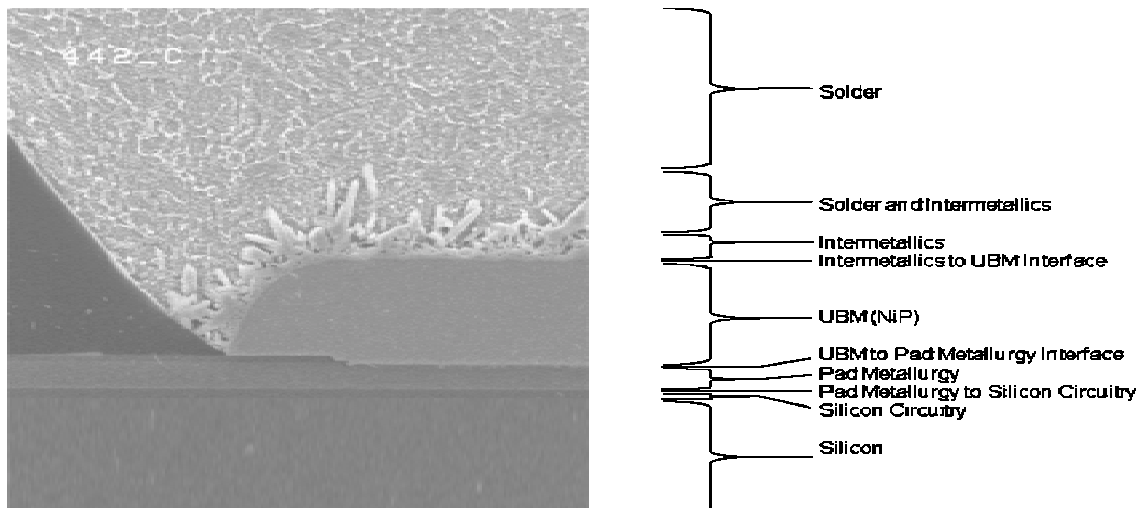


Figure 1: Possible Failure Modes on the Die Side of the Solder Interconnect.

Table 2. Failure modes and Common Terminology.

Mode	Responsible Manufacturing Site	Common Terms for Failure Mode
Solder	Wafer Level Bumping Facility	Ductile Solder, Bulk Solder
Solder & Intermetallics	Wafer Level Bumping Facility	Mixed Mode, Quasi Ductile or Brittle
Intermetallics	Wafer Level Bumping Facility	Brittle Intermetallic
Intermetallics to UBM Interface	Wafer Level Bumping Facility	Adhesive
UBM	Wafer Level Bumping Facility	Cohesive UBM
UBM to Pad Metallurgy Interface	Wafer Level Bumping Facility	UBM Lift
Pad Metallurgy	Integrated Circuit Fab	Cohesive Pad Metal
Pad Metallurgy to Silicon Circuitry	Integrated Circuit Fab	Pad Lift
Silicon Circuitry	Integrated Circuit Fab	Circuit Delamination
Silicon	Silicon Wafer Manufacturer	Silicon Cratering

Currently, the use of standard solder shear testing has been a prerequisite at nearly all bumping facilities as a minimal test for the integrity of the solder to UBM interface. For lead-based solders, this test was typically used as a pass-fail test criteria based on shear force. As the introduction of lead-free alloys progressed, it was quickly discovered that the shear mode is also an important failure criterion, because it qualitatively pointed to differences in the intermetallic strength vs the bulk solder strength. By dramatically increasing the speed at which one shears the solder bumps (high speed shear), one can gain some quantitative information about the intermetallic strength. This is accomplished by determining at what shear speed the mode changes from ductile bulk solder failure, to brittle intermetallic failure.

One of the drawbacks to high speed shear is that it requires that the wafer be diced into small pieces, and the density of bumps is limited to one row in order to allow the shear tool to move parallel to the die surface without contacting any other solder spheres. Another technique which can give comparable data is high speed pull testing (sometimes called cold ball pull). In this method, the solder spheres are pulled perpendicular to the die surface, which allows full wafers to be tested.

EXPERIMENTAL

The study described in this paper uses the high speed pull test method to evaluate the integrity of three different SnAgCu solder alloys (300 μ m spheres), deposited onto two different electroless nickel UBMs (e-Ni/Au and e-Ni/Pd). The test vehicle used for this study was a standard WLCSP semiconductor device which contained six 225 μ m I/O pads per die on a 500 μ m pitch (see Table 3 and Figure 2).

Table 3. Test Wafer Properties.

Wafer Size	150 mm
Wafer Thickness	150 μ m
Die Size	1500 x 1000 μ m
I/O per die	6
Pad Size	250 μ m
Pad Pitch	500 μ m
Passivation Opening	225 μ m
Pad Metallurgy	Al w/0.5%Cu

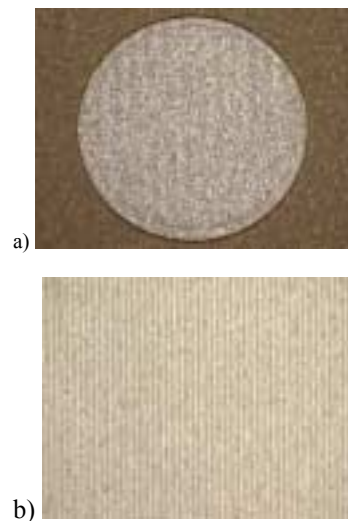


Figure 2. Optical Images of: a), I/O pad b), Pad Metallurgy.

The process flow used to create samples for this study, uses following five steps:

1) The Under-Bump-Metallurgy (UBM) is an integral part of all bumping processes. This layer is typically deposited by physical vapor deposition (PVD), electroplating, or electroless plating [7]. The choice between these three UBM technologies is often

dictated by cost and reliability. PVD and electroplating techniques require both high vacuum and photolithography steps and are therefore considered high cost operations. The electroless nickel/gold process technology is a simple wet chemical process that is self-patterning and is therefore low cost in relations to its total capital investment and operational costs.

For aluminum based integrated circuits, the chemical sequence for depositing the electroless nickel layer is to first clean off the pads of any organic or silicon based contaminants which may occur due to wafer handling, storage, or variations in the manufacturing process. The second step is to remove any native oxide that may have built up on the aluminum pad surface. This is typically performed using caustic based etching chemicals. The next step is to activate the surface of the aluminum. The most commonly used wet chemical system for this is “zincation”, where a zinc oxide solution is used to replace some of the pad aluminum with zinc in an electrochemical reaction. Empirical research has shown that by stripping this zinc layer off and then reforming it in a second zincation step, one creates a higher quality layer of zinc. This is often referred to as “double zincation”. This zinc layer changes the electric potential of the aluminum pad, and when immersed in a nickel sulfate solution, nickel replaces this zinc and an autocatalytic nickel reaction continues. By adjusting the time, temperature, pH, and chemical concentrations of the nickel plating bath, one can create nickel structures between 1 and 25 microns tall.

For most applications the deposition of solder does not immediately follow the nickel deposition process. The nickel surface will oxidize fairly quickly, and therefore a thin layer of a noble metal is typically deposited on top of the nickel to protect the surface from oxidation. There are two common metals (Pd and Au) which are compatible with the electroless nickel process and can be deposited sequentially within the same plating line using either immersion or electroless based processes. Table 4 lists the Ni/Au and Ni/Pd layers used in this study. Figure 3 shows the test die plated with e-Ni/Au. Note the slight increase in surface roughness compared to the original aluminum surface.

Table 4. e-Ni/Au and E-Ni/Pd Properties.

Nickel Thickness	5 μm
Gold Thickness	0.06 μm
Palladium Thickness	0.2 μm
Phosphorous Concentration	8-9%

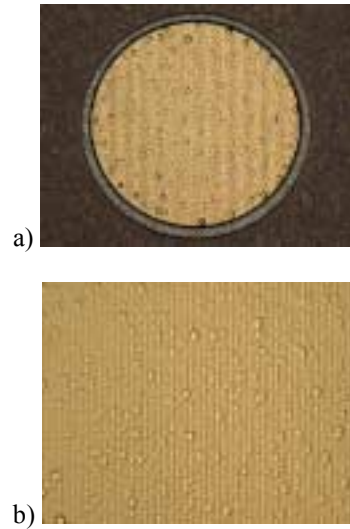


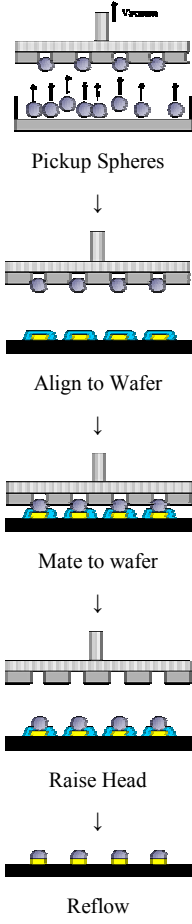
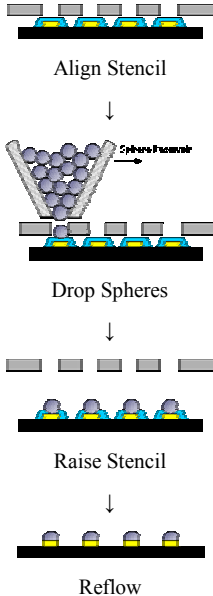
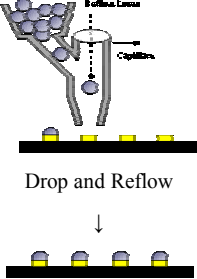
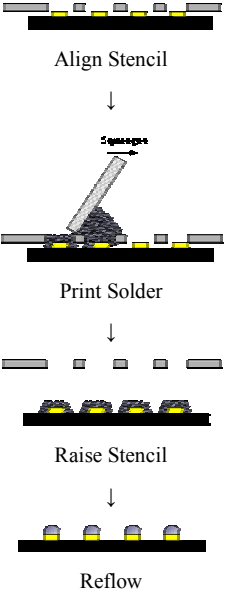
Figure 3. Optical Images of e-Nickel/Gold plated
a) I/O pad, b) Pad Metallurgy

2) Flux was applied to the wafer using a standard surface mount printer. Flux was applied through a screen with a thickness of approximately 2-4 mils. The specifications for flux thickness are fairly loose. However, if the flux is too thin the solder spheres do not adhere well to the pads during sphere placement, and if the flux is too thick, the spheres can move during reflow (floating spheres).

3) WLCSP bumps are typically produced by dropping preformed solder spheres onto the wafer, or by printing paste through a stencil based template. Table 5 lists several of the technologies used to create WLCSP sized bumps.

The Sphere Transfer (often referred to as Wafer Level Solder Sphere Transfer or Gang Ball Placement) and Solder Jetting technologies were used in this study to place solder spheres onto the silicon test wafers. The Sphere Transfer technology uses a patterned vacuum tooling fixture (arrangement plate) to simultaneously pick up preformed spheres and transfer them over to the wafer all at once. The first step in the process is to lower a tooling plate (vacuum stencil) into a sphere reservoir. Vacuum and mechanical vibration (e.g. ultrasonics) is applied to the plate to selectively pick up the spheres. This fixture is then inspected for missing or extra spheres. The tooling is then aligned to the wafer and lowered to bring the solder spheres into contact with the pre-fluxed wafer pads. Finally, the vacuum is turned off; the plate is raised.

Table 5. Process Summary of WLCSP Solder Deposition Technologies.

	Sphere Transfer [8-9]	Sphere Drop [10]	Solder Jet [11-12]	Stencil Print [13]
Process Flow	 Pickup Spheres Align to Wafer Mate to wafer Raise Head Reflow	 Align Stencil Drop Spheres Raise Stencil Reflow	 Drop and Reflow	 Align Stencil Print Solder Raise Stencil Reflow
Sphere Size (μm)	60-760	200-760	80-760	N/A
Solder Alloys	All Spheres	All Spheres	All Spheres	All Pastes
Bump Ht Variation (%)	< 5	< 5	< 5	5-10
Throughput (wafers/hr)	25-45	25-35	< 1	25-50
Wafer Size (mm)	100-300	100-300	Die & 100-300	100-300
Yields (ppm defects)	< 10	50-1000	< 10	100-1000
Tooling Cost (\$)	500-1500	1000-2000	0	500-1500

The solder jetting technology drops single spheres onto pre-fluxed wafers at a rate of ten bumps per second through a capillary tube. For this study the laser option was not used to reflow the spheres. This tool is typically used for MEMs and optoelectronics bumping, quick turn prototyping, disc drives, low

volume applications like military and medical application, and specialty bumping applications.

4) The wafers were removed from the solder deposition tools and reflowed using a standard conduction reflow oven. The peak temperature was set to 240 degC for ~25 sec dwell time.

5) After reflow the residual flux was cleaned by immersing the wafers in a commercial solvent and applying ultrasonics to increase the cleaning efficiency.

RESULTS

Three different solder alloys (SAC-105, SAC-305, and SAC-405) were deposited onto the test wafers. These wafers were first plated with either e-Ni/Au or e-Ni/Pd. Each sample was placed in the high speed pull tool and 10 bumps were pulled at 5 different speeds. The only failure modes that were observed occurred within the solder, within the intermetallics, or a combination of both (see Figure 4). No failures were observed within the UBM or within the device circuitry.

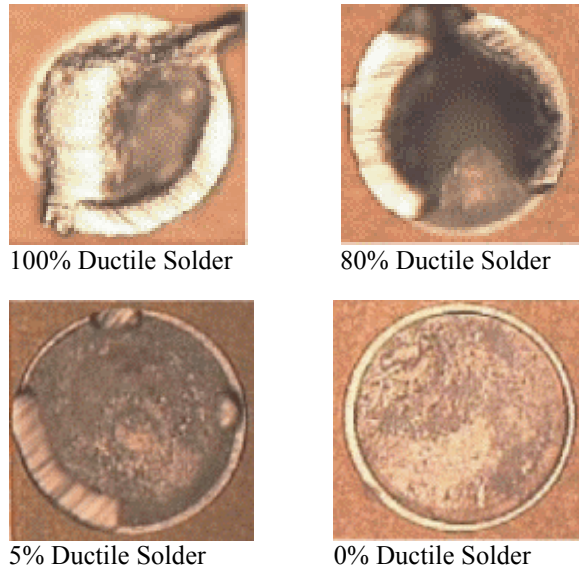


Figure 4. Optical Images of Typical Failure Modes.

The high speed pull results for the samples plated with an e-Ni/Au UBM are shown in Figure 5.

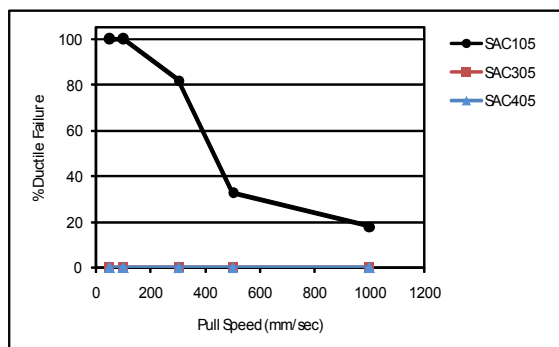


Figure 5. Plot of % Ductile Failure Mode vs Pull Speed on Ni/Au UBM.

Results show that the solder alloy which contained less silver (SAC-105) exhibited a transition from ductile solder failure to brittle intermetallic failure between 100 and 300 mm/sec. The other two alloys which contain higher levels of silver (SAC-305 and SAC-405) exhibited brittle intermetallic failure at all of the test speeds evaluated (50-1000 mm/sec).

The high speed pull results for the samples plated with an e-Ni/Pd UBM are shown in Figure 6. Changing the gold layer to palladium had the affect of moving the onset of brittle intermetallic failure to higher pull speeds compared to those measured for the SAC-105 Alloy on e-Ni/Au. This UBM also results in some ductile fracture for SAC305 and SAC405 at the lower pull speeds.

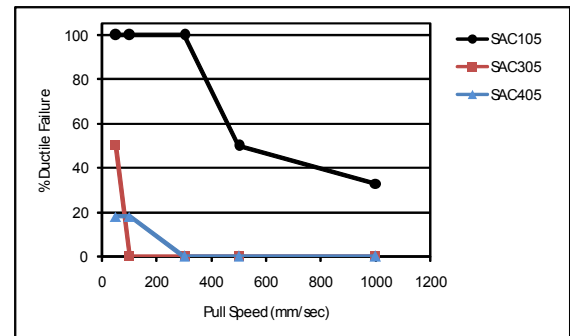


Figure 6. Plot of % Ductile Failure Mode vs Pull Speed on Ni/Pd UBM.

CONCLUSIONS

The failure mode for the SAC-105 alloy with the lower Ag content has higher levels of ductile solder failure than either the SAC-305 or SAC-405 alloys. This is consistent with high speed shear testing and drop testing results reported in the literature [14-16].

Ni/Pd has a slightly higher onset to brittle solder failure than Ni/Au. These results indicate that using e-Ni/Pd is a viable alternative to e-Ni/Au UBM for WLCSP applications.

The high speed cold ball pull test method has been shown to be an acceptable technique for online monitoring of WLCSP bumping processes. Continuing research which will be presented in Part II of this program. This work will include varying the nickel, gold, and palladium thicknesses, varying the reflow profiles and reflow techniques, and looking at quaternary solder alloys.

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