Board Level Failure Analysis of Chip Scale Package Drop Test Assemblies

Nicholas Vickers, Kyle Rauen, Andrew Farris, Jianbiao Pan
Cal Poly State University
San Luis Obispo, CA 93407
Email: navickers@gmail.com, krauen@calpoly.edu, ajfarris@gmail.com, pan@calpoly.edu

Abstract

This paper presents the failure analysis results of board level drop tests. In this study, the test vehicle was designed according to the requirements of the Joint Electron Device Engineering Council (JEDEC) drop test board. The test vehicle was assembled with 15 chip scale packages (CSPs) each having 228 daisy-chained 0.5 mm pitch solder joints using Sn-3.0 wt% Ag- 0.5 wt% Cu (SAC305) lead free solder. Assemblies were drop tested using three different peak accelerations of 900 G, 1500 G, 2900 G, with 0.7 ms, 0.5 ms, and 0.3 ms pulse durations, respectively. Scanning electron microscopy (SEM) with energy dispersive spectroscopy and dye-penetrant methods were applied to investigate the failure locations and the failure modes. The failure modes and solder joint locations were mapped. Failure analysis showed that pad cratering was the most common failure mode and that this led to trace cracking on the board side. Trace cracking was the second most common failure mode. Solder joint cracking was also observed on the board side near the intermetallic layer, which was the third most common failure mode. The results imply that the solder joint is more reliable than the printed circuit board during drop test.

Keywords: Lead free solder, drop impact test, pad cratering, failure analysis.

1. Introduction

Ten trillion solder interconnections are made annually in the electronics industry for mobile devices, computers, and other communications, medical, aerospace, and military applications [1]. The solder interconnection is the primary interconnection in microelectronics packaging because it provides the mechanical and electrical interconnection between the package and the printed circuit board (PCB). If one interconnection fails in a PCB, the whole board and even the whole system may fail. Therefore, establishing and improving the reliability of solder interconnections is vital to the $1.3 trillion electronics industry.

Handheld consumer electronic devices are prone to be dropped. The drop event may result in the solder interconnection failure. The drop impact response and failure characteristics are important topics to understand in order to improve electronic assembly reliability. With the enactment and enforcement of the European Union's Restriction of Hazardous Substances (RoHS) and similar legislation around the world, the focus of reliability researchers quickly shifted toward lead-free solder alloys. Tin-silver-copper (SnAgCu) is now a commonly used lead-free solder alloy in the electronics industry.

The drop reliability of SnAgCu solder joints has been researched by many [2-12]. Poor drop test reliability of lead-free solders has been reported [12], because SnAgCu alloys have higher strength and modulus than SnPb. Two ways to improve drop testing reliability of SAC alloys are: lower Ag content [13], and adding micro alloying [14]. Both methods result in many SAC alloys. However, the failure mechanisms of drop test remain unclear.

The purpose of this research is to study the failure mechanisms for board level lead-free chip scale packages (CSPs). The final goal is to improve the reliability of solder interconnections in electronics assemblies through an improved understanding of failure.

2. Experiment

The test vehicle used was a JEDEC JESD-B111 standard eight-layer FR4 test board as shown in Figure 1. Fifteen chip scale packages (CSPs) were attached to the test vehicle using a lead-free surface mount assembly process. Each 12 mm square CSP had 228 Sn-3.0 wt% Ag- 0.5 wt% Cu (SAC305) solder joints at a 0.5 mm pitch that form an electrical and mechanical connection to the circuit board. The full details of the board assembly, drop testing method, and reliability results are reported elsewhere [11]. The boards were drop tested using a Lansmont MTS II shock test system and were dropped until a majority of the CSPs experienced electrical failure. Three different peak acceleration inputs were used in drop testing: 900 G, 1500 G, 2900 G, with 0.7 ms,

0.5 ms, and 0.3 ms pulse durations, respectively. The electrical continuity of each daisy-chained CSP was verified before drop testing.

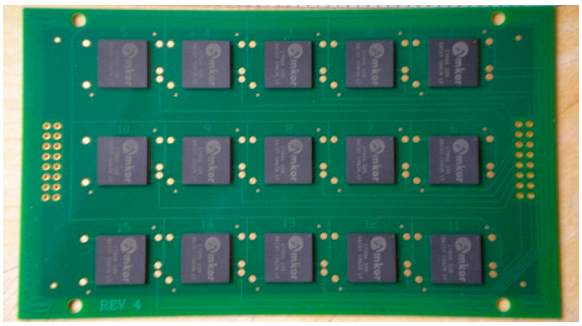

Figure 1. Test vehicle assembly

Two failure analysis methods were used to investigate the failure locations and the failure modes: 1) dye-penetrant and 2) cross-sectioning Scanning Electron Microscopy (SEM) with Energy Dispersive Spectroscopy (EDS). Dye penetrant is a common failure analysis method to examine pre-existing cracks in solder joints, especially for Ball Grid Array (BGA) and CSP solder joints. The process works as follows. The PCBs were submerged into a thermal-curable dye so that the dye will penetrate into the crack area. After the dye is cured, the components were pulled off exposing the preexisting cracks. The components and boards were examined using metallographic microscopes.

Cross sectioning SEM with EDS is another common failure analysis technique to investigate the crack location and intermetallic composition in solder joints. Sample preparation starts with cutting sections out of the PCB using a diamond abrasive saw. The CSP and board section are mounted in a clear epoxy, then ground and polished to expose the solder joint cross section. A succession of sand papers were used with the grit size from 80, following by the number 240, 320, 600, and 4000. The samples were then fine polished using 0.3 and 0.05 alumina slurries. The last steps were etching then sputter coating with a very thin layer of gold. Cross sectioned samples were etched with a 1% nitol etchant to evaluate the microstructure. Micro hardness tests were done on both the solder and resin to compare strengths of the materials. The tests used a vickers microhardness indenter at 100 grams of force.

3. Results

After analyzing 60 components on four boards that were dye penetrated, five failure modes have been identified: 1) pad cratering, 2) solder cracking near the board side, 3) solder cracking near the component side, 4) input/output (I/O) trace fracture, and 5) daisy chain trace fracture. Figure 2 summarizes the percentage of each failure mode on these 60 components analyzed. It shows that pad cratering is the dominant failure mode for these test vehicles in drop impact; 83.3% of the components exhibited pad cratering. Pad cratering is defined as cracking in the thin resin rich region underneath the copper pads and traces as shown in Figure 3. Note that some components had multiple failure modes so that the total percentage shown in Figure 2 is more than 100%.

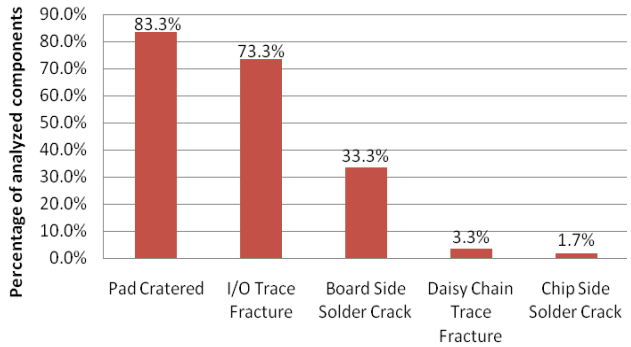

Figure 2. Summary of failure modes

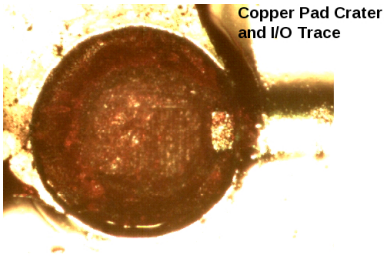

Figure 3. Copper pad cratering with dyed board fibers, 100X magnification

Drop test reliability data shows that the component location plays a significant role and the components along the board center tend to fail earliest and most frequently [11]. To investigate whether failure mode differs at different component locations, the failure modes and the component locations were mapped and shown in Figures 4 - 7.

The failure maps in Figures 4 - 7 show all the solder joint locations and failure modes observed for four test boards. All four boards were drop tested at 1500 G peak acceleration, but the drop count varies for each. The fill color in each device interior indicates the stage of failure: green is not failed, cyan is transitional failure (minor resistance change), orange is temporary discontinuity, red is permanent discontinuity. The individual solder joints are indicated in the array around each device with failure mode: white squares are not failed, black squares indicate pad crater, red squares indicate solder crack

near board side, and yellow squares indicate solder crack near component side (only 1 is shown).

Figures 4 and 5 show boards with no edge-bonding applied to the CSPs, and Figures 6 and 7 show boards with edge-bonding applied [11]. In Figures 5 and 6, pad cratering is shown to occur on nearly every CSP after relatively few drop impacts, and may exist before without electrical failure occurs. In a few cases electrical failure occurred by trace cracking without pad cratering or solder fracture.

It is clear that pad cratering occurred mainly in the corners of the CSPs with the exceptions to components 3, 8, and 13, where it often happened along the edges. The majority of pad cratering occurred on one side of the board (toward component 6), which indicates asymmetric strain distributions along the board. A dynamic failure measurement system was used with a cable attachment near component 6.

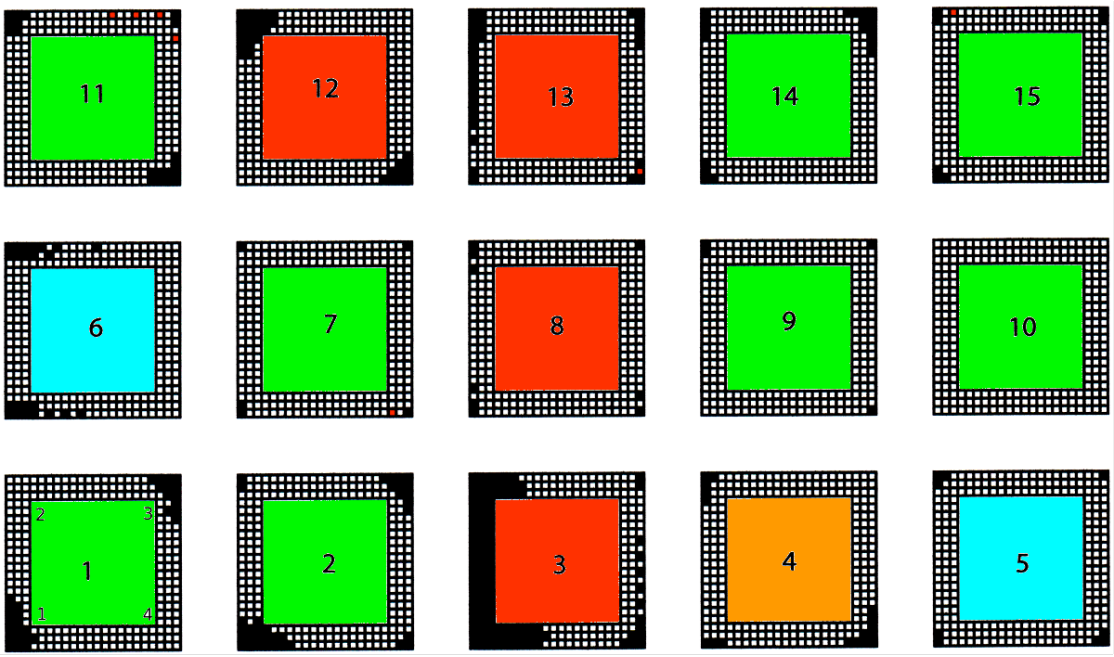

Figure 4. Failure mode map for not edge-bonded board after 10 drops at 1500 G.

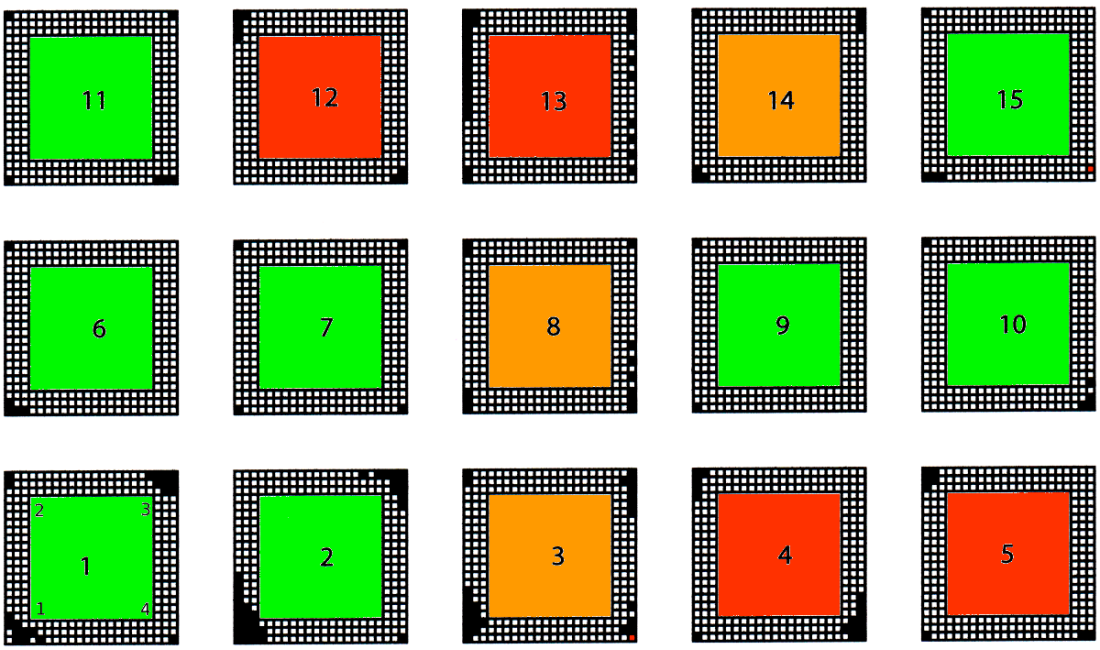

Figure 5. Failure mode map for not edge-bonded board after 14 drops at 1500 G.

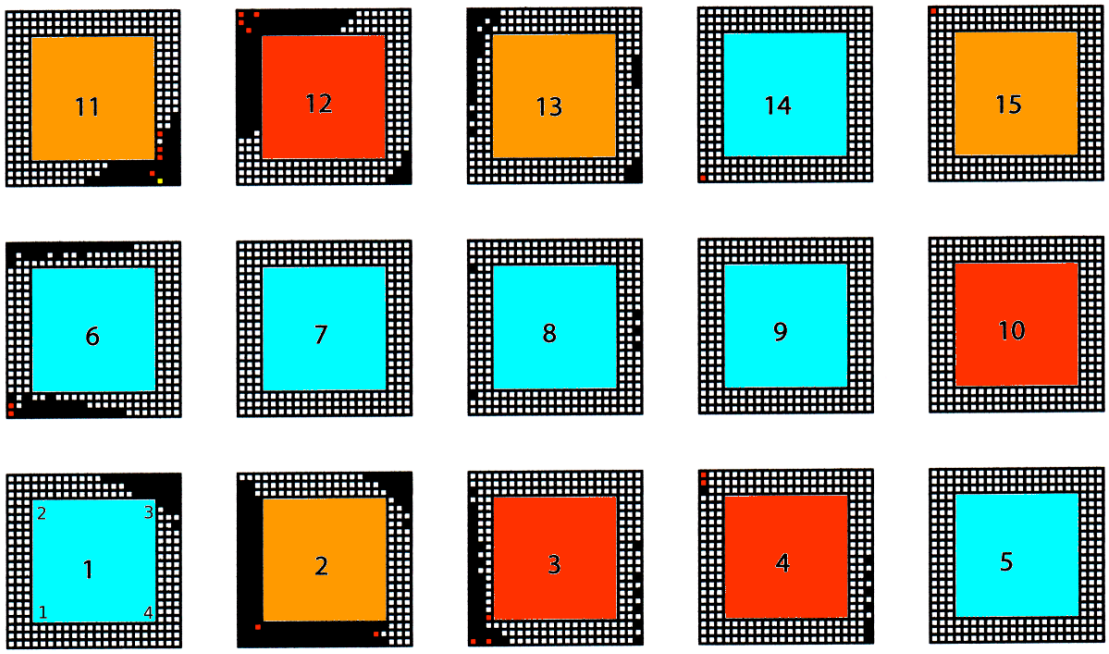

Figure 6. Failure mode map for edge-bonded board after 279 drops at 1500 G.

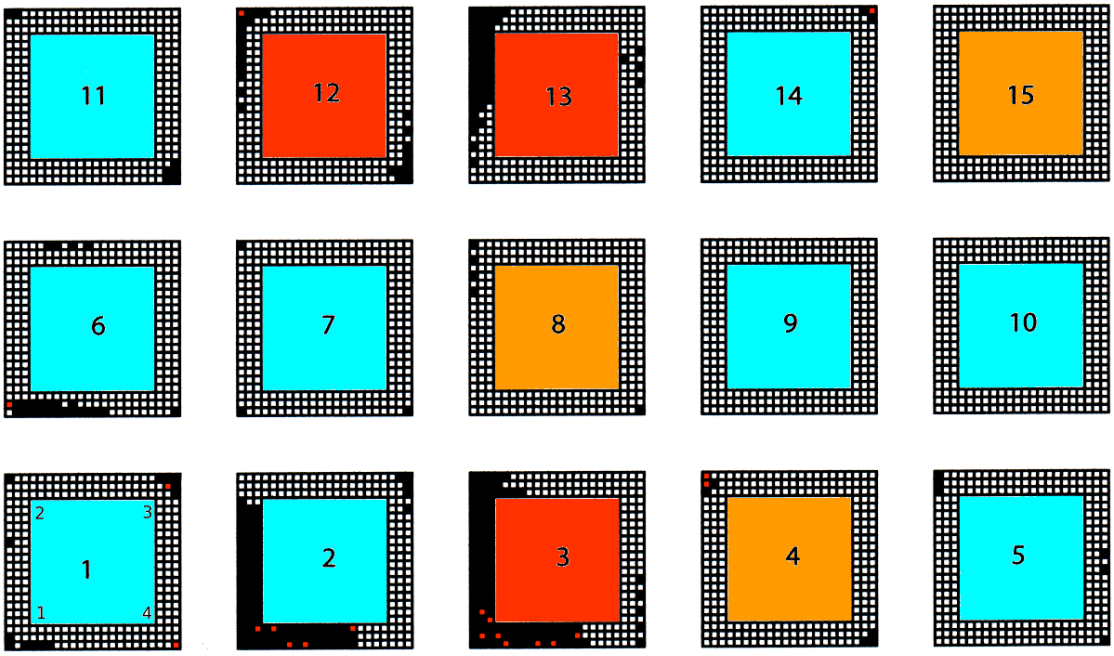

Figure 7. Failure mode map for edge-bonded board after 325 drops at 1500 G.

It should be pointed out that pad cratering does not necessarily lead to electrical failure of solder joints. Figure 8 shows the relationship between pad cratering and electrical failure. It shows that 19.4% of components that had pad cratering did not fail electrically. The figure also indicates that most components that electrically failed exhibit pad cratering, but pad cratering occurred on some components that were not yet failed; pad cratering was observed in combination with other failure modes.

The second most common failure mode is I/O trace fracture as shown in Figure 9. All components that exhibit I/O trace failures also exhibit pad cratering. 72.2% of pad cratered components exhibit I/O trace fracture implying that the two failure modes are coupled. Similarly all daisy chain trace fractured components exhibit pad cratering,

implying that daisy chain trace fracture is caused by pad cratering. Conversely, solder cracking appears to be independent of pad cratering. This is shown by Figure 8 where 5.6% of electrical failures are caused by solder cracking where pad cratering was not observed. Cracking of the solder joints on the board side and component side was observed in 33.3% and 1.3% of the components, respectively.

Combining the failure analysis with the reliability study previously reported [11], we see that pad cratering indirectly causes electrical failure. The reasons for this are simple, when the resin cracks under the solder joint, stress is then shifted on to the electrical trace on the PCB. When this occurs the trace can fracture as illustrated in Figure 10. These trace fractures occur both at outside trace connections where the input and output signals occur, and also in traces that connect solder balls within the BGA.

Figure 11 compares the ratios of failure modes. Input/output trace failures were attributed to causing 77% of the electrical failures. Of that 77%, 19% were in conjunction with solder fracture. Solder fracture accounts for 12% of the electrical failures observed, and 11% of the electrical failures were caused by the daisy chain trace fracturing.

Cross sectioning SEM showed three different failure modes: 1) pad cratering, 2) daisy chain trace fracture, and 3) solder fracture on the board side. Pad cratering as shown in Figure 12 was observed near the corners of the component. Resin cracks that cause pad cratering never penetrated into the weave region and occurred only in the resin rich region above the fiber weave near copper pads and traces. Resin cracks exhibited brittle fracture characteristics. Both daisy chain trace cracking and solder cracking as shown in Figure 13 are less common.

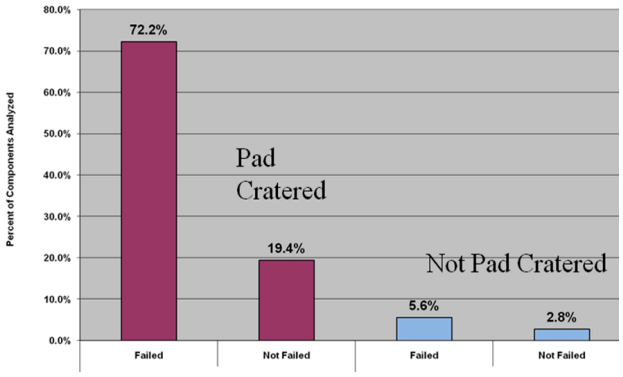

Figure 8. The relationship observed between pad cratering and electrical failure

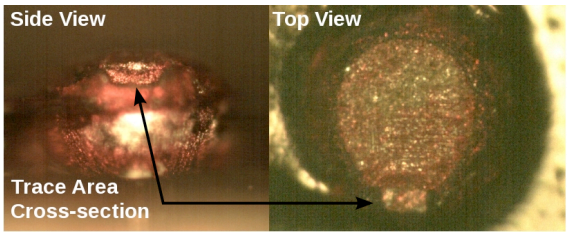

Figure 9. I/O trace cracked away from solder joint, 100X magnification

Figure 10. Illustration of cracked trace caused by pad cratering

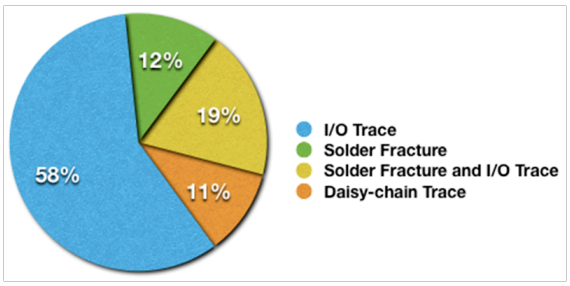

Figure 11. Percentage of electrical failure attributed to the different material failure modes

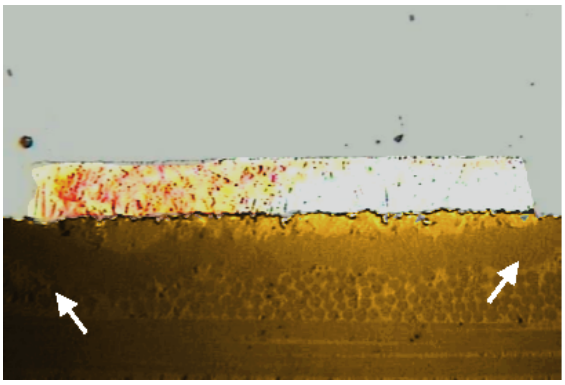

Figure 12. Resin cracks beneath copper pad. Magnification is 500X

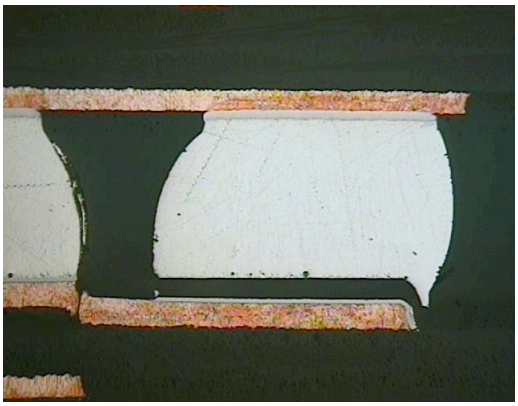

Figure 13. Solder crack near board side IMC shown on the right side of the picture. On the left is evidence of a daisy chain trace fracture on the board side at 100X magnification.

After evaluating the cross-sectioned samples, an investigation of the solder ball microstructure and also the relative strength of the solder material compared to the resin was performed. The resulting microstructure of the solder ball as shown in Figures 14a and 14b shows small dendritic grain growth. The smaller grains strengthen the solder material. Failures are consequently shifted to the weaker material, the resin. Figure 15 shows the microhardness test results. The solder material had an average microhardness of 72 while the resin has a microhardness of 33. The result indicates that the solder is much stronger than the resin. This finding verifies that the resin is the weakest link and suggests that pad cratering should be the most common material failure.

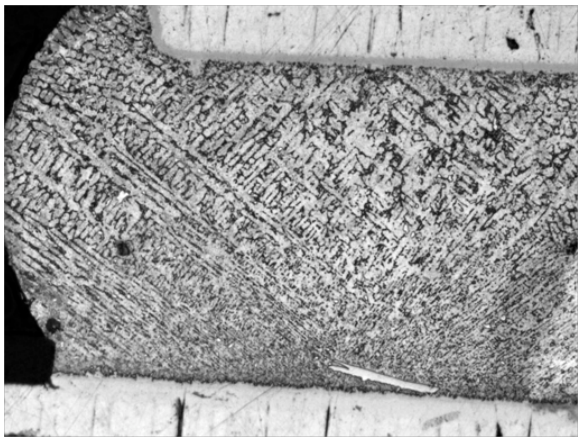

Figure 14a. Image of solder ball microstructure at 200X magnification.

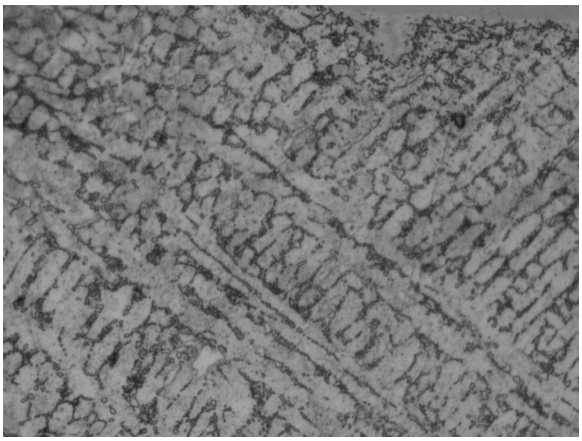

Figure 14b. Image of solder ball microstructure at 500X magnification.

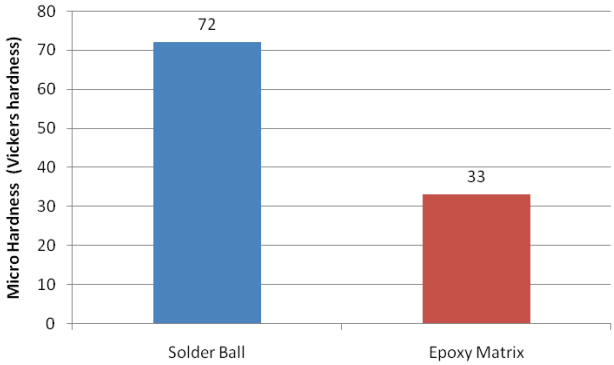

Figure 15. Results of the microhardness testing

4. Summary

The failure modes of drop testing CSP packages with SAC305 solder joints assembled on a JEDEC standard test vehicle are reported. The following conclusions can be drawn from this study:

1. Pad cratering is the primary material failure mode.
2. The board material is the weakest link in the electronic assembly, will fail first, and will cause other failures such as trace cracking.
3. Trace cracking due to pad cracking is more common than solder cracking, especially where traces are connected to outer array solder joints and run outward from the CSP.
4. Majority failures occur at the corners of the packages implying that the corners of the components experience the most strain and stress.

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References

[1] N. Brathwaite, "Forword," *Lead-free Solder Interconnect Reliability*, edited by D. Shangguan, ASM International, p. vii, 2005.

[2] Y. Liu, G. Tian, R.W. Johnson, and L. Crane, "Lead-free chip scale packages: assembly and drop test reliability", *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 29, No. 1, Jan. 2006, pp. 1-9.

[3] P. Marjamaki, T. Mattila, J. Kivilahti, "Finite element analysis of lead-free drop test boards", Proceedings of 2005 IEEE Electronics Components and Technology Conference, pp. 462-466.

[4] M.A. Matin, W.P. Vellinga, M.G.D. Geers, , "Microstructural Stability and Failure Modes in Eutectic Sn-Ag-Cu Solder", 5th International Conference on Thermal and Mechanical Simulation and Experiments in Micro-electronics and Micro-Systems, pp. 337-340.

[5] A.R. Zbrzezny, P. Snugovsky, T. Lindsay, and R. Lau, "Reliability Investigation of Mixed BGA Assemblies", *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 29, No. 3, pp. 211-216, 2006.

[6] H. Lou, X. Qu, Z. Chen, J. Wang, T. Lee, and H. Wang, "Lifetime assessment of solder joints of BGA package in board level drop test", Proc. of IEEE 6th International Conf. on Electronic Packaging Technology, 2005, pp. 696-700.

[7] F.X. Che, J.H.L. Pang, W.H. Zhu, W. Sun, A. Sun, C.K. Wang, H.B. Tan, "Comprehensive modeling of stress-strain behavior for lead-free solder joints under board-level drop impact loading conditions", Proceedings of 2007 IEEE ECTC, pp. 528-534.

[8] E.H. Wong, R. Rajoo, Y.M. Mai, S.K.W. Seah, K.T. Tsai, and L.M. Yap, "Drop Impact: Fundamentals & Impact Characterization of Solder Joints," Proceedings of 2005 IEEE ECTC, pp. 1202 – 1208.

[9] D.Y.R. Chong, F.X Che, J.H.L. Pang, L. Xu, B.S. Xiong, H.J. Toh, and B.K. Lim, "Evaluation of influencing factors of board-level drop reliability for chip scale packages (fine-pitch ball grid array)", *IEEE Transactions on Advanced Packaging*, Vol. 31, No. 1, pp. 66-75, 2007.

[10] Y.S. Lai, P.F. Yang, and C.L. Yeh, "Experimental studies of board-level reliability of chip-scale packages subjected to JEDEC drop test condition", *Microelectronics Reliability*, Vol. 46, No. 2, 2006, pp. 645-650.

[11] A. Farris, J. Pan, A. Liddicoat, B. J. Toleno, D. Maslyk, D. Shangguan, J. Bath, D. Willie, D. Geiger, "Drop Test Reliability of Lead-Free Chip Scale Packages", Proceedings of 2008 IEEE Electronics Components and Technology Conference, pp. 1173-1180.

[12] D.Y.R. Chong, K. Ng, J.Y.N. Tan, P.T.H. Low, J.H.L. Pang, F.X. Che, B.S. Xiong, L.H. Xu, "Drop impact reliability testing for lead-free & leaded soldered IC packages", Proceedings of 2005 IEEE Electronics Components and Technology Conference, pp. 622-629.

[13] H. Kim, M. Zhang, C.M. Kumar, D. Suh, P. Liu, D. Kim, M. Xie, and Z. Wang, "Improved drop reliability performance with lead free solders of low Ag content and their failure modes", Proceedings of 2007 IEEE Electronics Components and Technology Conference, pp. 962-967.

[14] R.S. Pandher, B.G. Lewis, R. Vangaveti, and B. Singh, "Drop shock reliability of lead-free alloys -- Effect of micro-additives", Proceedings of 2007 IEEE Electronics Components and Technology Conference, pp. 669-676.