

The Design and Applications of Embedded Passives on Flexible PCB Substrates

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Abstract

This paper demonstrates the design and application of embedded passives on flexible PCBs (printed circuit boards). Embedded capacitors and inductors are integrated in a four-layer flexible PCB process. Four copper layers and three organic materials constitute the PCB lamination. The library of embedded passives is developed by measurements, simulations and circuit models. In addition, the 3D transformation models of embedded passives are also presented. Thus, the electrical deviations between bended and straight structures are estimated. Therefore, the feasibility of embedded passives is verified by the library and transformation models.

Key words: Embedded passive, Flexible, PCB, Capacitor, Inductor, Transformation model,

Introduction

Embedded passives are passive components placed between interconnecting substrates of a printed wiring board, [1]. Embedded capacitors, inductors and resistors are formed by etching circuit patterns on each metal layers, and then are interconnected by buried and blind via holes. With special materials, the size of embedded passives can be reduced. There are many potential advantages of embedded passives for many types of applications. Capacitors could be placed underneath the active component they support; thereby reducing the number of layers and interconnecting vias, [1]. So, lower parasitic inductance and cross talk benefit the performance of circuits. A capacitor dielectric placed between power and ground planes would lower noise and provide blocking capacitors for filtering applications, [1]. Additional advantage includes a large reduction in the number of solder joints leading to improved reliability, [1]. ITRI has proposed several applications of embedded passives, such as Power Amplifier, Bluetooth and WLAN modules, [2]~[7].

Flexible electronic products are drawing the attentions of customers and designers. The electronic reader products – Kindle and Reader - proposed by Amazon and Sony are candidates for the applications of flexible electronics. Electronic components will be realized by directly printing on plastic substrates in the future. With the aforementioned advantages, embedded passives have great potentials for the design of flexible electronics. The paper describes the design and verifications of embedded passives in a multi-layer flexible PCB. Measurements, simulations

and circuit models are used to verify the electrical characteristics of embedded capacitors and inductors. With regard to bended structures, we have developed the 3D transformation models of embedded passives. The concept of building transformation models is introduced and the electrical deviations between bended and straight structures are observed. As a result, the feasibility of embedded passives is verified for the applications of flexible multi-layer PCBs.

I. Flexible Embedded Capacitors

The four-layer stacked PCB lamination process consists of four copper layers and three ultra-thin organic materials. The Hi-Dk Copper-Clad Laminate (CCL) instead of rigid fiberglass material is first treated as a core, and its Dk is almost 20 @ 0.1GHz. With a total thickness of 0.2mm, the multilayered, ultra-thin PCB substrate is mechanically flexible. In addition, HDI (high-density interconnect) vias and plated through holes (PTH) are used to interconnect copper layers. Thus, embedded capacitors and inductors can be integrated into the process. The structure of the four-layer stacked PCB is shown in Fig.1.

The simulation, circuit and measurement models of flexible embedded capacitors are shown in Fig.1 through Fig.3. These models assist circuit designers in understanding the electrical characteristics of embedded capacitors. Embedded capacitors are laid on both sides of Hi-Dk CCL in order to shrink the dimensions of capacitors with large capacitance. Fig.1 shows the structures of multilayer flexible PCB and one-port capacitor. Fig.2 shows the circuit model extracted from the s-parameters of EM (electromagnetic) simulations. The circuit model interprets

the intrinsic and parasitic effects of one-port capacitor. With regard to the circuit model of a $30 \times 30 \text{ mil}^2$ capacitor, its intrinsic capacitance C_s is 17pF; the parasitic effects of feed line and capacitor plates are modelled as a series of inductor $L_s=0.03\text{nH}$ and resistor $R_s=0.63\Omega$. The fringe effect is modelled as two pairs of series resistor $R_{p1}/R_{p2}=2.5\Omega$ and capacitor $C_{p1}/C_{p2}=10.1\text{pF}$ shunted to ground. Fig.3 shows the measurement results of embedded capacitors. The results are distributed into two figures according to the dimensions of capacitors; one is for the area less than $10,000 \text{ mil}^2$, and the other is for its dimensions extended to $800,000 \text{ mil}^2$. For dimensions less than $10,000 \text{ mil}^2$, capacitances increase linearly with its dimension. However, the relationship is not linear for the capacitors with large dimensions. This is because fringe effects and radiations have dominated the electrical characteristics of large-sized capacitors.

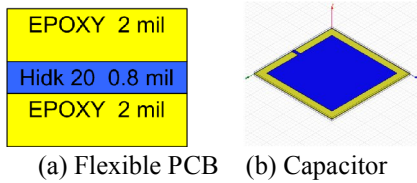


Fig.1 The simulation model of capacitors

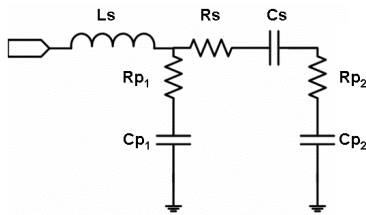
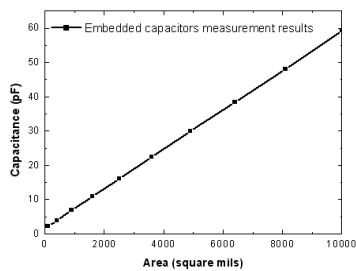
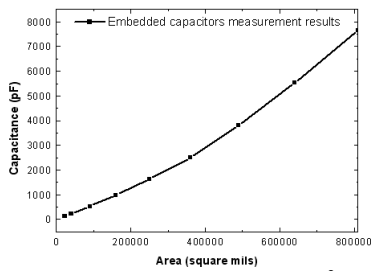


Fig.2. The circuit of one-port capacitor



(a) Area < $10,000 \text{ mil}^2$



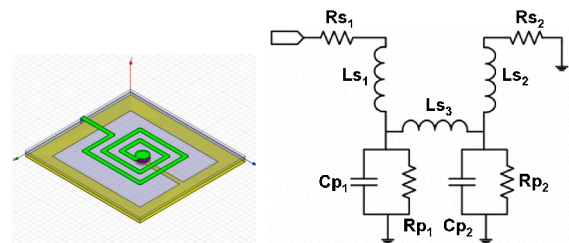
(b) Area < $800,000 \text{ mil}^2$

Fig.3. Measurements of capacitors

II. Flexible Embedded Inductors

The models of flexible embedded inductors are presented in Fig.4 and Fig.5. The embedded inductors are laid on the top side of epoxy layer and are encircled by ground loops. The ground loop structure is intended for reducing the parasitic effects between inductors and surroundings; thus electrical performances are improved. Fig.4 shows the EM and circuit model of an inductor. The circuit model interprets the parasitic effects of one-port inductor. For the model of a 2-turn inductor, its intrinsic inductance L_{s3} is 8nH; and the parasitic inductance and resistance of the feed-line and ground-connection line are $L_{s1}/L_{s2}=0.1\text{nH}$ and $R_{s1}/R_{s2}=0.3\Omega$; and other parasitic effects between the inductor and multilayer structure are modeled as two pairs of parallel $C_{p1}/C_{p2}=127\text{fF}$ and $R_{p1}/R_{p2}=8\Omega$. The planar spiral inductors with various dimensions were designed and fabricated on the four-layer flexible PCB with conductor line width/space 3mil/3mil.

Furthermore, the influence of ground planes on electrical characteristics are tested and verified by circuit patterns and measurements. In this experiment, the 1-turn inductors are laid on the top layer (layer1) and are arranged with different ground planes. Four cases of ground planes are considered. The ground planes are individually set on metal layer 4/ 3/ 2 and a looped ground on layer4. The measurement results are shown in Fig.5 and Table.1. In Fig.5, the line L1 figures the inductor with a ground loop; L2 figures the inductor with a ground plane on the bottom metal (layer4); L3 figures the inductor with a ground plane on layer3; and L4 figures the inductor with a ground plane on layer2. The measured inductances, self resonant frequency (SRF) and Q_s are tabulated in Table1. According to the experiment, the inductance and Q of the inductor with a looped ground (the L1 case) are higher than other cases. The approaching of ground planes enhances parasitic capacitances and decreases inductance and Q values. Therefore, the ground plane must be carefully designed in order to improve the electrical characteristics of embedded passives.



(a) Planar Spiral Inductor (b) Circuit Model

Fig.4. Models of one-port inductor

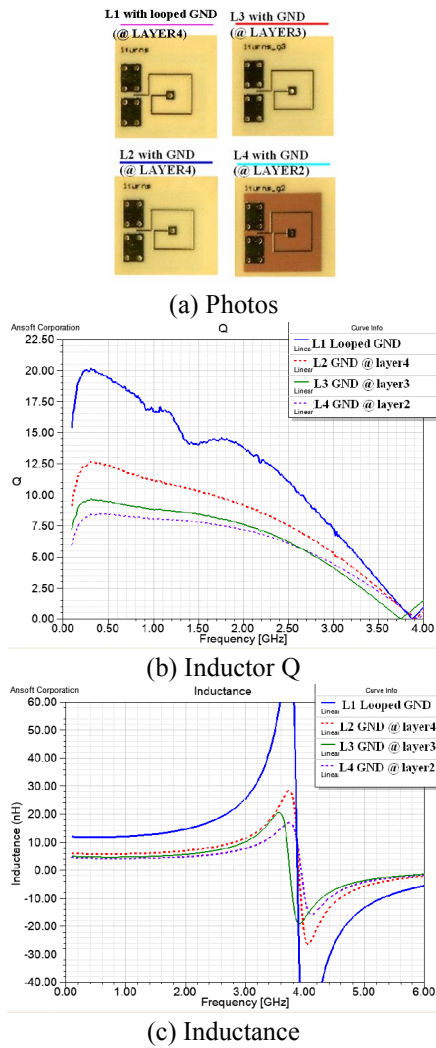


Fig.5. Inductors with various ground planes

Table1. Inductors with various ground planes

Line	Ground Plane	Ind. (nH) @100MHz	SRF (GHz)	Peak Q
L1	Looped GND	12.0	3.95	20.1
L2	GND @ layer4	6.1	3.95	12.7
L3	GND @ layer3	5.1	3.75	9.7
L4	GND @ layer2	4.5	3.95	8.5

III. LC transformation Model

The multi-layer PCBs are not straight because thermal stress is applied during the lamination process. Common electro-magnetic (EM) simulators are intended for straight structures and the corresponding electrical characteristics. Thus, there exist electrical variations between simulations and fabrications. Since the transformed structures can not be built directly on a 3D EM simulator, like Ansoft HFSS, building transformed structures must rely on other mechanical CAD tools. Fig.6 interprets the concept of developing a transformation model. At first, the destined structure is tested and simulated in HFSS, and then its 3D geometry is exported. Then, the transformed structure is generated by projecting

the 3D geometry on a standard curved surface in a mechanical CAD tool. Afterward, the structure is further imported and regenerated in HFSS. However, the structure cannot be simulated immediately because the analytic method of HFSS must be satisfied. Some key issues and file formats must be corrected for the cooperation between CAD and HFSS, such as the definition of parts, the sequence of building elements, and the overlay, etc. After testing and running EM simulations, the 3D transformation model is done. In addition, the degree of deflection for structures – delta δ (%) – is defined as the quotient of the risen distance divided by the length of the curve. If delta δ (%) is positive, the transformation is convex; otherwise, it is concave.

As the transformed structure is regenerated in HFSS, there exist geometry errors induced by fractional intersections of misaligned objects. For corrections, the structure is divided into different parts in CAD, and then the parts are imported into HFSS in proper sequence. In Fig.7, convex and concave structures are developed for capacitors and inductors; wherein the deltas are $\pm 20\%$, $\pm 3\%$ and $\pm 1\%$. The δ (%) of $\pm 3\%$ and $\pm 1\%$ are the transformations induced by thermal stress while δ (%) of $\pm 20\%$ are the transformations caused by bending flexible structures. By EM simulation, the electrical characteristics of transformed capacitors and inductors are generalized in Fig8, Fig9, Table2 and Table3. As a result, the electrical variations between the straight and transformed cases are estimated and are noted in parentheses. In conclusion, the electrical variations induced by thermal stress are lower than 6% but those caused by bending are higher than 20%. From table 2 & 3, the electrical variations of capacitors are much more than inductors because capacitors are sensitive to transformations. Thus the design for compensation will be considered in the future.

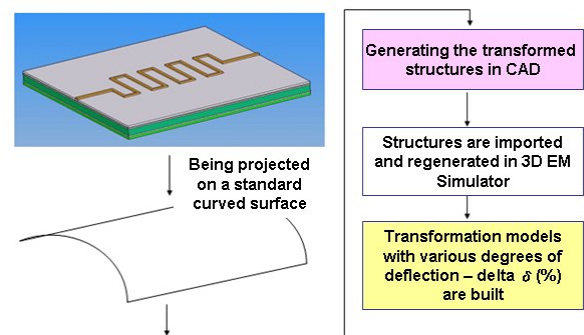
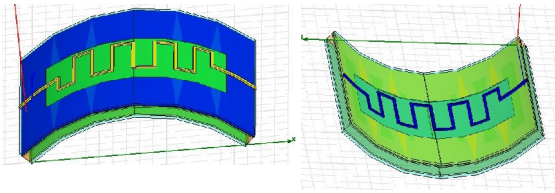
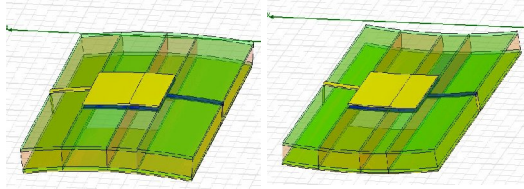
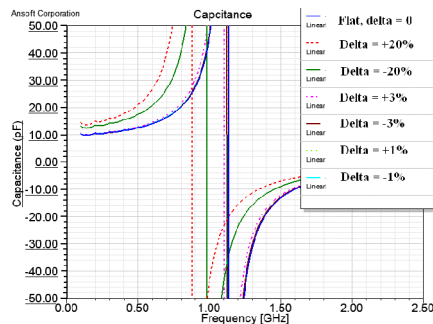


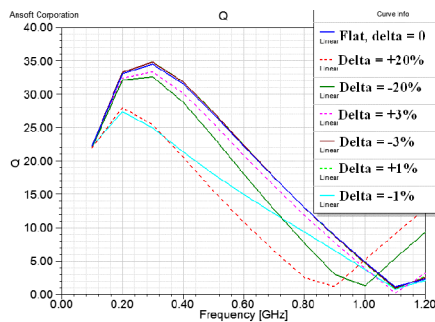
Fig.6. The concept of building transformation models



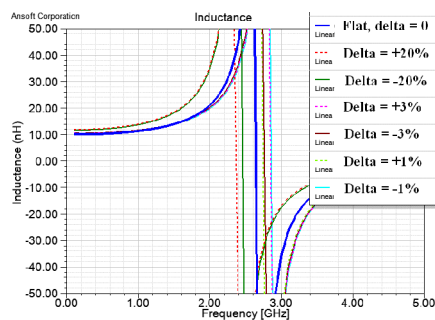
(a) The convex inductor, (b) The concave inductor

(c) The convex capacitor, (d) the concave capacitor
Fig.7. Transformed structures

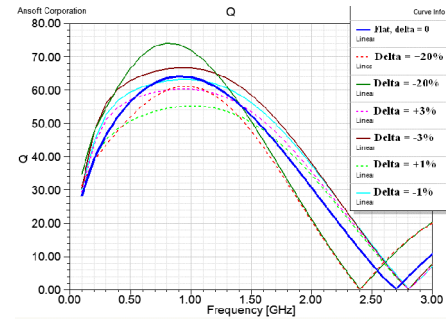
(a) Capacitance vs frequency



(b) Capacitor Q

Fig.8. Simulations of transformed capacitors

(a) Inductance vs frequency



(b) Inductor Q

Fig.9. Simulations of transformed inductors**Table.2 The conclusion of transformed capacitors**

Items \ $\delta(\%)$	Flat	+20%	-20%	+3%	-3%
C(pF) @ 0.1GHz	10.3	14.4 (+40%)	13.1 (+27%)	10.5 (+2%)	10.3 (-0.4%)
C(pF) @ 0.5GHz	12.6	21 (+67%)	17.6 (+39%)	13.1 (+3%)	12.6 (-0.2%)
SRF (GHz)	1.1	0.8	0.9	1.1	1.1
Q_{max}	34.5	28 (-19%)	32.6 (-5%)	33.3 (-3%)	34.8 (+1%)

Table.3 The conclusion of transformed inductors

Items \ $\delta(\%)$	Flat	+20%	-20%	+3%	-3%
L(nH) @ 0.1GHz	10.3	12.1 (+18%)	11.8 (+15%)	10.5 (+2%)	10.6 (+3%)
L(nH) @ 1.0GHz	11.4	14 (+23%)	13.7 (+21%)	11.6 (+2%)	11.7 (+3%)
L(nH) @ 2.0GHz	21	35.5 (+69%)	34.6 (+65%)	19.8 (-5.6%)	20.2 (-4%)
SRF (GHz)	2.6	2.3	2.4	2.8	2.7
Q_{max}	64.1	61 (-5%)	74 (+16%)	60.3 (-6%)	66.7 (+4%)

Conclusions

The characteristics of embedded capacitors and inductors are investigated in this paper. The parasitic effects between passive components and surroundings are analyzed through simulation, circuit and measurement models. In addition, the transformations caused by thermal stress and bending stress are also investigated. We have explored the key issues of building 3D transformation models. With these models, the variations between deflected and straight structures are estimated. As a result, the feasibility of embedded passive is verified for the applications of flexible multi-layer PCBs. These passive models will also support the design of circuit modules such as power amplifier and RF front-end circuits.

References

- [1] W. J. Borland and S. Ferguson, "Embedded Passive Components in Printed Wiring Boards, A Technology Review," DuPont i-Technologies
- [2] C. L. Weng, C. K. Wu, etc, "2.4GHz Power Amplifier Design with Embedded Passives in Printed-Circuit Boards," *Electronics Spectrum*, The Newsletter of EDMA, Vol.8, num. 2, Dec.2002, pp. 50~58.
- [3] C. L. Weng, P. S. Wei, etc, "Embedded Passives Technology for Bluetooth Application In Multi-layer Printed Wiring Board (PWB)," *Proc. 54th Electronic Components and Technology Conf.*, Las Vegas, Nevada, May. 2004.
- [4] C. S. Chen, S. F. Liu and C. K. Wu, etc, "Embedded Capacitors Technology in 2.4GHz Power Amplifier with Multi-Layer Printed Wiring Board (PWB) Process," *Electronic Materials and Packaging*, 2002. *Proceedings of the 4th International Symposium on Electronic Materials and Packaging*, 4-6 Dec. 2002, pp. 348-355.
- [5] Uei-Ming Jow, Shyi-Ching Liao, Ying-Jiunn Lai, etc, "Cost Effective SiP Solution for the RF Wireless Applications". IMAPS'2004.
- [6] U. M. Jow, Y. J. Lai, C. L. Weng, C. S. Cheng, and C. S. Shyu, "Functional Embedded RF Circuits on Multi-layer Printed Wiring Board(PWB) Process," *Proc. 55th Electronic Components and Technology Conf.*, Lake Buena Vista, Florida, May. 2005
- [7] C. H. Tsai, C. S. Chen, C. L. Wei, K. C. Chin, W. T. Chen, and C. S. Shyu, "Embedded Passives in Multi-dielectric Layer Printed Wiring Board for IEEE 802.11a/b/g Tri-mode Dual-band Wireless Carbus Adapter," *Proc. European Microelectronics and Package Conf.*, Oulu, Finland, June. 2007.
- [8] D. Pozar, "Microwave Engineering", 2nd Ed., John Wiley, 1998.