

Development of Thin LSI Embedded Circuit Boards

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Abstract

In recent years, electronics manufactures and PWB manufactures have focused attention on active LSI embedding technology as a key technology to achieve further downsizing of electronics system and electronic module. We have developed LSI embedding technology by simultaneous laminate process, using newly developed testable LSI chip carrier. This paper discusses 1st level reliabilities of thin LSI chip carrier and 2nd level reliabilities with PWB embedded structure, then describes that electrical performances of LSI embedded circuit boards is excellent through comparative examination with surface mounted circuit boards using by simulation study.

Key words: flip-chip technology, LSI Carrier, LSI embedded, NCP, simulation

I. INTRODUCTION

Recently highly efficient miniaturization in electronics progresses remarkably on strong demand for adapt to electronics evolution. In the semiconductor packaging technology, SiP(System in Package) is spreads enough in compose the module, such as GPU or CPU-core systems, witch required high-speed interface in order to achieve high-speed signal transmission. Several active bare or packaged chip and passive parts mounted side-by side on the substrate is typical example of these practical use¹⁾. And POP (Package on Package) technology, 3-dimensional stacking of memory package and SoC package is also another example of SiP. On the other hand, in the printed circuit board mounted with a lot of passive components, passive parts embedding technology was already introduced especially to the sub-set module of cellular phone, such as camera module, in order to aim improvement of technical function, maintaining a specified form factor. Furthermore, LSI embedding technology, using low pin count bare LSI and processed to WLP, were putted to practical use in some set application²⁾.

In this paper, potentials for practical use of newly

developed high-pin count LSI carrier embedded PCB are described using reliability data and electrical characteristics consideration.

Outline of Basic Technology for LSI embedding

Testable LSI carrier formation procedure

In this study, carrier substrate is newly developed to embed 400 pin class bare LSI into the printed wiring board. Carrier substrate is fabricated using B2it (buried bump interconnection technology) technology, cultivated more deeply for the purpose to embed large number of pin count LSI. This substrate consists of design rule, L/S=30/30 micros and 80 microns diameter for the interconnection of Ag paste between both metal lands. Dielectric body is consisted with 40microns thickness epoxy-pre-preg and has excellent performance such as high heat resistance due to its intrinsic properties, in other words these are low CTE and high Tg (Glass transition temperature).

Fig.1 shows the outline of assembly process of bare LSI with carrier substrate to embed circuit board. Firstly, Au stud bumps are formed in all Al pads on a wafer. Secondly,

wafer is back-grinded to 90 microns thickness, and LSI is singulated consequently using dicer machine. Thirdly, singulated LSI with Au stud bump connected to carrier substrate by using flip-chip technology with NCP (Non-conductive paste). Fourthly, whole region of carrier substrate, in which LSI attached side is encapsulated with dielectric film to have low warpage performance of thin LSI carrier after singulation process. Lastly, formation of LSI carrier is completed by lead-free solder bumping in external-electrode on the back side of substrate and package singulation process performed.

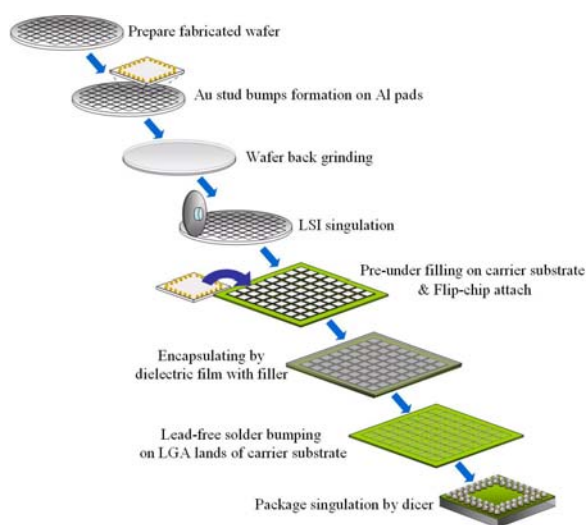


Fig.1 Testable LSI carrier formation procedure

Figure 2 shows the photograph of LSI carrier that converted 7.3mmSQ size LSI into 9.4mmSQ size chip carrier package. Because this chip carrier may have external terminal of the JEDEC standard formats to test functions (AC) test using conventional socket, equal with wafer level package or fine-pitch BGA.

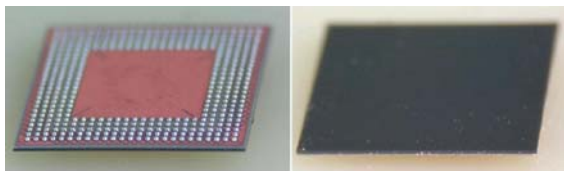


Fig.2 Photograph of LSI carrier package

LSI embedding procedure using by simultaneous laminate B2it technology

Figure 3 shows the process flow of LSI embedding

method by simultaneous laminating using B2it technology. First of all, four layers wiring board is prepared to mount LSI carrier. Secondly, Lead free solder paste is supplied on terminals of piece units of circuit board, which qualified through visual inspection and electrical inspection. After LSI carrier mounted by chip mount equipment, interconnection between terminals are finished through IR reflow process. Finally, four layered circuit board and two layered circuit board are prepared, and adjustment processed using X rays, LSI embedded process and Ag-bump piecing process are finished by one-time heat pressing. This large pin-count LSI embedding method made by simultaneous laminate technology is extremely simple compared with usual sequential build-up, witch spreading industrial method.

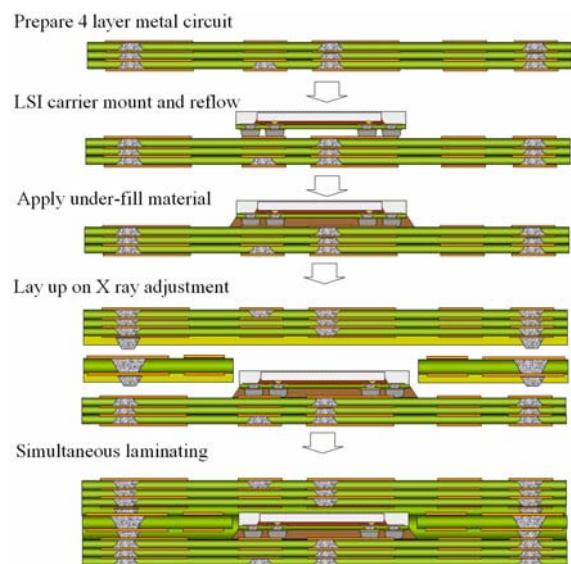


Fig.3 LSI embedding process

This large pin-count LSI embedding method made by simultaneous laminate technology is extremely simple compared with usual sequential build-up, therefore it is possible to product by the short delivery of date holding high yields.

II. EXPERIMENT AND RESULTS

Specimen design and preparation I

The specimen designed to investigate 1st level reliability of LSI carrier package, as shown in Fig.4, with high Tg

PCB substrate of 70 μ m thickness and 90 μ m thickness of silicon LSI, bonded by 384 Au stud bumps joint. Total thickness of LSI carrier package is 200 to 210 μ m without solder bump height. Au stud bump diameter and pitch of flip-chip inter-connections are 50 μ m and 75 μ m (L/S=35/35 μ m), respectively. Au stud bump inter connections are distributed forming peripheral region of 7mm SQ silicon die and are daisy chained to monitor the 1st level interconnect reliability.

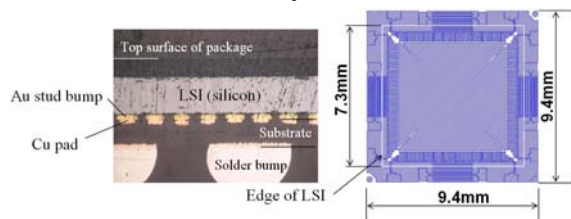


Fig.4 Specimen for 1st level reliability test

First level reliability of testable LSI carrier

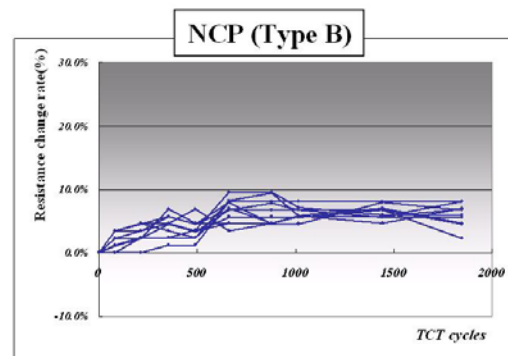
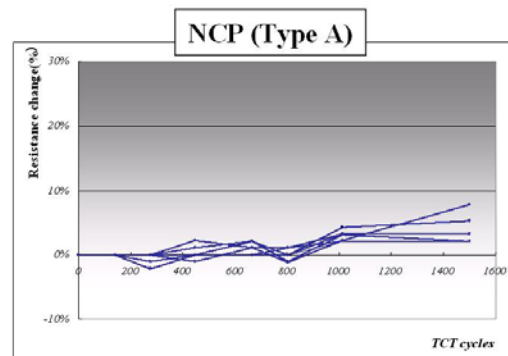
Specimens are prepared for two different NCP (Non conductive paste) under-fill materials, shown in Table I.

Table I Material properties of NCP

Material	Glass transition temperature (Tg)	C.T.E.($\alpha 1$)	C.T.E.($\alpha 2$)	Flexural modulus
Unit	degree	ppm/degree	ppm/degree	Gpa
Type A	145	35	100	8.5
Type B	172	30	120	6.6

Two type of NCP, physical-properties value shown in table I evaluated by thermal cycling test. Thermal cycling test performed using LSI carrier package as in Fig.4 where 10 specimens can be cycled simultaneously, according to JEDEC JESD22-A104 Specifications for Temp Cycle Test Condition B(-55deg C to 125deg C).

Graph 1 shows the result of thermal cycling test of specimens constituted with two kinds of NCP. It turns out that sufficient reliabilities are held both kind of specimens, exceeds 1,000 cycles. Of course, it is also important to consider physical properties of encapsulating material molding LSI to obtain the result of excellent thermal cycling test. We will discuss this encapsulating material in the following chapter.



Graph1 Results of thermal cycling test

Evaluation of encapsulating material to control LSI carrier warpage

In order to mount thin thickness LSI carrier on the circuit board using the solder bump joint method, it is necessary to control the warpage of LSI carrier under reflow operation. Then, we investigated the influence that physical properties of encapsulating material give warpage of LSI carrier. Table II shows that physical properties, two kinds of encapsulation materials. Both type A and type B have equal low CTE and high flexural modulus, a point different characteristic is that type A has higher Tg than type B material.

Table II Physical properties of encapsulating materials

Material	Glass transition temperature (Tg)	C.T.E. ($\alpha 1$)	C.T.E. ($\alpha 2$)	Flexural modulus	Water absorption
Unit	degree	ppm/degree	ppm/degree	Gpa	%
Type A	215-220	12	40	20(@40degree) 2(@230degree)	0.5
Type B	165	18	-	15(@25degree) 1(@280degree)	0.8

We investigated the warpage behavior of LSI carrier, encapsulated with these materials, shown in table II by using shadow moiré method. In addition, as reference, non

encapsulated LSI carrier was added to conduct the experimental test. Fig.5 shows the warpage behavior of LSI carriers during reflow process. Under normal temperature, non-encapsulated LSI carrier and encapsulated by type B material show remarkable warpage phenomenon. Non-encapsulated LSI carrier becomes about 250 microns and type B becomes 190 microns in the amount of the maximum warpage respectively under the reflow process. The causes of initial (normal temperature) warpage are CTE mismatch of silicon and organic carrier substrate and thermal contraction of NCP curing reaction. Moreover, non-encapsulated LSI carrier and encapsulated by type B LSI carrier show that direction reverses behavior of warpage during reflow process. On the other hand, Type A LSI carrier holds up excellent flatness (about 100 microns in the amount of maximum warpage) from start to finish under the reflow process. Fig.6 shows isothermal diagram of LSI carriers under reflow process. From this diagram, we can check clearly that only type A is restored to warpage effectively.

From all of these reasons, warpage phenomenon that influences to solder joint reliability has a connection with Tg of encapsulation material.

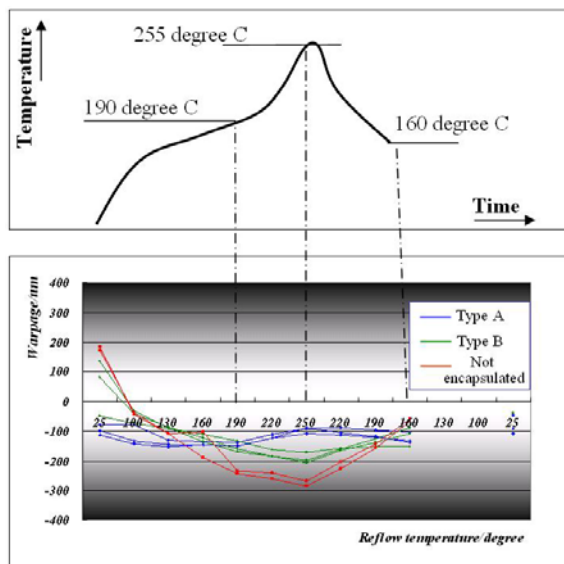


Fig.5 Warpage behavior of LSI carriers during reflow process

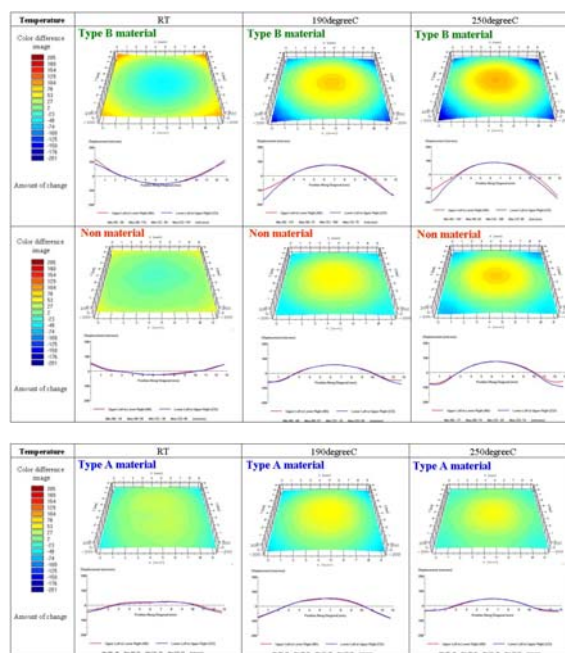


Fig.6 Isothermal diagram of LSI carriers during reflow process

Stand-off design to achieve soldered connection

Since the warpage of LSI carriers comes up to about 100μm at the melting point of lead-free solder, it is impossible to mount LSI carriers with low stand-off. Consequently, we investigate the optimum stand-off, where the target is 100μm, and the mounting process. Additionally, we also pose another target where the total height of the LSI carrier including connecting portion should be less than 320μm to achieve embedding into the PWB. Figure 7 shows the photographs of solder bumps made from solder balls on the bottom of the LSI carriers. Solder balls are attached on the lands, then melt through the reflow process. The diameter of the balls is smaller than the lands; however, solder is spread over a land through the reflow.

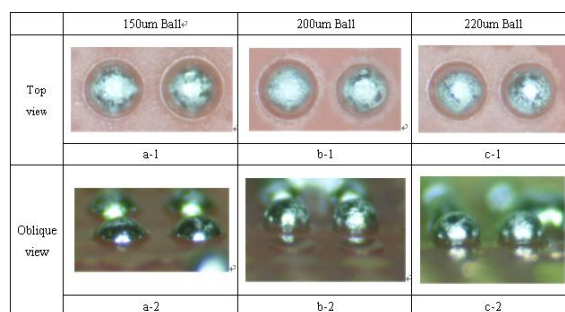
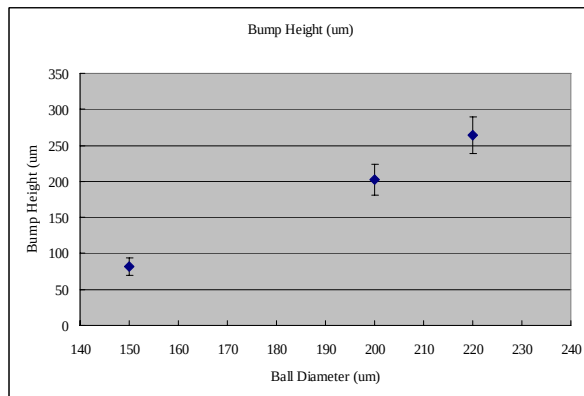


Fig.7 Photograph of solder bumps

Graph 2 shows the height of bumps with the diameter of solder balls. The stand-offs are calculated to be half of the height of the balls, assuming a bump is parabolic cone on a LSI carrier and then cylindrical when the carrier is mounted on a PCB. This graph indicates that it is possible to obtain arbitrary bump height from 80 μm to 260 μm if we select the ball of the size from 150 to 220 μm .



Graph2 Bump heights with ball diameter

We examined the adequacy of solder joint strength formed with each size ball. Table III shows the result of the ball shear test on solder bumps. It shows that solder bumps have enough adhesion to carrier substrate in all ball sizes.

Ball	150um	200um	220um
Average	53.3	47.5	54.1
3 Sigma	22.2	5.0	11.6
Unit	MPa	MPa	MPa

Table III Ball adhesion on ball shear test

The height of the most outside lands from the most inside ones is important issue. It is necessary that bumps and stand-offs are high and large enough comparing with these gaps for mounting LSI carriers. Table IV shows the gap measured on 3-D surface profiler where the thickness of LSI and encapsulating material on silicon are 90 μm and 30 μm respectively. The bumps are expected high enough for mounting LSI carriers with solder ball of 200 μm and 220 μm . However, balls of 150 μm are not enough for the mounting of LSI carriers. The calculated is expected about 40 μm , that is, it is less than the maximum gap.

Item	Value μm
Average	47.0
3 sigma	18.7
Max	59.1
Min	33.9
	μm

Table4 Height dispersion of all lands

Fig.8 shows the relation of stand-offs with ball diameter measured with 3-D surface profiler. It is resulted that 200 μm solder ball brings 100 μm of stand-off, i.e. the target stand-off. On the other hand, the stand-off includes large 3 sigma. It comes from the warpage of both the LSI carrier and the PWB at the reflow. Beside, fig.8 shows that it is easy to control the stand-off on the ball mounting process. The stand-off is calculated with assuming that a connection bump is cylindrical with the same diameter as the land and has the same volume as the solder ball. The calculation of result agrees consistently with experimental studies. The total height of the LSI carrier from PCB is 430 μm . It is taken place with the warpage of both the LSI carrier and the PWB.

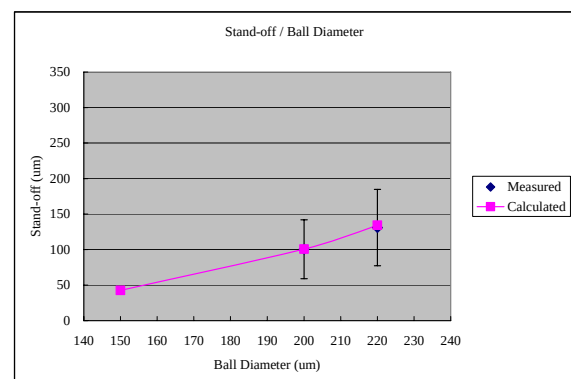


Fig.8 Relation of stand-offs with ball diameter

Specimen design and preparation II

The specimen designed to investigate 2st level reliability of embedded LSI carrier package, as shown in Fig.9, with B2it 8layers laminate board of 600 μm total thickness. 90 μm thickness of silicon LSI, bonded by 384 SAC305 balls joint embedded in this one. Each top surface covered with green solder resist and ENIG treatment was done only to the measurement terminals.

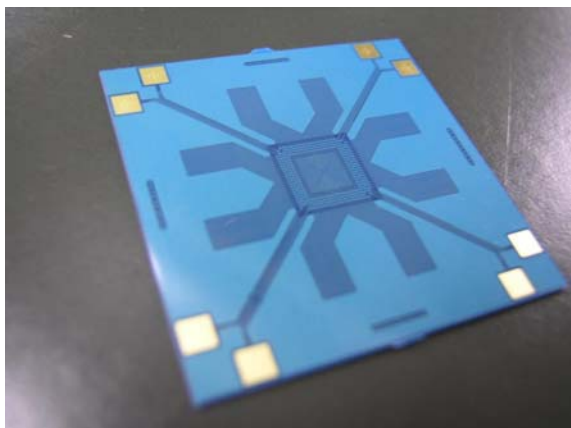


Fig.9 Specimen for 2nd level (embedded) reliability test

Fig.10 shows that cross-sectional view of fabricated LSI embedded PWB shown in the Fig.3. It is shown that both lands of 350um pitch are maintaining the good connection status with lead-free solder (SAC305) bumps. And we can check the 80um thickness and 7.3mm SQ size LSI is not broken by the heat press of lamination process.

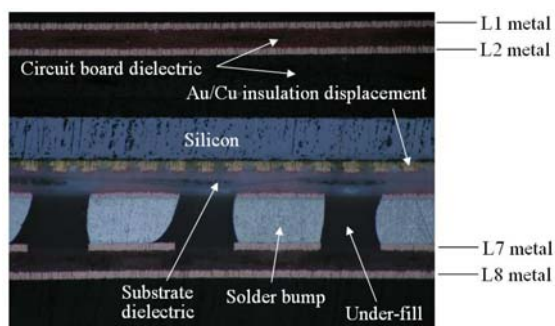


Fig.10 Cross-section of thin LSI embedded PWB

Second level reliability of embedded LSI carrier

JEDEC Level 3 floor plan and IR reflow were already passed. Thermal cycling test and high temperature storage test are executing now. We will review results of these acceleration tests at oral session of IMAS2008.

III. STUDY of ELECTRICAL CHARACTERISTIC OF EMBEDDED ACTIVE DEVICE

We investigated electrical properties of the PCB with embedded active device using simulation technology.

Fig.10 shows the front and cross section figures of the substrate with embedded LSI applied to this simulation study. A carrier converted CPU is embedded in the substrate, and four DDRII-DRAM are mounted on the substrate top surface, opposed to external terminal of embedded CPU. Embedded CPU possesses 400pin external terminals, signal I/O of these are connected with DDRII I/Os by SSTL-18 (1.8volts) interface. And surface mounted packaged CPU model was applied referring to this electrical simulation study.

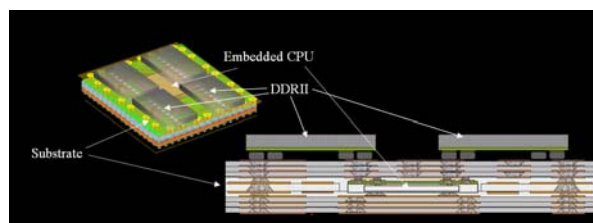


Fig.10 Structure of LSI embedded PCB

Table5 shows that result of extracted parasitic parameters of typical signal net, based on the wiring layout data of embedded substrate and SMT structured substrate. The point of special mention is that all parameter's values are small compared to referred SMT structure, because that can connect the signal lines by the short length when LSI embedding structure adopted. Another point is that to packaging CPU of 400pin class, it is necessary to interpose that by four metal layers substrate that has fine pitch circuits. Therefore, these complex routings including of package wiring enlarges parasitic parameters.

Table5 Parasitic parameters of wiring net

<Worst Case>	Length[mm]	delay[sec]	R[ohm]	L(Self)[H]	C(Self)[F]	G(Self)[S]
EMBEDDED LSI	9.53	9.62E-13	0.38	2.19E-09	4.53E-12	2.82E-04
Surface Mount	30.48	2.93E-10	1.88	1.38E-08	6.31E-12	3.75E-04

Figure 11 shows the result of current and voltage wave form in receiver edge for DQ(data) signal by using SPICE simulation. The left figure shows CPU embedded structure and the right one shows the surface mount structure. The

big ringing and over/under shoot phenomena of current and voltage were observed in surface mount structure model (right figure). These phenomena originated by loading impedance (especially inductance and capacitance) of wiring and impedance mismatch of board trace and PKG trace. On the other hand, clear current and voltage wave can be obtained in embedded structure (left figure), because the characteristic impedance (Z_0) of wiring and I/O impedance can be easily adjusted. This fact indicates that layout design of wiring considering signal quality is very easy when embedded structure applied to high speed module.

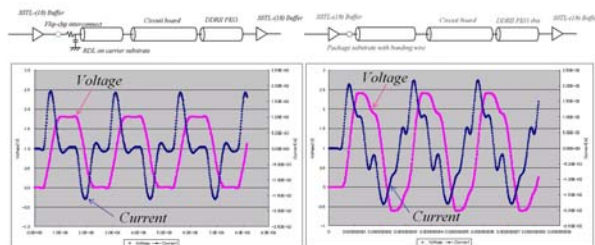


Fig.11 SPICE wave form of DQ-line signal

Fig.12 shows SPICE wave form of surface mount structure when ODT(On-Die-Termination) function of DDR turned on and dumping resistor (R_s) was inserted in series. The signal wave form becomes relatively clear by effect of ODT function and inserted dumping resistor, power consumption of system increased by generation of heat in the termination and dumping resistors respectively.

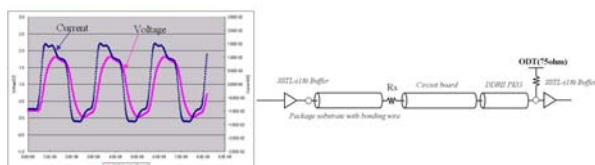


Fig.12 SPICE wave form of DQ-line signal for surface mount structure after ODT function and dumped resistor are added

Fig.13 shows the result of simulated Crosstalk voltage of seven signals with high wiring density. Either model of embedded structure and surface mount has low enough noise voltage either. CPU embedded structure shows extremely little noise levels both near-end and far-end

compared with surface mount one. This noise reduction effect of embedded structure originates in reduce of the interconnected wiring length on dielectric material each layers. These results demonstrate that LSI embedded structure have excellent performance equivalent to quasi-3 dimensional stacked structure (i.e. Through Silicon Via structure).

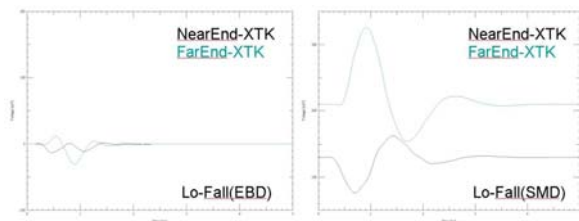


Fig.13 X-talk noise voltage of embedded structure (left) and surface mount structure (right).

Fig.14 is the photograph of substrate with embedded CPU base upon this study. 400 pin CPU is embedded in eight metal layered substrate.

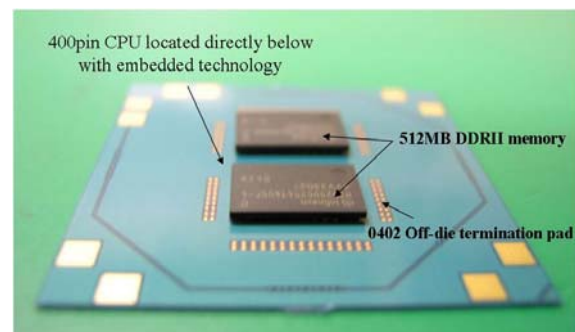


Fig.14 Fabricated CPU module with embedded active device by simultaneous laminate technology

IV. CONCLUSION

We developed LSI embed technology, handling up to 400pin class bare LSI using by simultaneous B2lit laminate method. The warpage is reduced by controlling physical properties of carrier substrate, under-fill and encapsulation material for the chip below 100um thickness. Consequently, it is possible to embed thin thickness and large number of pin-count LSI that cannot be achieved using by conventional wafer level CSP.

We investigated electrical properties of CPU embedded module, using newly developed LSI embedding method.

We verified some outstanding characteristic of embedded structure, using by simulation technology. The electrical access performance with DDRII is superior to that of conventional SMT technology.

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