

Using Embedded Capacitance to Improve Electrical Performance, Eliminate Capacitors and Reduce Board Size in High Speed Digital and RF Applications

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Background

The global electronics industry has continued to exhibit a widespread and growing interest in the technology of embedded passives. This interest can be attributed to three primary benefits. First, embedded passives have far less parasitic inductance than discrete components, which enables electrical performance advantages. Second, embedding saves surface real estate, which allows for board size reductions or the ability to add more functionality into the same area. Third, the incremental cost of embedding additional passive components is typically negligible, which suggests the potential for system cost reduction in designs with high passive component counts.

3M™ Embedded Capacitor Material is a high performance embedded passive material intended for embedded capacitor applications. It is a copper-clad laminate which utilizes an ultra-thin, high K-value dielectric material between the copper planes to deliver a capacitance density of over 6 nF/in².

This presentation will focus on this laminate material and how it can be used to improve electrical performance and reduce board size (by replacing discrete capacitors), and will also address the impact on PCB reliability and system cost.

Electrical Performance Advantages

Moore's law continues to drive the semiconductor industry, shrinking feature sizes and sending transistor counts higher. Along with these changes comes lower operating voltages and increased current requirements.

These trends place severe demands on the ability of the circuit board to distribute power to the surface-mounted active devices. The circuit board's power distribution system must meet increasingly low impedance requirements.

The typical components of a circuit board's power distribution system include a switching power supply, bulk decoupling capacitors, high frequency decoupling capacitors and inner layer power and ground planes. One of the best ways to improve power distribution (i.e. decrease impedance) is to use closely spaced power and ground planes within the multilayer board stack up. This approach has been used for over 20 years with FR-4 dielectrics in the range of 2 to 4 mils in thickness.

The use of thinner, high dielectric constant (k) dielectrics can significantly increase the effectiveness of this approach. Standard FR-4 technology is limited to 2 mils thickness, a k value of approximately 4 and a capacitance density of only 0.5 nF/in². Thinner (<25 um) dielectric materials, especially those filled with high dielectric ceramic particles, are now being used to address the power distribution issues of today's high frequency designs.

One such material is 3M's embedded capacitor material, offered in a range of dielectric thicknesses from 8 to 14 microns (0.31 to 0.55 mils) and a k of 16. In combination, these features deliver a high capacitance density of 6.4 nF/in² to 11 nF/in² and offer many benefits when used for decoupling high speed digital electronics, including:

- o Lowers impedance of power distribution system
- o Dampens board resonances
- o Reduces noise on power plane
- o Reduces radiated emissions
- o Replaces large numbers of discrete decoupling capacitors

From a designer's perspective, noise margins are increased, which can translate into improved performance and less engineering time devoted to troubleshooting and fixing noise problems. In addition, the component count reduction saves time in board layout.

Examples of Electrical Performance Improvement in High Speed Digital Board Designs

Below are several examples of high speed digital board designs that used ultra-thin dielectric with a

dielectric constant (k) of 16 for distributed decoupling (power-ground) in multilayer rigid printed circuit boards.

In the first example (Figure 1), the self-impedance of a 5" X 10" multilayer bare board with ultra-thin (8 μ m) dielectric between the power and ground planes is compared to the same board design with 50 μ m (2 mil) thick FR-4 and 25 μ m (1 mil) thick FR-4 dielectric between the power and ground planes.

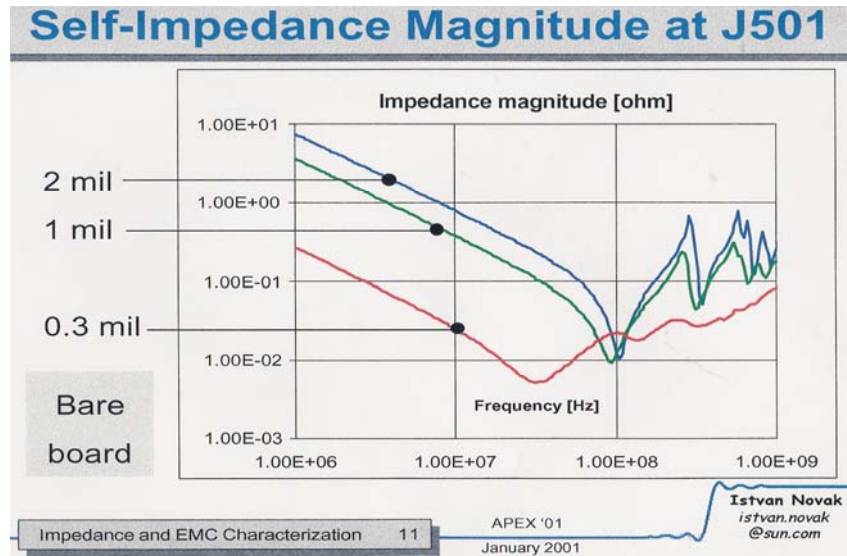


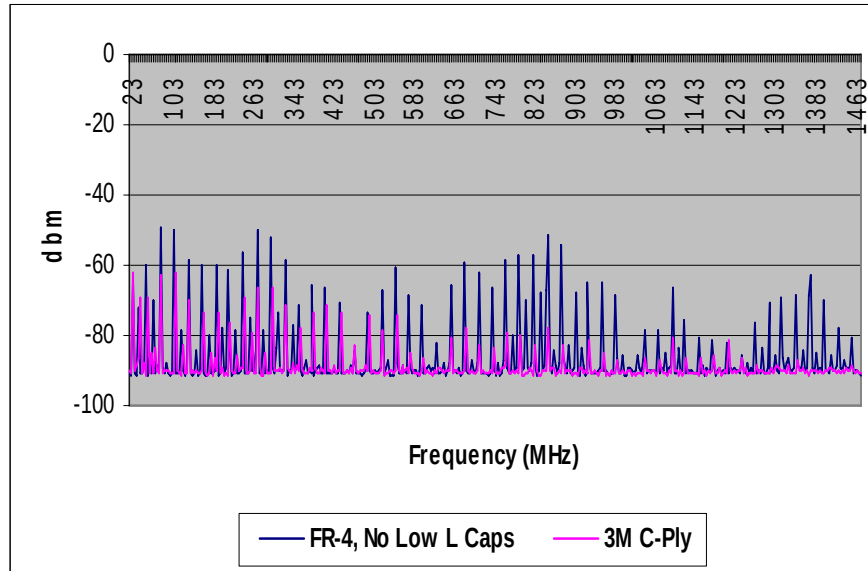
Figure 1 – Self-Impedance vs. Frequency
(Courtesy of Sun Microsystems)

At lower frequencies, it can be seen that the self-impedance of the ultra-thin laminate material is more than an order of magnitude lower than that of 1 or 2 mil thick FR-4. This is due to the much higher capacitance density of the ultra-thin material (~ 10 nF/in² vs. $\sim 0.5 - 1$ nF/in²). At higher frequencies, the self-impedance of the ultra-thin dielectric material is also significantly lower than that of the 1 or 2 mil FR-4 laminate. This is primarily due to the significantly lower self-inductance of the ultra-thin material. Finally, in the 100 MHz to 1 GHz frequency range, both the 1 mil and 2 mil FR-4 laminates show very large impedance spikes caused by board resonances. These are very undesirable as the noise associated with these impedance spikes can trigger false switching, signal integrity and EMI issues. However, in the case of the ultra-thin dielectric, the board resonances are almost

completely damped due to the high copper losses of closely spaced power and ground planes at high frequencies.

In figure 2, the noise versus frequency was measured on a fully assembled daughter board with an approximate size of 5" X 5". The noise was measured on the 1.5 volt plane up to a frequency of ~ 1.5 GHz. The daughter card had a MIPS R14K processor running at 550 MHz and 9 secondary cache SRAMs running at 275 MHz.

Two board designs were compared. The first had a 3 mil FR-4 dielectric thickness between power and ground planes and the second board had an 8 μ m dielectric thickness (with a k of 16) between power and ground planes.



**Figure 2 – Power Bus Noise vs. Frequency
(Courtesy of H.P.)**

As can be seen in Figure 2 above, the board with the ultra-thin dielectric had significantly less noise at all frequencies above ~50 MHz. At frequencies above 500 MHz, the board with the 3 mil FR-4 still had a large amount of noise whereas the board with the ultra-thin dielectric had extremely effective noise dampening above 500 MHz. Over the frequency range measured, the board with the 8 μ m dielectric (k of 16) had 13.3 dB less noise than that of the board with the 3 mil FR-4 power ground plane.

The peak-to-peak voltage ripple was also measured on these boards. For the case of the board with the 3 mil FR-4 power-ground plane spacing, the peak-to-peak noise was 235 mV (15.7% of 1.5V). For the board with the 8 μ m power-ground spacing, the voltage ripple was 114 mV (7.6% of 1.5V), or slightly less than one-half of that of the 3 mil FR-4 board.

As part of the National Center for Manufacturing and Sciences (NCMS) Embedded Decoupling Capacitance (EDC) industry consortia, power bus noise and voltage fluctuation were measured by the University of Missouri at Rolla. The six metal layer boards were 2" X 3" in size. Each contained a 50 MHz oscillator, a 22 μ F bulk decoupling capacitor, eight octal clock drivers and a number of load capacitors.

The materials used for layers 3 (power) and 4 (ground) of the boards were various embedded

capacitance laminate materials including 2 mil FR-4 (BC2000TM) and the 3MTM Embedded Capacitor Material (5 μ m; k of 16). These boards were compared to a baseline board with an approximate 4 mil FR-4 laminate used for the power-ground core.

None of the boards with embedded capacitance laminates were surface mounted with any decoupling capacitors beyond the 22 μ F bulk decoupling capacitor. The baseline board was surface mounted with 33, 0.01 μ F high frequency decoupling capacitors (total of 330 nF). The amount of embedded capacitance for the 2 mil embedded capacitance board was ~3 nF and was ~107 nF for the 5 μ m embedded capacitance laminate board.

First, the 5 μ m laminate board (with no decoupling capacitors) was compared to the 4 mil FR-4 baseline board, with and without the 33, 0.01 μ F decoupling capacitors over the frequency range of 1 MHz to 5 GHz (Figure 3). Here it can be seen that the .01 μ F decoupling caps did a reasonably good job decoupling in the 1 MHz to 1 GHz range on average. However, at frequencies beyond 1 GHz, the decoupling capacitors are completely ineffective due to their high inductance. The 5 μ m laminate did a much better job of decoupling across the entire frequency range (10 to 40 dB noise reduction) even though it had only one-third of the capacitance (107 nF vs. 330 nF) of the SMT decoupling capacitors.

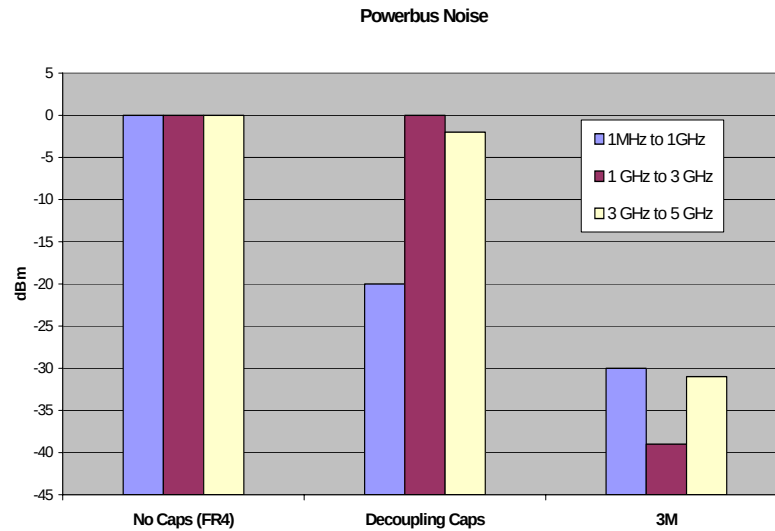


Figure 3 – Power Bus Noise
(Courtesy of University of Missouri at Rolla)

Power bus voltage ripple measurements were also taken on the embedded capacitor and baseline 6 metal layer boards. Below (Figure 4) the amount of voltage fluctuation from the nominal 3.3 volt power

plane are shown in the time domain for the 4 mil FR-4 baseline board with 33 decoupling capacitors, the 2 mil FR-4 board and the 5 um board.

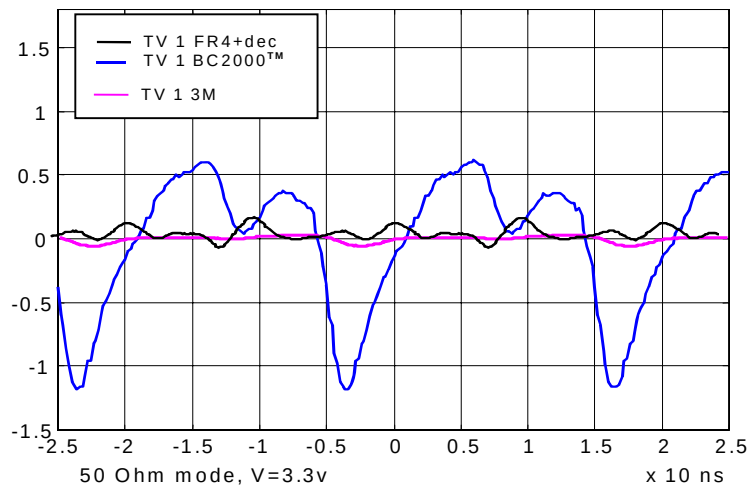


Figure 4 – Power Plane Voltage Fluctuation
(Courtesy of University of Missouri at Rolla)

The peak-to-peak voltage ripple for the baseline board with SMT caps, the 2 mil FR-4 board and the 5 um board were 214 mV, 1740 mV and 89 mV respectively. The board with the 5 um embedded capacitance material had less than one-half the voltage ripple even though it had less than one-third of the capacitance of the SMT caps. The board with

the 2 mil FR-4 embedded capacitance had such a large voltage fluctuation that it did not function properly. This was due to the lack of sufficient embedded capacitance to provide charge to the IC until the bulk decoupling capacitor could provide charge.

Board Size Reduction and Capacitor Elimination in High Speed Digital Board Designs

3M's embedded capacitor laminate material has been successfully implemented on a number of OEM designs to replace large quantities of discrete decoupling capacitors from the board surface. Some of the data from these board designs is shown in Table 1. Here it can be seen that in every case, the use of the embedded distributed capacitance allowed the elimination of at least 60% of the discrete

capacitors. In most cases it was at least 75% and in two cases, all of the discrete decoupling capacitors were removed. In one case, over 500 capacitors were eliminated from the board design. It is also very important to note that only a very small amount of embedded capacitance was needed to replace a very large amount of discrete capacitance (each nF of embedded capacitance replaced 10 to 40 nF of discrete capacitance).

Table 1

Design	Discrete Capacitance Removed (nF)	Embedded Capacitance (nF)	Ratio of Removed to Embedded	% of Total Discrete Caps Removed
EDC TV1	330 <i>33 x 0.01 uF</i>	105	3.1	100%
OEM A	12,600 <i>126 x 0.1 uF</i>	300	42.0	>75%
OEM B	6,310 <i>62 x 0.1 uF 11 x 0.01 uF</i>	210	30.0	>60%
OEM C	3,180 <i>29 x 0.1 uF 28 x 0.01 uF</i>	305	10.4	>75%
OEM D	52,900 <i>529 x 0.1 uF</i>	1970	26.9	>75%
OEM E TV	9,900 <i>99 X 0.1 uF</i>	660	15.0	100%
OEM F	~35,000 <i>443 total (mostly 0.1 uF)</i>	~1000	~35	100%

Table 2 provides additional information including the board size and number of embedded capacitor laminate cores used in each of these designs. From this it can be seen that this ultra-thin embedded capacitor material is capable of removing 3 to 6

capacitors per square inch of board surface area with only one or two cores in the board stack up. On larger sized boards, this can allow the elimination of well over 500 capacitors.

Table 2

Design	Board Layers	No. of 3M ECM Power-Ground Cores	Approx. Board Area (in ²)	Total No. of Caps Removed	Caps Removed per sq in
EDC TV1	6	1	6	33	5.5*
OEM A	12	1	35	126	3.6
OEM B	10	2	17	73	4.3
OEM C	8	2	12	57	4.6
OEM D	14	2	121	529	4.4
OEM E TV	4	1	120	99	0.8*
OEM F	14	2	~100	443	~4.4*

* indicates that 100% of high frequency decoupling capacitors were removed from board

All the OEM boards were tested and found to be fully functional. For two of the OEM design boards, the power bus noise was measured and found to be much improved (90 vs. 230 mV voltage ripple in one case and a 30 dB+ reduction in noise on the other). In the two OEM board designs where EMI was tested, there was no increase in EMI. One board had similar EMI and the other had a ~10-15 dB reduction in EMI.

In summary, the use of ultrathin, high k embedded distributed capacitance (as a power-ground core or cores) can replace a very large number of surface mounted decoupling capacitors. Typically, all decoupling capacitors under 0.1 uF can be removed as well as the majority of 0.1 uF decoupling capacitors. For high speed designs, this can result in the removal of many hundreds of capacitors. This is also very significant for portable and military products where the desire for board area reduction is paramount.

Board Size Reduction and Capacitor Elimination in RF Board Designs

The above data were examples of using embedded distributed (power-ground) capacitance to remove discrete decoupling capacitors in high speed digital designs. The 3M material can also be used in RF applications such as modules for cell phones to remove large numbers of capacitors.

In one such design where there was a significant RF noise issue, the material was used in place of discrete capacitors due to board size constraints. In this application where the embedded capacitor material was used for RF filtering, an extremely high density of capacitors (>50 caps/in²) were not required due to a combination of the high capacitance density of the material and the low capacitance requirements (<100 pF) of the capacitors.

In this case, the noise problem was very successfully solved (>20 dB reduction) and no board size increase was required due to adding discrete capacitors to the board surface. If the board had used discrete surface mount capacitors, the noise reduction seen may have been less (due to higher inductance) and it would have required a significant increase in board size and/or board layers.

The above program has been extremely successful. The embedded capacitance material was designed, tested, qualified and ramped to high volume production in 2006. In 2008, well over 100 million cell phones will have been manufactured with the ultra-thin (14 um), high capacitance (6.4 nF/in²)

material. This includes shipments to over 10 cell phone manufacturers around the world including several Tier 1 cell phone manufacturers.

Cost Reduction

The use of ultra-thin, high k embedded capacitance has the potential to lower the system level cost of many products. However, the assessment of potential system level cost reduction is very complex. Ultra-thin embedded capacitor materials currently cost significantly more than standard laminate material. They can also cost significantly more to process due to their material handling requirements. These increased costs may be offset by the ability to get more boards up on a panel or by a reduction in the total number of board layers. It may also be possible to combine two or more boards in a system into the same board. However, in general, unless there is significant board size reduction, bare board costs of embedded capacitor boards will be significantly more than traditional bare boards.

The use of ultra-thin, high k embedded capacitance laminates can also be used to eliminate large numbers of discrete capacitors from the board surface. When all of the costs associated with the drilling of the capacitor vias, and the purchase and assembly of the discrete capacitors (assembly, inspection, rework, etc.) are combined, it can represent a very significant cost reduction per board, especially if assembly can be reduced from double to single sided.

There may be additional cost reduction available with the use of ultra-thin embedded capacitor materials. Embedded capacitor materials can reduce or eliminate EMC issues. This may provide cost savings associated with EMI shielding and containment. Additional cost reduction is possible by fewer or shorter design cycles, but this can be difficult to quantify. Removing the discrete capacitors improves board long term reliability because solder joint and via failures are reduced. Bare board yields can improve due to the elimination of vias, board size reduction and increased routing space. On the other hand, material handling or other processing issues with embedded capacitor materials could have a significant negative effect on board yield. Another factor is that rework is not possible with embedded capacitor materials once the material has been laminated into a board.

In summary, some inputs into the cost comparison can be easily understood and quantified while many others cannot. Some factors increase the system level cost while others decrease it. There are also a

number of inputs that can increase or decrease system level cost depending on the material involved and the design and manufacture of the boards.

There are three important items to remember when considering potential cost reduction with the use of embedded capacitor materials. The first is to always consider total system cost, not bare board or assembled board costs. The second is to compare not only what the system level cost is at the current time but what it will be throughout the life of the product. Thirdly, it should be kept in mind that as the supply chain grows, gains experience, and becomes more competitive, the costs associated with the use of these materials will continue to decrease which will make system cost reductions possible in a greater number and variety of applications.

Reliability

A large amount of internal and external reliability testing has been completed over the last ten years. This includes numerous designs from a large number of PCB fabricators. Ultra-thin, high k embedded capacitor materials have shown to be a reliable material for use in multilayer rigid printed circuit boards. These designs have consisted of anywhere from four to over 40 metal layers with anywhere from one to approximately a dozen embedded capacitor cores.

Since 1996, many hundreds of multilayer boards from a large number of PCB fabricators have been tested using the following industry reliability tests seen in Table 3 below.

Table 3 – Reliability Tests

Electrostatic Discharge (ESD)
High Potential (HiPot)
Life (high temp exposure with bias)
Mechanical (bend)
Multiple Solder Float (288C)
Multiple Solder Reflow (incl. lead free)

Moisture/Reflow Sensitivity (Popcorn)
Temperature, Humidity (with and without bias)
Thermal Cycle
Thermal Shock
TMA 260 (time to delamination)
Vibration

Electrical tests and properties measured included capacitance, dissipation factor, insulation resistance/leakage current, and via resistance. The test results have been very positive. The ultra-thin embedded capacitor material passes all tests with no significant changes to electrical properties or issues with board reliability including plated-through-hole reliability. Visual inspection of boards from multiple fabricators has shown all of them to pass MIL-PRF-31032, even after 6 solder floats at 288C.

The only tests which had an effect on electrical properties were high temperature, high humidity tests. In these tests, both the capacitance and dissipation factor increased due to moisture absorption. After baking, these properties returned to their pre-test levels. The same effect was seen in boards with high Tg FR-4 power-ground cores. Overall, the reliability of the ultra-thin embedded capacitor material has been shown to be very similar to high glass transition temperature FR-4 power-ground cores. In some cases (ESD, TMA 260 and lead free reflow), they outperformed high Tg FR-4 materials.

Commercialization Status and Market Segment Interest

3M's embedded capacitor material (14 um) has been commercially available since April 2004 and does not require a license from 3M for use. The product is RoHS compliant, does not contain bromine and received UL certification in 2001. Manufacturing is done on a high volume production line at a 3M facility in North America. It has been used by over 80 printed circuit board fabricators across the globe.

Thinner and higher capacitance density embedded capacitor laminates are also being developed. These materials are available for use in limited quantities. Additionally, 3M is developing a resistor-capacitor (R-C) laminate material. In this case, one or both of the bare copper foils is replaced with copper foil having a thin-metal resistive layer. The sheet resistance of the thin-film resistor material is typically in the 10 – 1000 ohms per square. The obvious advantages of combining resistive and capacitive structures into the same substrate include cost reduction, space reduction and electrical performance improvements. However, other potential advantages include improved power ratings of the resistors (due to the close proximity of the additional copper layer), improved ESD resistance of

the embedded resistors as well as potential improvement in the embedded capacitance material abilities to dampen noise at high frequency (due to the presence of embedded resistor material adjacent to the dielectric layer where most of the current flow takes place).

Summary

Embedded passives can assist OEMs looking to improve electrical performance, reduce EMI, reduce the size, or lower the overall system cost of their products. Ultra-thin, high k embedded capacitor materials are especially good in meeting these objectives while still offering very high reliability, even in designs requiring lead free assembly.

References

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