

Reliability of Embedded Large-Area High-K Dielectric Capacitors in LTCC Substrates

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Abstract

Low-Temperature Co-fired Ceramic (LTCC) electronic substrates offer high density features such as integral electrical connections, backside printed resistors and embedded passive components all of which allow the substrate to shrink in overall size. Traditionally, high tolerance resistors and small (pico-farad) type capacitors were the only components considered for embedding into LTCC substrates. However, many automotive products require multiple high-value high-tolerance capacitors, as large as 100 nF that could be embedded, if a high-k dielectric could be successfully utilized. This paper summarizes the results of a study designed to evaluate the automotive under-hood reliability of large-area (up to 0.250 in²) embedded capacitors into LTCC substrates using a high-K barium titanate thick-film dielectric paste developed by DuPont Electronics.

Key words: Low Temperature Co-fired Ceramic (LTCC), automotive, embedded and capacitors

Introduction

Many of the automotive electronic products produced by Delphi Electronics & Safety require multiple discrete capacitors to accomplish functions that include electromagnetic interference (EMI) protection, power supply filtering, integrated circuit decoupling, and system bypass. These capacitors can vary greatly in capacitance value, but usually have a common ground connection and their tolerance requirements are in the 20-30% range. Due to the large number of these capacitors requiring placement and reflow soldering on the substrate surface, any possibility of embedding these capacitors within the substrate would be an attractive alternative.

In 2004, a two-year Indiana state government funded project was initiated to develop the design tools and processes for embedding capacitors using DuPont's high dielectric constant thick-film paste into LTCC substrates.

A follow-up project (the source for this paper) was then completed to utilize embedded capacitor technology to fabricate capacitors capable of being utilized in under-hood automotive products.

Three Delphi Electronics & Safety products utilizing LTCC substrates were identified as potential applications for embedded capacitors. Each of these products required multiple high tolerance surface mount capacitors of various capacitance values and mechanical sizes. The embedded capacitor technology required for all three products were documented and summarized as follows:

- » Capacitance density approaching 400 nF/in², 20% tolerance
- » X7R dielectric temperature and frequency response requirements
- » Reliability 1000 (-40 to 125°C) thermal cycles without shorts or opens and <10% change in measured capacitance value

- » Dielectric breakdown voltage > 50 volts
- » ESD Testing capability > 2kV
- » Use of standard LTCC substrate manufacturing processes

DuPont Electronics has recently developed a high dielectric constant barium-titanate thick-film paste with a dielectric constant of approximately 1500. Though still in the experimental development stage, it was the material of choice for embedding capacitors up to 100 nF in a 0.25 in² LTCC substrate. This report documents the initial research, design, development and testing of embedded capacitors in LTCC substrates capable of meeting automotive reliability requirements.

Chemistry of the Thick-film Formulation and the Fired Composite Structure

Major functional phases of the system include substituted solid solutions of ferroelectric materials and mixed relaxor ceramic materials. Also, addition of liquid-phase sintering aids in the formulation enables increased sintering and densification of the capacitor materials at the low temperature firing of 850 °C resulting in a less porous microstructure. The material system also includes cure point shifters and suppressors to minimize the temperature-coefficient of capacitance (TCC) of the fired devices. The selected organic medium allows easy organic “burn-out” before softening the glasses present in the laminates, and minimizes the delamination of the fired composites.

A typical temperature coefficient of capacitance of the buried capacitor is shown in Fig 1. The capacitor is terminated with compatible conductors and the capacitance is measured as a function of temperature using an automated measuring unit.

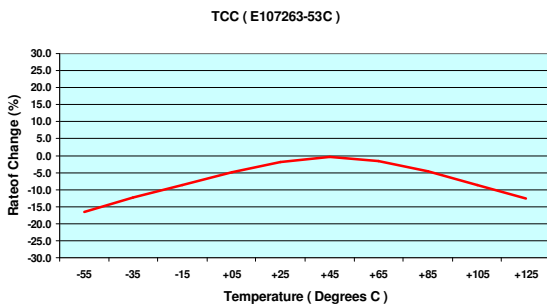


Figure 1: A typical TCC Curve for the Capacitor Buried within 951 LTCC Composite

The results show close to X7R characteristics for the capacitor when buried within the DUPONT 951 fired composites. The capacitor shows a dielectric constant (K) of 1900 with a dissipation factor (DF) of less than 2% when terminated with 951 compatible conductors. Thickness of the capacitor is measured from the Scanning Electron Micrograph (SEM) of the polished cross section of the capacitor for dielectric constant calculation.

The SEM microstructure of the fired LTCC composite is shown in Fig 2. The interfaces of (1) conductor-capacitor dielectric and (2) conductor-951 tape dielectric have no delamination and the over-all composite is densified with little / no significant porosity.

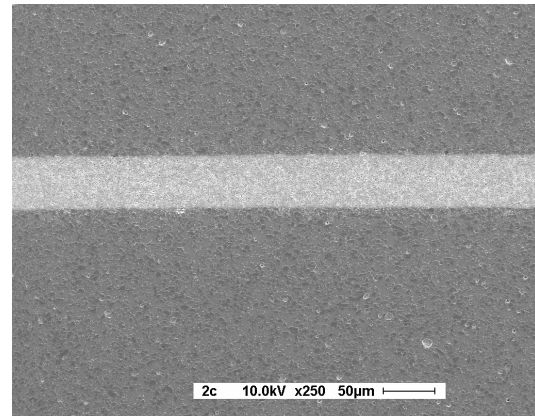


Figure 2: Microstructure of a Buried Capacitor within DUPONT 951 LTCC Composite

LTCC Technology / Processing

An LTCC test board was designed to evaluate the electrical performance and reliability of large-area embedded capacitors in automotive applications.

The test board was designated as Large-Area Capacitor test board #1 (LAC1) and was developed to test single-layer embedded capacitors in LTCC substrates. Figure 3 show the simple design concepts developed for the single-layer embedded capacitors. Three different sizes were designed based on varying substrate sizes of the target products. The largest single-layer capacitor size considered was for a LTCC substrate that is approximately 0.250 in² and a target capacitance of 100 nF. All three capacitor designs were based on a

single print of DuPont's K1800 high-K thick-film dielectric paste with a thickness of 20 microns.

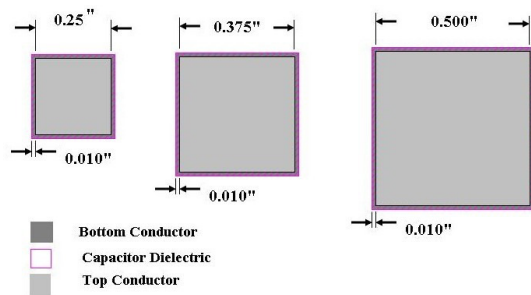


Figure 3: Large area capacitor single-layer design concepts

The lay-up drawing and material set for the large-area capacitor test board is shown in Figure 4. The boards were to be processed by CIS Microelectronics of Lafayette, IN, their inputs were key during the design phase to help insure a "flat" substrate could be fabricated. To minimize the impact of the added high-K dielectric thick-film within the substrate structure, four layers of DuPont LTCC tape were placed both above and below the printed capacitor layer. This type of substrate structure is well balanced with an equal number of layers above and below the dielectric layer. This tends to reduce the impact of the different shrinkage rates between the dielectric material and the DuPont 951 LTCC tape, thus resulting in an overall flatter substrate without blistering or dimpling of the surface.

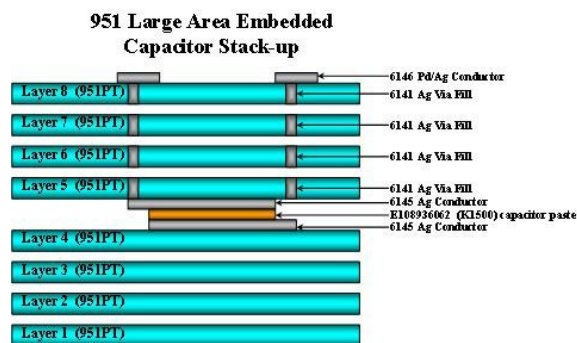


Figure 4: Lay-up drawing and materials for large-area capacitor test board

Another key processing parameter in maintaining a flat substrate is the firing profile.

Figure 5 contains the box furnace firing profile used to develop the LAC1 test substrates.

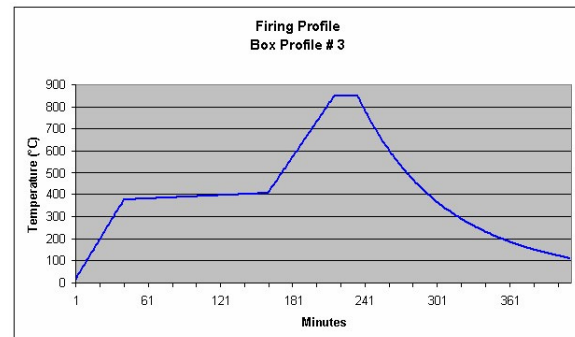


Figure 5: LTCC substrate firing profile

Screen printing was accomplished using a MPM TF-100 printer. To obtain a low film thickness for the high dielectric constant paste, a fine mesh screen was used to not only reduce film thickness but to also reduce possible pin-holing. As viewed in the Figure 6 photo, screen mesh marks appear prevalent. With the Hi-K dielectric paste being experimental, optimization of the paste rheology for this application had not yet been completed. A higher deposited paste flow rate adjustment in the paste formulation would aid in reducing the pin-hole effects and enable lower film thicknesses to be achieved.

During the early phases of screen printing at CIS Microelectronics, using DuPont's K1800 high-K dielectric paste, pin holes were detected in all the single layer screen prints of approximately 20 microns (dried) thickness (see Figure 6). Pin-holing within the dielectric has the potential to produce either direct shorts and/or very low breakdown voltages. To solve this problem a double print of the high-K dielectric paste was required. The double printing eliminated the pin holes - however it effectively doubled the dielectric thickness, thus reducing overall capacitance. All embedded single layer printed capacitors were thus affected. The target value for the 0.250 in² capacitor design was reduced from 100 nF to approximately 50 nF, due to the requirements for double printing the dielectric paste.

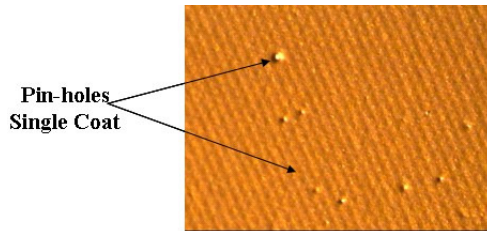


Figure 6: Single print of high-K dielectric print exhibiting pin holes

High-K Dielectric Thickness Confirmed

Cross-sections were completed on two of the large-area capacitors to determine the actual dielectric thickness of the high-K (DuPont K1800) thick-film paste. A dimensioned photo of one of the cross-sections is shown in Figure 7. Both cross-sections revealed the dual-printed dielectric thickness was approximately 38 microns. Recalculating the capacitance value for the 0.250 in² capacitor design using the actual measured thickness of 38 microns yielded a new target value of 56 nF.

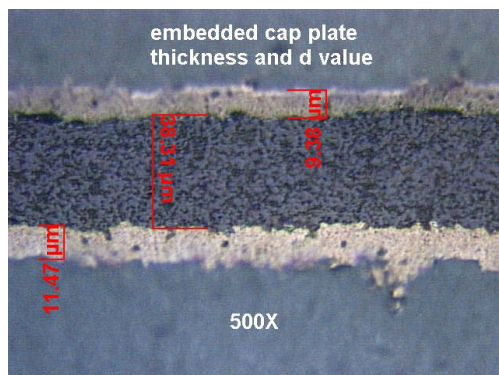


Figure 7: LTCC substrate cross-section indicating thickness of capacitor layers

Capacitor Electrical Evaluation

Initial capacitance values were measured on sixteen large-area single-layer capacitors for each of the three different capacitor sizes. The capacitance measurements were taken using an Hewlett Packard 4284A LCR meter with source amplitude of 1.0 VRMS at a frequency of 1.0 kHz. The averages for all readings, standard deviation and percent yield can be found in Table 1.

Capacitor Dimensions	Target Value	Capacitance Ave (nF)	Std. Dev.	% Yld	Calc. Dk
0.25" x 0.25"	14 nF	18.4	0.37	100	1960
0.375" x 0.375	32 nF	39.5	0.77	94	1870
0.50" x 0.50"	56 nF	66.6	1.11	94	1770

Table 1: Initial Capacitance measurements with calculated value for dielectric constant (Dk)

Calculating for the dielectric constant (Dk) yielded values of 1770 - 1960 for large-area capacitors utilizing the DuPont's 951 LTCC materials. The calculated Dk values represent a 18-30% increase over the original value (1500) used to determine the target capacitance value. Equivalent Series Resistance (ESR) is a measure of the total loss of a capacitor, usually defined at the self-resonant frequency where the capacitive and inductive impedances cancel each other out. Figure 8 contains a frequency sweep from an Agilent Precision Impedance Analyzer model 4294A. Measured at the self resonant frequency, the ESR for a 0.0625 in² large-area capacitor was 19.22 milliohm at 18.7 MHz. All average ESR measurements are summarized in Table 2.

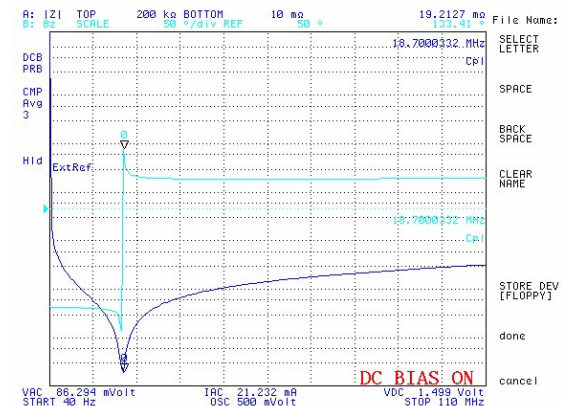


Figure 8: ESR measurement for a 0.250" x 0.250" large area capacitor.

In the equivalent circuit for a capacitor there is both a series resistance (R_s) and a parallel resistance (R_p). The higher the resistance value of R_p - the lower the electrical leakage of the capacitor. R_p was measured on all capacitors and the average results are within Table 2.

The loss tangent is defined as a ratio between the real and imaginary parts of a capacitor's

impedance. The loss tangent is a unit-less number that yields a relative measure of the dielectric material's electrical leakage at a given frequency. Loss Tangent was measured on all capacitors and the average results are contained within Table 2.

Capacitor Dimensions	ESR mOhms	Self-Resonant Frequency kHz	Rp Ohms	Loss Tangent
0.25" x 0.25"	8.3	18.15	1.46M	0.021
0.375" x 0.375"	17.3	12.92	631K	0.024
0.50" x 0.50"	15.3	9.08	374K	0.026

Table 2: ESR, Rp and Loss Tangent measurements for all capacitor sizes.

The typical percent capacitance change curve for an X7R dielectric material measured across the automotive temperature range has a maximum capacitance at approximately 0° C and approaches minimum values at the extremes of the temperature range. A representative X7R capacitance curve, available from a major ceramic capacitor supplier, is shown in Figure 9 for reference.

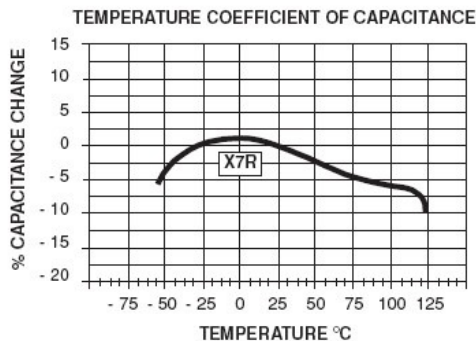


Figure 9: Typical capacitance change over temperature for an X7R dielectric. [1]

Figure 10 shows the measured capacitance from -50 °C to +150 °C. All capacitance readings were taken with a Hewlett Packard 4284A LCR Meter at 1.0 KHz and 1.0 volt AC RMS. The peak capacitance value occurs approximately at room temperature (25°C) for all three capacitor sizes then decreases approximately 10% at -50 °C and 20% at +125 °C.

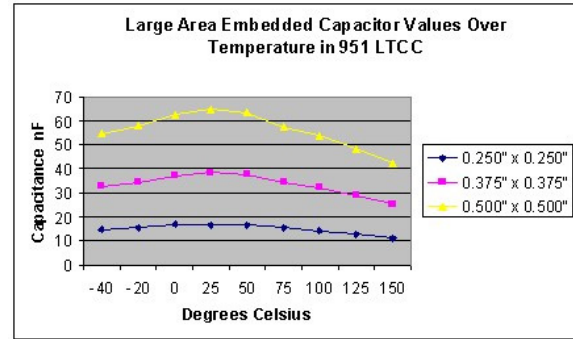


Figure 10: Capacitance measurements over the temperature range from -50 to +150 °C.

Capacitor Reliability Evaluation

All of the high-K dielectric embedded large-area single-layer capacitors were placed on thermal cycle reliability testing at -40/+125 °C (1-hour cycle).

The initial capacitance was measured using an Hewlett Packard 4284A LCR Meter at 1.0 volt AC RMS and 1.0 kHz. Measurements were repeated at 250 cycle endpoints up through and including 1000 cycles. Box-plots were generated at each endpoint showing the median value, the inner quartile and overall range of the data set for each capacitor size. Box-plots for all large-area single-layer capacitors LTCC material are shown in Figure 11.

A capacitor material annealing effect can be seen between the 0 and 250 cycle endpoints whereby the capacitance increases from 5-10% for all large-area single-layer capacitors.

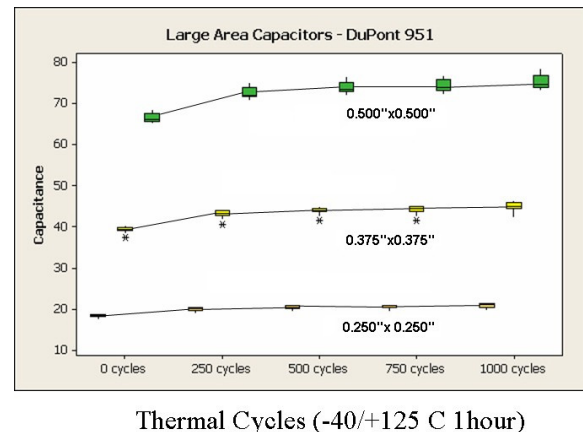


Figure 11: Thermal cycle reliability testing results for large-area embedded capacitors

Table 3 compares the overall reliability for all large-area single-layer capacitors before and after thermal cycle reliability testing. The average values for initial and 1000 thermal-cycle endpoint measurements for capacitance, dissipation factor (DF) and parallel resistance (Rp) were recorded.

Reliability test results (Table 3) indicates an overall capacitance shift of 10% or less after 1000 thermal cycles. Dissipation factors were nearly identical and Rp measurements were within 25%.

Capacitor Dimensions	Initial Capacitor Measurements			After 1000 Cycles -40/+125 C		
	Cap (nF)	DF	Rp	Cap (nF)	DF	Rp
0.25" x 0.25"	18.4	0.006	1.46M	0.021	0.007	1.11M
0.375" x 0.375"	39.5	0.007	631K	0.024	0.007	501K
0.50" x 0.50"	66.6	0.006	374K	0.026	0.007	293K

Table 3: Embedded capacitor reliability test results for all capacitor sizes.

Dielectric Voltage Breakdown Testing

The thickness of the high-K dielectric print was designed to be consistent for all capacitors independent of their size. The target dielectric thickness was a two-layer print approximately 38 - 40 microns thick. Voltage breakdown tests were conducted on all large-area capacitors fabricated within the DuPont 951 material set. The tests were conducted utilizing a Vitrek 944i Dielectric Analyzer. Results of these tests are included in Table 4.

Capacitor Dimensions	Average Breakdown Voltage (V)
0.25" x 0.25"	933
0.375" x 0.375"	818
0.50" x 0.50"	703

Table 4: Embedded capacitor dielectric breakdown test results.

LTCC Substrate Flatness Measurements

Substrate flatness is a critical requirement for all products that utilize surface mount components and flip-chip integrated circuits. Two sample substrates were submitted to the Delphi Metrology Lab for flatness measurements. Table 5 shows the worst case overall substrate camber for the 4" x 4" substrates. Camber,

measured with a three-point plane system, should not exceed 0.003" / inch or 0.012" overall. Both test samples met this requirement.

Substrate Flatness Test	Large Area Capacitor Test Board #1 Dimensions (worst case)
Overall Camber	0.0031"
Localized Flatness	+/- 0.001"

Table 5: Worst case LTCC substrate flatness measurements.

Localized flatness measurements, taken on the substrate surface directly over the embedded capacitors, were obtained using a Mitutoyo 3D CNC Vision Measuring System. The results are also shown in Table 5. Flatness measurements that exceed +/- 0.001" per in² would not be acceptable for placement of a flip-chip integrated circuit component. Both test samples also met this localized flatness requirement.

Summary & Conclusions

A LTCC test board was designed and fabricated to evaluate three different sizes of large-area embedded capacitors. The large-area capacitors were targeted for potential automotive under-hood electronic applications.

The large-area capacitor design consisted of a dual-print of DuPont's K1800 high-K dielectric paste for an area print as large as 0.250 in². The three capacitor sizes were designed for the high-K dielectric print to be placed in the middle of an eight layer LTCC substrate stack-up. By placing the capacitor dielectric near the center, surface irregularities due to the dual-layer dielectric print would be minimized.

The LTCC large-area embedded capacitor test board was fabricated using the DuPont 951 tape system. Initially, the embedded capacitors were tested for capacitance and dissipation factor then placed on reliability thermal cycle testing at -40/+125 °C (1-hour cycle) for 1000 cycles. All capacitors were retested electrically at 250 cycle intervals.

In addition to the reliability tests all the large-area embedded capacitors were evaluated for equivalent series resistance, parallel resistance and loss tangent. The embedded capacitors were also measured across their specified temperature range and compared to the typical capacitance temperature response of an X7R

dielectric, an industry standard. Dielectric voltage breakdown testing was completed - confirming a dielectric breakdown of greater than 700 volts.

Two types of topographical surface analyses were completed to evaluate the overall flatness of the substrate and also the flatness directly over the embedded capacitor. A three-point plane coordinate system measured the overall camber of the test substrates. The large-area capacitor test board easily met the Delphi general hybrid specification of ± 0.003 "/inch overall and the maximum local deviation measured directly over the embedded capacitor of ± 0.001 " per square inch.

Through the results of this limited, but highly focused project, DuPont's experimental high-K dielectric paste (E108936062, K=1500) was proven capable of meeting the capacitance and reliability requirements for automotive under-hood applications within an LTCC substrate. The capacitors met all the expected performance specifications by utilizing a two-layer print (~ 40 microns thick) to eliminate the affect of pin-holes. The double print effectively cut-in-half the initial capacitance target values, driving the potential need for further studies involving multilayer embedded large-area capacitors. DuPont continues to develop the high-K dielectric material, soon to be moved beyond the experimental laboratory stage to a production product - K1800.

Acknowledgements

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References

1. Vishay-Vitramon VJX7R Dielectric Data Sheet, Document Number 45008, Revision 30-Mar-05, available at www.vishay.com