

3D Integration Technologies for Miniaturized Tire Pressure Monitor System (TPMS)

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Abstract

3D integration of micro electromechanical systems (MEMS) together with integrated circuits (ICs) brings in several specific requirements. For instance, 3D integration of the different modules that make up a Tire Pressure Monitor System (TPMS) is a real technological challenge. A TPMS typically consists of a MEMS device, an application specific integrated circuit (ASIC), a power supply, a radio and an antenna. As part of the European project e-CUBES, a miniaturized TPMS demonstrator is being fabricated in which the MEMS, ASIC and radio devices are 3D integrated into a heterogeneous system. Au stud bump bonding (Au SBB), SnAg micro bumps and Cu/Sn solid liquid interdiffusion soldering (SLID) are used for electrical and mechanical interconnection between the individual layers. W filled through silicon vias (TSV) are applied through the transceiver chip whereas two different types of TSVs are demonstrated for the cap wafer of the MEMS device. The maturity of the applied technologies spans from brand new to well established, but combining these into a single 3D integrated device is nevertheless a significant logistical and technological challenge. As a follow-up to previous publications, this paper will focus mainly on the technological studies performed for the Au SBB, the SLID connections and the TSVs for the MEMS cap wafer. Visual, electrical and mechanical characterization will be presented, including reliability studies. Some results from the final miniaturized TPMS demonstrator will also be presented.

Introduction

Today's Tire Pressure Monitoring System (TPMS) fabricated by SensoNor Technologies AS [1] for Infineon Technologies [2] consists of a sensor block module and a radio block module mounted on a printed circuit board (PCB) and interconnected by wire bonds. For future applications it is highly desirable to miniaturize the TPMS, which is best done by tightly integrating the sensor and radio block modules using 3D integration technology. The sensor block consists of the sensor and its microcontroller ASIC (μ C) whereas a transceiver ASIC (TX), a bulk acoustic resonator (BAR) and an antenna constitute the radio block. Within the e-CUBES project [3] a demonstrator was fabricated in which those components, except the antenna, were 3D integrated using different interconnection and through-silicon via (TSV) technologies (Fig. 1). In a first version of the demonstrator (Fig. 2) the TX was stacked on top of the μ C using μ -bumps whereas in a second version solid-liquid interdiffusion (SLID) using Sn and Cu [4] is used. The sensor and the BAR are stacked next to each other on top of the TX/ μ C stack using Au stud bump bonding (Au SBB). W-filled TSVs (also referred to as ICVs) [4] lead electrical signals through the TX, whereas TSVs in the sensor cap wafer are achieved with silicon pins through the glass substrate, which is a technology patented by Plan Optik AG [5]. As an alternative solution for realizing TSVs in the

sensor cap wafer, hollow vias were tested in parallel. The 3D integrated sensor stack is mounted in a moulded interconnect device (MID) which protects the sensitive subcomponents. The antenna is integrated in the MID and an opening is provided for the pressure inlet. Following up on previous publications [6-13], this paper focuses on the experimental results of the Au SBB used for stacking the sensor and BAR onto the TX, the hollow TSV technology proposed as an alternative for the sensor cap wafer, and the SLID technology proposed for stacking the TX onto the μ C.

Experimental

Hollow through-silicon vias

An alternative solution to the silicon TSVs in glass as offered by Plan Optik AG are hollow vias in a silicon substrate with thermal oxide as insulation and highly doped poly silicon as a conductive layer. In order to demonstrate this alternative solution, dummy sensor cap chips with hollow vias were fabricated and bonded onto dummy TX wafers using Au SBB. The hollow vias were made on 150 mm diameter silicon wafers. A 2.5 μ m thick thermal oxide was grown and 50 x 50 μ m² holes were defined in the oxide by reactive ion etching (RIE). Deep reactive ion etching (DRIE) was then used to etch vertical holes through the 300 μ m thick silicon

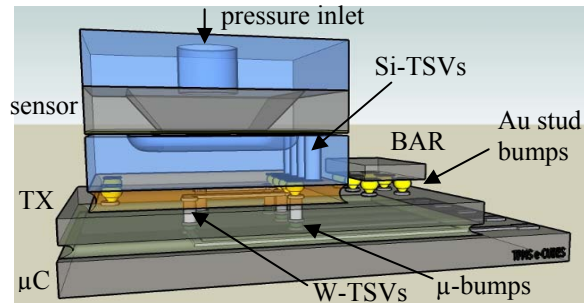


Fig. 1: Illustration of the 3D integrated miniaturized tire pressure monitor system.

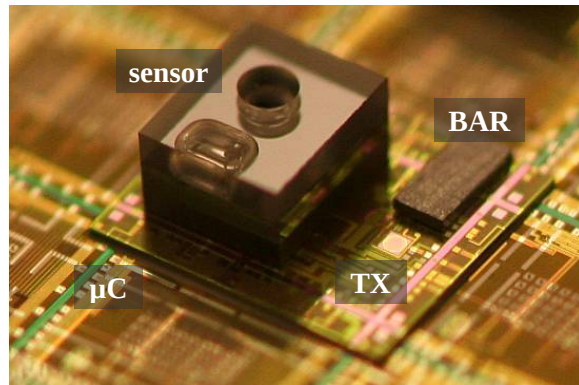


Fig. 2: Image of the miniaturized TPMS demonstrator before final dicing.

wafer, using a modified Bosch process [14] on an Alcatel AMS 200 I-productivity etching tool. The average etch rate was 16 $\mu\text{m}/\text{min}$. Following DRIE, the oxide was stripped and a new 1 μm thermal oxide was grown in order to electrically isolate the vias from the substrate material. A 1 μm poly silicon layer was then deposited by low pressure chemical vapour deposition and doped using phosphorous gas phase doping. In order to form a good electrical contact to the poly silicon, a 1.2 μm thick aluminium layer was sputtered on both sides of the wafer. At this stage of the processing the wafers are perforated with 50 x 50 μm^2 holes which make it impossible to use conventional spin-on resist for further patterning of the different layers. Instead, the 10 μm thin Dupont MX-5010 dry-film resist was laminated onto both sides of the wafer. Following exposure, the resist is patterned using spray development. The laminated resist easily covers the perforations in the wafer, thereby protecting the hollow vias from the subsequent etching steps. RIE was used to pattern the aluminium as well as the underlying poly silicon layer. At this stage the TSVs created through the dummy cap wafers were tested electrically. The wafers received Au stud bumps before being diced and sent for flip-chip bonding (Fig. 3 and Fig. 4).

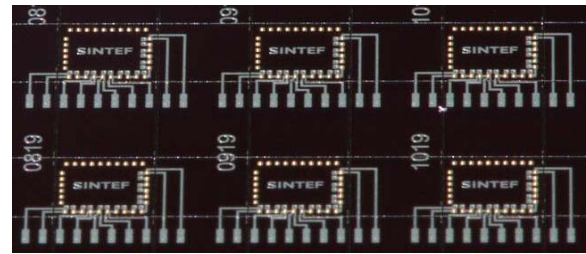


Fig. 3 : Cap wafer with hollow TSVs after Au stud bump bonding and dicing.

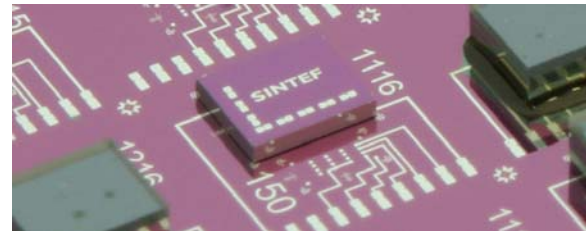


Fig. 4 : Die with hollow TSVs bonded to a TX substrate wafer.

Au stud bump bonding

After comparing various interconnect technologies, Au SBB was found to be ideally suited for 3D stacking of a micro-electromechanical system (MEMS) on top of an ASIC component. One of the main advantages of using Au SBB is the fact that there is no need for any wet processing that otherwise could be problematic for a MEMS device. Furthermore, there is no need to deposit an under bump metallization layer as would normally be needed for conventional solder bumping. Whereas solder bumps normally need a reflow step at temperatures higher than 200 $^{\circ}\text{C}$, for Au SBB lower process temperatures can be used, especially when using thermosonic bonding. Since stud bumping is a serial process, it is most cost-effective for interconnecting devices with low I/O counts like most MEMS. For the TPMS demonstrator, a MEMS sensor and MEMS BAR device needed to be bonded on top of a 60 μm thin TX chip that had previously been bonded to a μC wafer using μ -bumps and underfiller. This was definitely a technological challenge. The MEMS devices needed to withstand the temperature, force and energies that are used during the stud bumping, and all devices had to withstand the bonding process itself. Prior to fabricating the actual demonstrator, several trial runs with dummy devices were done in order to optimize the Au SBB process for this particular application.

During back side thinning of the TX substrate wafers, a temporary handle wafer was

attached to the front side of the TX using a wax. After thinning, any wax residues were removed using an O_2/H_2O plasma strip. Bonding results were compared for substrates that had undergone this O_2/H_2O plasma strip and substrates that had not. As it was feared that the 60 μm thin TX chips bonded onto the μC wafer would be too fragile to withstand the force used during stud bumping, it was decided to place the Au stud bumps onto the sensor and BAR devices. Kulicke&Soffa [15] did the stud bumping on the 150 mm sensor and BAR wafers using their so-called Accubump process. The bumps on the BAR devices had an average diameter of 47 μm and a height of 32 μm . On the sensors the bumps had a diameter of 53 μm and a height of 30 μm . Following the stud bumping, the sensor and BAR wafers were diced and sent to Datacon [16] for chip-to-wafer bonding. Both thermocompression bonding (TCB) and thermosonic bonding (TSB) were tried. TSB allows the use of lower temperatures and shorter bonding time, but the ultrasonic energy that is used could be detrimental for fragile devices. The tool that is holding the chip to be bonded was at 200 $^{\circ}C$ for TCB and at room temperature for TSB, while the chuck temperature was 120-140 $^{\circ}C$ in both cases. For TCB a bond force of 20-30 N was applied for 10 seconds, while for TSB the tool force was 12-20 N for 2 seconds. To improve the adhesion of the sensor to the TX, Epo-Tek 353ND no-flow underfiller was used. This is a non-conductive epoxy adhesive that was dispensed onto the TX substrate right before the flip-chip process. One of the main advantages of the Epo-Tek underfiller is its large range of operation temperatures. It can be used continuously at operating temperatures between -55 $^{\circ}C$ and 250 $^{\circ}C$ and allows brief exposure at up to 350 $^{\circ}C$. This makes it ideally suited for use in devices like the TPMS which need to comply with very strict reliability demands. Following the bonding of the sensor, the BAR devices were bonded. However, in order to avoid interference with the operation of the BAR, no underfiller was used in that case.

Solid-liquid interdiffusion

Dummy 150 mm wafers with test patterns and realistic routing, but without TSVs, actual MEMS structure or active functions, were fabricated to test SLID bonding with Cu and Sn. The surfaces of the wafers were meant to represent typical wafer surfaces. A 1.2 μm pure aluminium metallization on a thick thermal oxide was selected for these tests. A 500 nm thick PECVD oxide layer was added in order to assure protection of the Al layer during plating. A plating base of TiW (200 nm) and Cu (300 nm) was sputtered. The regions to be plated were defined by

photolithography using a positive resist (AZ4562). A 5 μm thick Cu layer was plated on three “bottom wafers” whereas 5 μm Cu and 3 μm Sn was plated on three “upper wafers” (Fig. 5). The resist was stripped and the plating base removed outside the regions of plated material by differential etching. The upper wafer was diced and the chips mounted on a temporary handle wafer using wax. The handle wafer with the chips was optically aligned and bonded to the bottom wafer using a bonder from EVG. A bonding temperature of 325 $^{\circ}C$ and a tool pressure of about 3 kN were applied. Plating and dicing were performed by Fraunhofer IZM in Berlin [17], whereas the bonding was done at the Munich division of Fraunhofer IZM. The assembly of dies onto a handling wafer was done by Datacon. The area of the Al pads on the contact points was $60 \times 60 \mu m^2$ whereas the contact openings in the PECVD oxide were $10 \times 10 \mu m^2$. Circular SLID bumps were plated on every contact point, with a diameter of 50 μm on the bottom wafer and 40 μm on the upper wafer.

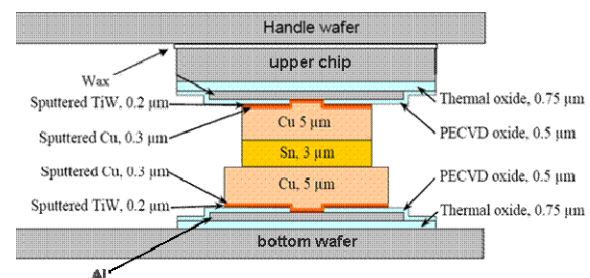


Fig. 5 : Cross section illustrating the SLID bumps during bonding. The chips from the “upper” wafer were mounted on a handle wafer for bonding onto the “bottom” wafer.

Layout considerations and design rules

One of the main challenges of 3D integration is to get the layout of the different components to match in such a way that they can be interconnected flawlessly. Each technology that is being applied has its own set of design rules, and combining different technologies can be a real logistical challenge since at this time there are no standard design tools available for 3D integration.

The hollow via technology can be applied to silicon substrates with thicknesses of up to 1 mm, although there is a trade-off to be made between substrate thickness, minimum pitch, via resistance and cost. Larger via holes etch faster and have a lower resistance, but this comes at the expense of a larger via pitch. The via size and shape need therefore to be optimized for a particular application. Hollow

vias with $50 \times 50 \mu\text{m}^2$ via holes allow a minimum TSV pitch of $140 \mu\text{m}$, corresponding to a via density of approximately 5 thousand vias/ cm^2 . However, the technology is believed to be scalable down to a pitch of about $60 \mu\text{m}$ for $300 \mu\text{m}$ thick silicon substrates, which corresponds to about 27 thousand vias/ cm^2 .

In order for the Au SBB to be successful, it is important that the stud bumps are distributed in a symmetric fashion over the die, such that each bump experiences the same pressure during bonding. For the TMPS demonstrator, this was achieved by adding a number of dummy stud bumps on the sensor devices. No dummy stud bumps needed to be added on the BAR devices since it has bondpads that were distributed symmetrically over its surface. The minimum pitch for Au SBB is currently set at $90 \mu\text{m}$, corresponding to a density of approximately 12 thousand bumps/ cm^2 , but it is estimated that in the future the minimum pitch could be reduced to about $50 \mu\text{m}$ or 40 thousand bumps/ cm^2 .

The electrical and mechanical interconnects are performed in one process step during the stack formation when using SLID. The layout of the SLID pads, for the electrical as well as for the mechanical contact points, has to consider the topography of the devices that are to be connected. For the SLID version of the TMPS demonstrator, Cu-plating will be applied on the backside of the TX ASIC, which has previously been thinned for uncovering the tungsten TSVs. Only a redistribution layer consisting of $0.8 \mu\text{m}$ thick AlSiCu and the via-opening into the backside isolation oxide ($1.0 \mu\text{m}$ thick) contribute to the topography on this surface. Electrical constraints like e.g. no metal pads beneath the coil region of the TX were more challenging than the modest surface topography. On the other hand, the topography was more of a concern for the placement of the SLID pads on the μC ASIC. Al tips at the measurement pads and special structures at the corners of the scribe lines had to be taken into account. It was avoided to place SLID pads in these regions. The pads for the Au SBB of the sensor and BAR as well as the pads for the wire-bonds to the PCB had to be mechanically supported by adding underlying dummy SLID pads. Most of the area of the SLID pads for electrical contact was placed on top of the $0.8 \mu\text{m}$ thick AlSiCu redistribution layer. Due to a relatively low density of the electrical interconnects, coarse dimensions for width ($> 60 \mu\text{m}$) and spacing ($> 30 \mu\text{m}$) of the SLID pads could be chosen, thereby enhancing the solder region and achieving a robust design with respect to possible misalignment. Alignment marks on the bottom side of the TX wafers are used for a precise assembly of the dies onto the handle wafer. For the

SLID bonding of the handle wafer with TX dies to the μC wafer, an additional alignment mark was implemented into both SLID layers. Empty regions were filled with additional dummy structures, thereby reaching an overall area allocation of about 30 %, which improves the thickness uniformity of the through-mask electroplated Cu and Sn-layers. The final layout is shown in Fig. 6. Although the standard size for SLID pads is $30 \times 30 \mu\text{m}^2$ with a minimum pitch of $60 \mu\text{m}$, the pads can be scaled down to about $5 \times 5 \mu\text{m}^2$ and $10 \mu\text{m}$ pitch, corresponding to a density of 1 million interconnects / cm^2 .

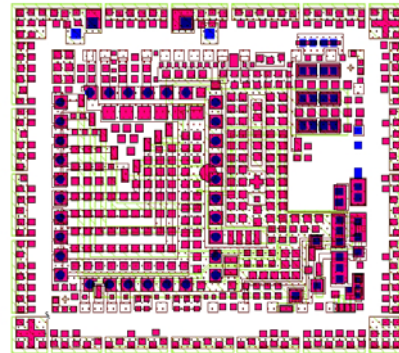


Fig. 6 : Layout of the SLID version of the TPMS demonstrator : SLID layers (red), Au SBB and wire bond pads (dark blue), redistribution layers of the TX (green) and μC (dotted).

Test set-up

Cross-sections of the stud bumps and SLID interconnections were obtained by embedding samples into an epoxy resin. The samples were grinded and polished to obtain precise cross sections for studies in a NEOPHOT 32 light microscope. Scanning electron microscopy (SEM) was performed in a FEI Quanta 600 FEG, with an integrated energy dispersive spectrometry (EDS) system for element analysis.

Destructive die shear tests were performed on bonded devices, as a simple and fast method to check the bump integrity. Shear tests were performed using a DAGE 2400A shear tester with a D10 kg die shear load cartridge. The shear height was $20 \mu\text{m}$ and the shear speed $200 \mu\text{m/s}$. Shear strengths are specified in MPa and calculated by dividing the applied force by the bonded area.

The electrical performance of interconnects was tested using daisy chain structures with either stud bumps only, stud bumps combined with hollow TSVs, or SLID interconnects. Mostly, manual 4-wire resistance measurements were done. However, the

wafers with hollow TSVs were subjected to a full wafer test on a TSK A-PM-90A automatic probe station.

Thermal cycling (TC) stress tests were performed in order to investigate the effect of thermally induced stress on the reliability of the interconnects. TC was performed between $-40\text{ }^{\circ}\text{C}$ and $+150\text{ }^{\circ}\text{C}$ in a Heraeus HT 7012 S2 thermal cycling chamber. A total of 1000 thermal cycles were executed, with 8 thermal cycles per hour, 50 % duty cycle and load transfer time less than 15 seconds between temperature extremes. Bonded units were also tested to see if they could withstand post processing like lead free soldering with process temperatures of up to $260\text{ }^{\circ}\text{C}$ and exposure times around 10 seconds. Therefore, high temperature post processing (HTP) stress tests were done, during which the units were stored for 30 minutes at $260\text{ }^{\circ}\text{C}$. This relatively long time exposure at elevated temperature is a severe test condition. For samples bonded with Au SBB, electrical resistance measurements and die shear tests were done after bonding, after TC and after HTP stress. A somewhat reduced test program was run for the SLID samples.

As an additional non-destructive inspection method for the bonded MEMS devices, X-ray imaging was done by Fraunhofer IZM in Berlin. For some devices, the X-ray results were verified by subsequent shear testing.

Results and Discussion

Hollow through-silicon vias

The hollow TSVs were tested electrically prior to Au SBB and dicing. A full wafer test (550 dies) of daisy chains with 2 and 16 hollow vias was done. On the wafer that was sent for Au SBB, the average resistance of the daisy chain with 2 vias was $15.0\text{ }\Omega$ with a standard deviation of $0.7\text{ }\Omega$. For the daisy chain with 16 vias the resistance was $119.4\text{ }\Omega$ with a standard deviation of $4.6\text{ }\Omega$. This means that the resistance of one TSV was approximately $7.5\text{ }\Omega$. The yield of the daisy chain with 16 bumps was 90 %, but all failing dice were located along the wafer edge. This is where the DRIE process exhibits a lower etch rate which resulted in vias that were not etched completely through. All other dies were good.

Au stud bump bonding

Cross-sections of bonded devices revealed bump heights varying from 8 to $21\text{ }\mu\text{m}$, depending on the bonding parameters that had been used. For all

devices, an Au-Al intermetallic region is seen on the sensor side of the bumps (Fig. 7), as confirmed by EDS analysis. It is believed that this intermetallic region was formed already during the stud bumping of the sensors. Similar intermetallic regions are formed at the TX substrate side of the bumps, but only for those bumps that have been squeezed to a height of less than approximately $15\text{ }\mu\text{m}$. Although only a limited number of cross-sections were made, it seems that those bumps also tend to have a lower electrical resistance. In order to obtain a good bonding result it seems therefore important to apply a high enough bond force and enough energy. Though not noticeable in electrical tests, some of the cross-sections show the presence of a thin layer in between the TX substrate metallization and the stud bump. EDS analysis of this layer shows a high concentration of both carbon and oxygen, which probably means that this is a thin residual layer of underfiller. Cross-sections of bonded devices after TC and HTP test did not reveal any visible differences compared to the cross-sections made directly after bonding.

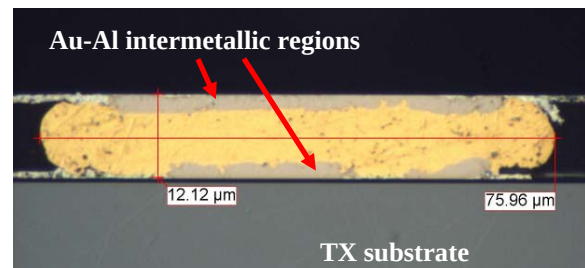


Fig. 7 : Cross section of Au stud bumps after bonding (sensor die on top, TX substrate below).

Resistance values for daisy chains that have 16 Au stud bumps connected in series are shown in Fig. 8. Based on the layout of the test structure and the metal thickness, it is estimated that the metal connections in between the bumps contribute with about $0.6\text{ }\Omega$ in total. The rest of the measured resistance can be attributed to the bumps themselves. Resistance values were measured directly after bonding, after TC stress and after TC plus HTP stress. Only devices that had a resistance below $5\text{ }\Omega$ after bonding were subjected to TC test, and only devices that still showed a resistance below $5\text{ }\Omega$ after TC were sent for an additional HTP test. As can be seen from Fig. 8, the measured resistance values after bonding show significantly less variation for the substrate that had been subjected to the $\text{O}_2/\text{H}_2\text{O}$ plasma strip. For those devices the average resistance value was $0.10\text{ }\Omega$ per bump. Whereas thermal cycling increased the variation somewhat for that wafer, a tremendous increase in resistance is seen for the wafer that had not received the $\text{O}_2/\text{H}_2\text{O}$ plasma strip.

This clearly showed that the plasma strip significantly improved the quality of the Au SBB. Even after an additional HTP test, the substrates that had seen the plasma strip still show low resistance values, which indicates an excellent reliability.

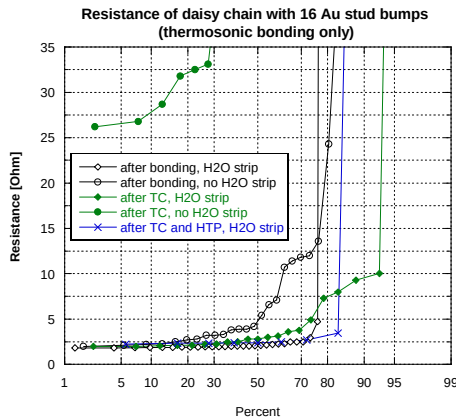


Fig. 8 : Resistance of daisy chains with 16 Au stud bumps. Results of different process splits are shown.

In Fig. 9, the resistance values are shown for daisy chains that have a series of 16 Au stud bumps each combined with a hollow TSV through a dummy capping die. A comparison is made between devices that were bonded using thermosonic bonding (TSB) and devices bonded by thermocompression (TCB). The substrate wafers used for these tests had undergone an O_2/H_2O plasma strip. The measured resistance after bonding is around 124.5 Ω , which corresponds to 7.8 Ω for a single via combined with a bump. However, for some devices bonded by TSB the measured resistance values are closer to 110 Ω ,

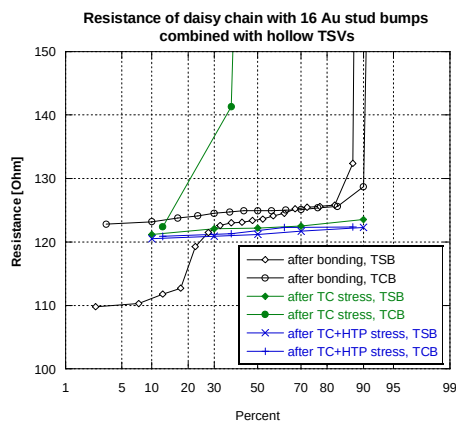


Fig. 9 : Resistance of daisy chains with 16 Au stud bumps combined with hollow TSVs. Results of TSB and TCB bonded devices, after bonding, after TC stress and after TC + HTP stress.

which is lower than what had been measured for the vias only. Inspection of these dies revealed that the metal on top of the bonded dies had been scratched during TSB, thereby causing a short-circuit between two TSVs, which explains the lower resistance. The vacuum that was holding the die was not strong enough to keep the die perfectly in place during the ultrasonic bonding, which caused the surface to become scratched. Fabricating a dedicated tool for handling these particular dies could have solved this issue. TSB bonded devices with resistance values indicating that no shorts were present were thermally stressed and showed good results after TC. On the other hand, 3 out of 4 stressed TCB bonded devices appeared to have reduced conductivity after TC. However, after an additional HTP test on the same devices, good results were achieved for all devices independent of bonding method.

Prior to bonding, the bumps placed on the sensor devices had a shear strength of 102 MPa, whereas the bumps on the BAR devices had a shear strength of 113 MPa. After optimizing the bonding process such that the right amount of underfiller was applied, shear strengths of more than 50 MPa were obtained for sensor devices bonded with the Epo-Tek underfiller surrounding the bumps. Fracture occurred within the dies, thereby confirming a very strong bond when underfiller is present. BAR devices bonded without underfiller typically showed a shear strength of 27 MPa. Fracture occurred either through the bump or at the interface between the bump and the Al pad on the TX side. Shear strengths for both sensor and BAR remained excellent after TC and HTP stress, and no changes in fracture mechanisms were observed. In some cases the shear strength even increased somewhat after TC.

X-ray inspection of complete 3D integrated stacks helped to verify the alignment of bonded chips and the quality of the Au SBB. A good alignment in X/Y direction was known to be critical, but also the parallelism of the bonding planes was later recognized as highly important. The planarity of the tool pressing the sensor and the BAR down during flip-chip bonding onto the underlying TX chips was critical. If the tool itself was not perfectly flat or if it came down in a skew manner, the bumps would be squeezed too much on one side and not enough on the other side. On the weakly bonded side, bad electrical interconnects might occur. On the other hand, typical failures related to “over-bonding” are short-circuits between adjacent bumps or damage to the chip or substrate structures close to the contact points due to high forces. The shape of the bumps seen from the X-ray images allowed to verify if the devices had been

bonded in a satisfactory parallel fashion, which was also correlated to electrical results of the 3D stacks. In Fig. 10 a comparison is shown between a BAR device that was functional after bonding and one that was not functional after bonding.

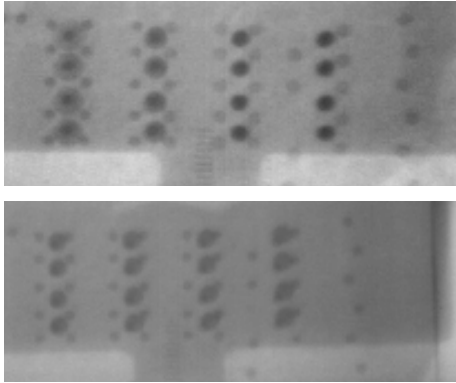


Fig. 10: X-ray images of a functional (lower) and non-functional (upper) BAR device after bonding. The sizes and shapes of the bumps are more equal for the well bonded BAR device (lower).

Solid-liquid interdiffusion

A row of 12 virgin SLID bonded Cu-Sn-Cu bumps was studied optically before TC and another row of equally many bumps after TC (Fig. 11). Two out of the 12 studied bumps had a light grey phase on the side of the central Sn layer. The Sn layer seemed to have undergone strong deformation and material had been squeezed to the sides. Small copper coloured structures were distinguishable in the central layer. EDS analysis showed the presence of the original copper layers, whereas all the original tin had reacted with copper to form mostly the targeted ϵ -phase (Cu_3Sn). The light grey regions that were seen in some cases were identified as some residual η' -phase (Cu_6Sn_5). Note that the ϵ -phase is the most Cu rich and therefore the most stable and preferred phase. It is thermodynamically stable and has a melting point higher than 600 °C. The small copper coloured structures in the central layer were too small for analysis by EDS, but they can be assumed to consist of copper. The thin initial TiW-layer at both sides of the bump was clearly visible in white on the SEM-image (Fig. 11, lower) and it seemed to be intact. Although not shown here, in some cases voids were observed inside the regions of the ϵ -phase. After TC there seemed to be slightly larger regions of the η' -phase, but the difference was not significant. The small copper coloured grains in the central layer were not seen anymore after TC. Samples studied after high temperature storage did not show notable differences to the thermally cycled sample, but the

η' -phase was not observed on these units which could indicate that un-reacted η' -phase regions had reacted with the surrounding copper during annealing. With little or no η' -phase regions left, one can expect the SLID interconnects to be highly reliable.

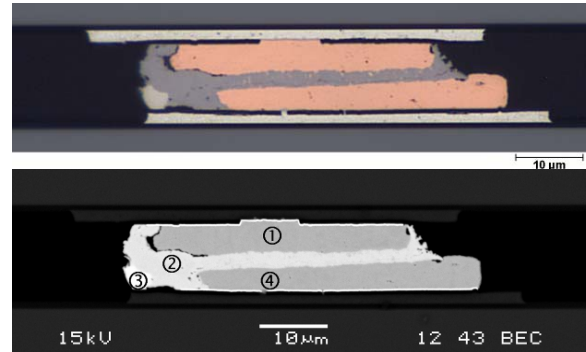


Fig. 11 : Light microscope (upper) and SEM image (lower) of a bonded sample. EDS identified the different regions as : copper (1 and 4), tin-copper phase ϵ (2) and tin-copper phase η' (3).

Shear tests performed on 10 bonded samples before and after TC supported the theory that no significant change took place in the microstructure of the SLID bumps during TC. Only a minor change in shear strength was seen, from 37 ± 11 MPa before TC to 36 ± 5 MPa after TC, thereby confirming the excellent reliability of the SLID interconnects. Three main fracture mechanisms were identified for virgin samples. The strongest samples had several bumps that had fractured horizontally along the PECVD oxide layer under the plating base layer on the bottom wafer side. The medium strong samples typically had bumps with a fracture going vertically or diagonally through the bump. For the weakest samples several bumps were found to have fractured horizontally along the PECVD oxide layer under the plating base on the upper chip side.

A daisy chain of 100 bumps was measured before TC for 13 samples showing a resistance of $5.7 \pm 1.1 \Omega$. The resistance of a daisy chain with only two bumps showed $2.7 \pm 1.1 \Omega$ when measured on 15 samples. This indicates that the resistance of the aluminium conductors dominated the resistance values when the bonding was good. No electrical measurements were made after TC, but no changes were expected from the cross sections and shear tests.

Demonstrator results

The first version of the demonstrator used μ -bumps between the TX and the μ C. After the full 3D

stack was completed, it was mounted on a micro-PCB that fitted into a MID with integrated loop-antenna and two batteries (Fig. 12). The total volume of the miniaturized TPMS was just below 1 cm³.

Electrical tests that were done on the PCB confirmed that the communication between the different devices was functional. The μ C could be programmed and the BAR operates at the correct frequency. These results prove that the integration of the different interconnect technologies was successful. Testing of the sensor functionality itself is still ongoing and a second version of the demonstrator in which the μ -bumps are replaced by SLID interconnects is also under development.

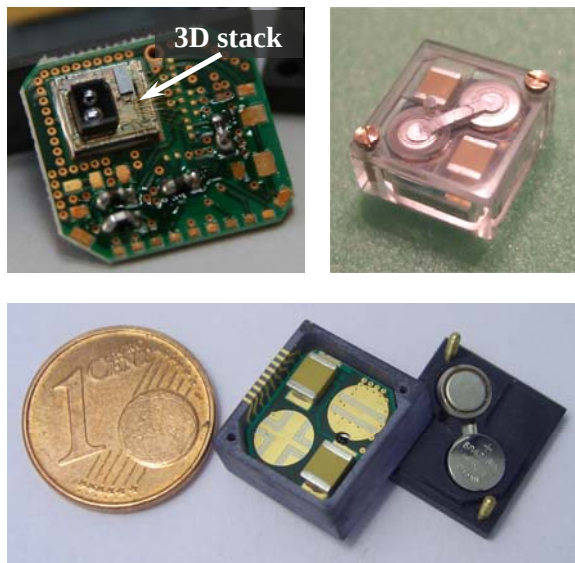


Fig. 12: Micro-PCB with 3D stack (upper, left), transparent demo version of the completed TPMS demonstrator (upper, right), MID with PCB, integrated antenna and batteries (lower).

Conclusion

Different 3D integration technologies suitable for stacking of MEMS and ASICs were developed and experimentally tested. Their feasibility and reliability was demonstrated through visual, electrical and mechanical tests. Some of the presented technologies were used for the fabrication of a miniaturized TPMS demonstrator.

Acknowledgements

This report is based on a project which is supported by the European Commission under support-no. IST-026461. The authors would like to thank the colleagues of the e-CUBES project as well as G.

Hillmann (Datacon), R. Johannessen, J. M. Graff and L. G. Tvedt (SINTEF), V. McTaggart (K&S), T. Baumgartner (Fraunhofer IZM), W. Liebsch (Dupont).

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