

Side Mount Package (SMP) for Ultra-High Density Memory Applications

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Abstract

In recent years, package stacking technology has been pursued and practiced widely in industry, mainly as perimeter array package on package (PoP) stacking configuration. However, the stacking quantity is limited to just two. For ultra high density die stacking application such as solid state drive (SSD), there can be as many as 64 dice assembled in limited space. For this type of application, multi-package stacking can provide practical lower cost solution compared to die level memory stacking by Through Silicon Via (TSV) technology. However, multi-package stacking technology has not yet been demonstrated in High Volume Manufacturing. Therefore, new low cost highly reliable and easily manufacturable multi-package stacking concept is necessary for ultra high memory density packaging solution. In this paper, we developed side mount package (SMP) cube, which is shown to use smaller board space than any of other package stacking technology. Small board space for eight or more multi-stack packages is due mainly because SMP doesn't need redistribution layer formation process for side wall interconnection or through mold via (TMV) formation and solder filling process, and solder joints between individual packages.

Key processes for SMP are; (a) Quad-Flat-No-Lead (QFN) single package build by typical die stacking technology with wire bonding and die attach film (DAF). Key feature in this step is the exposed lead pad on side wall of the QFN package. (b) QFN package stack by polymeric adhesive layer with thickness of 20~50 um, (c) the eight QFN package stack up by adhesive layer and the exposed pad is aligned on one area of the package stack up. This array of the exposed pad from each QFN pad is naturally redistributed pad to the sidewall. (d) Final step is solder ball attach process on the exposed pad array for board level interconnection. We demonstrated ultra-high density package stacking solution by novel package interconnect structure, side mount package and the board level interconnection by solder arrays on the sidewall of the package cube.

Key words: High Density Memory, Die Attach Film (DAF), Multi-Cube Package (MCP), Side Mount Package (SMP), Quad-Flat-No-Lead (QFN), Solid State Drive (SSD)

Introduction

Highly integrated three dimensional (3-D) packaging systems have become primary assembly solution for electronic device/component assembly solution to meet ever increasing requirements pursuing small form factors, better functionality, high interconnect density and cost effective assembly. Especially solid state drive (SSD) application as killer application of flash memory market requires ultra high density memory capacity within small space and therefore robust 3-D packaging solution for higher number of memory die to be interconnected is necessary.

There are usually three different 3-D packaging technologies; bare die stack, package stack and module stack [1]. Bare die stack is the most compact 3-D stacking technology in terms of stacking density and electrical performance. However, the package design complexity and high manufacturing cost for advanced bare die stacking is blocking its wide application. On the other hand, 3-D packaging assembly by module stacking is relatively cheap and convenient because conventional module manufacturing is adopted and only solder joint is necessary between the modules. However module stacking is not desirable for the system where the ultra high density memory is to be assembled in limited space. Package stacking is the best 3-D

packaging technology in terms of moderate manufacturing cost and achievable high memory density. Although there is still technical challenges for package stacking together with die level stacking in individual package such as package stacking density, interconnect design and material, package stacking yield and reliability, package stacking technology has been practiced widely in industry mainly for perimeter array package on package (PoP) stacking configuration as shown in Fig. 1.

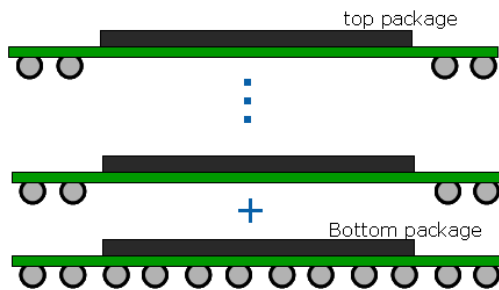


Fig. 1 Most common package stacking configuration

For SSD application, there are more than 50 dies assembled in limited space, and package stacking is the right solution practically because die level memory stack by bare die stack with sidewall interconnects [2~4] and TSV (Through Silicon Via) [5~6] technology are still in high manufacturing complexity and cost. Even package stacking technology is rare available for low cost and highly reliable stacking configuration although several package stacking approaches were tried for high density memory module [7~8].

Therefore, it is highly necessary to develop low cost, ultra-high density and most simple 3-D package stacking technology. In this paper, we will describe new design and process steps for 3-D package stacking and side mountable package configuration especially for ultra high density memory application.

Fabrication Process

We developed Multi-Cube Package (MCP) to provide low cost, ultra high memory density packaging solution for solid state drive application. Individual package is typical quad-flat-no-lead (QFN) package. QFN is one of main stream package for low-to-medium I/O count due to its simple structure, low cost and high electrical/thermal performance [9]. We selected QFN package as building block for MCP demonstration because it provides inherent side pad

opening for electrical side wall interconnect, suitable for high die stacking by die attach film and wire bonding inside the package and easy manufacturing with existing HVM technology.

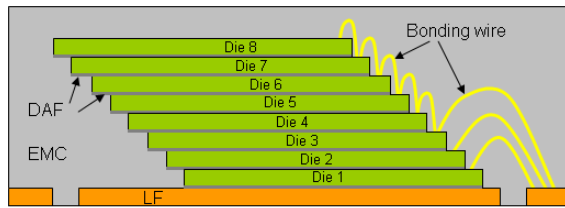
Fig. 2 shows the process steps for MCP. (a) 8 die stacking by staggered configuration on QFN package, (b) QFN package stacking by adhesive layer, (c) QFN cube stack up to 8 packages using adhesive layer and (d) solder ball attach and reflow on exposed LF pad. Detail process description is as follows.

QFN Building Block Fabrication

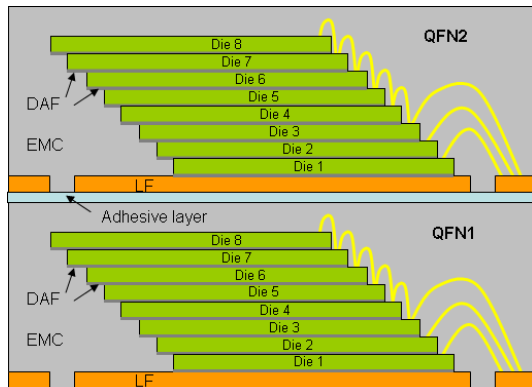
First, individual QFN package was fabricated as building block for SMP in this paper. Fig. 2(a) shows QFN single package configuration by typical die stacking technology with wire bonding and die attach film material on QFN lead-frame. Key feature here is the exposed lead pad on side wall of the QFN package, in which 8 dies are stacked in staggered form and all wire connection are made to one side of QFN pads. Individual die thickness was 75 μm by polish treatment and die attach film (DAF) was 20 μm thick. Die attach process was done by wafer level die attach film material lamination, wafer sawing process, die pick up and placement on leadframe die pad and on top of pre-attached die. Each DAF layer is fully cured for 1 hour at 120 $^{\circ}\text{C}$ in convection oven before wire bonding process on the same die's I/O pad. QFN leadframe substrate was Cu based leadframe material with Matt Sn coating. NiPdAu finished Cu based leadframe can be used. Environmentally green molding compound material with 55 μm max filler cut and CTE matched with Cu leadframe for low QFN warpage was used for transfer molding process. After package singulation, QFN building block fabrication is finished.

QFN Package Stacking Process

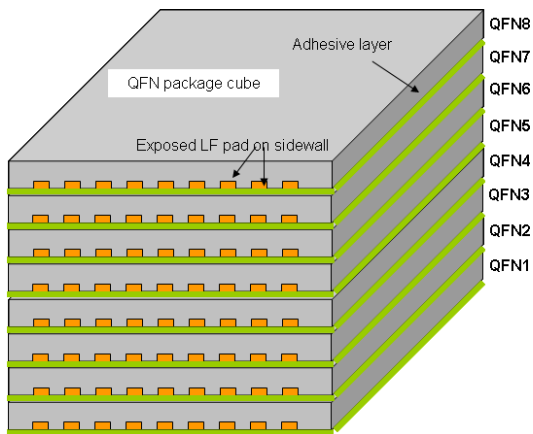
Next process is QFN package stacking by adhesive layer (two package stack in this figure as in Fig 2(b)) and the adhesive layer thickness is 20 μm thickness and its formulation is same as DAF layer used in die stacking. The adhesive layer was transferred to the backside of QFN building block manually, but the adhesive layer film can be laminated into back side of QFN package strip before QFN singulation. After QFN package strip singulation with pre-attached adhesive layer film, QFN package stacking can be automated by conventional pick and place machine. The adhesive layer is also fully cured by convection oven for 1 hour at 120 $^{\circ}\text{C}$. Fig. 2(c) shows the eight QFN package stack up by the adhesive layer and the



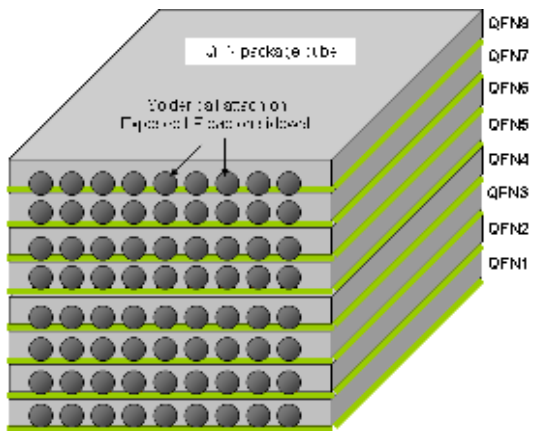
(a)



(b)



(c)



(d)

Fig. 2 SMP process flow; (a) 8 die stacking by staggered configuration on QFN package, (b) QFN package stacking by adhesive layer, (c) QFN cube stack up to 8 packages using adhesive layer and (d) solder ball attach and reflow on exposed LF pad.

exposed pad is aligned on one area of the package stack up. This array of the exposed pad from each QFN pad is naturally redistributed pad to the sidewall.

Solder Ball Attachment

Finally the solder balls are attached on the exposed pad array for board level interconnection as shown in Fig. 2(d). The exposed pads from individual QFN package are already covered by solder wettable surface such as Sn or Au. The additional UBM formation on exposed pad after passivation layer formation is an option depending on the reliability requirement. 300 μm diameter Sn1.0Ag0.5Cu solder ball is attached with flux dipped and reflowed by lead-free solder reflow condition with peak temperature of 260 $^{\circ}\text{C}$ under N_2 condition.

Board Level Interconnect by SMT process

After solder ball mount on the side wall of SMP, it is compatible with customer standard SMT process for board level interconnect. Fig.3 shows schematics of the board level interconnection by solder arrays on the sidewall of the package cube and actual SMP prototype. Fig.4 shows the final multi cube packages on board for 8 x 8 cube arrays for SSD memory board assembly.

This is an example of SSD memory density calculation in package cube dimension. Each QFN package has 8 die stacks up for 8 G bytes (1 G bytes per 1 die) in 8 mm x 8 mm x 1 mm. The package cube stack up is made of 8 package stack and 7 adhesive layers in 20 μm thickness per layer bringing to total 8.14 mm thickness. Final package cube dimension is 8 mm x 8 mm x 8.14 mm and 64 G bytes equivalent to 8 GB. In SSD board assembly with SMP of 8x8 cube arrays as shown in Fig.4, we can get 512 GB SSD board. The 8 x 8 cube array dimension is 71 mm x 71 mm x and SMT space is 1.0 mm. Z-height of SMP cube array is less than 8.5 mm considering solder ball collapse after SMT and package dimensional tolerance.

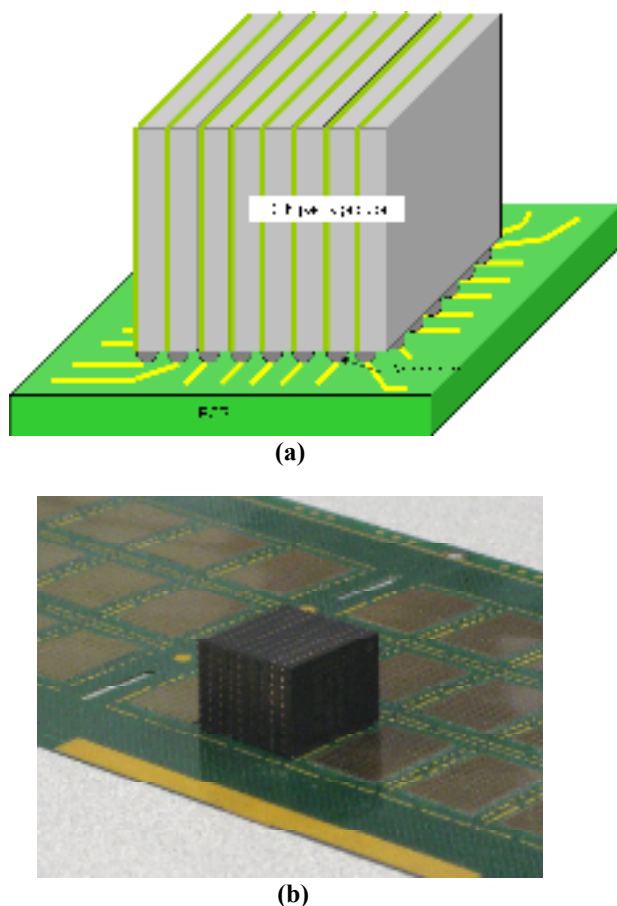


Fig. 3 (a) Schematic drawing of QFN package cube assembled on PCB for SSD application and (b) demonstration of SMP by 8 QFN package stacking

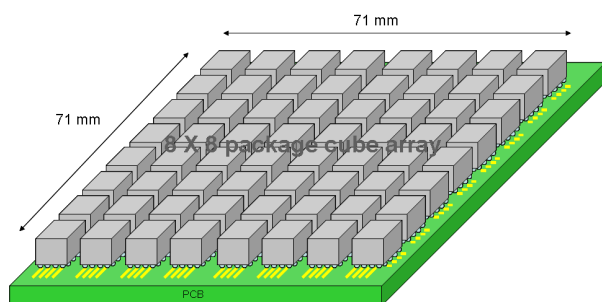


Fig. 4 Schematic drawing of multi cube package: 8 X 8 cube array for SSD board

Advantages of SMP

The newly developed SMP has technical advantages over other package stacking technologies.

This MCP with side mountable capability is cheaper process and smaller space than any of other package stacks useful more than 8 packages because it doesn't need redistribution layer formation process for side wall interconnection or through mold via formation and solder filling process, and solder joints between individual packages. Therefore, the assembly yield for package stack process is higher than other alternative package stacking mostly by solder ball joints. Another advantage for SMT assembly is that this SMP cube is compatible with conventional SMT compatible format without concerns on SMT yield. The SMP cube provides also easy testability for individual SMP cube before SSD board assembly. The last advantage is the design flexibility. We demonstrated SMP cube with QFN package, but its design is not limited to QFN substrate. Even CSP substrate with extended Cu layer for external side wall pad can be used for package building block when the CSP substrate layout is designed for redistributed signal pattern for side wall pad.

In summary, the advantages of the newly developed SMP cube are as follows.

Advantages of the SMPs

- Low cost solution and ultra-high density package stack up solution for SSD application
- Totally compatible with current HVM environment for Individual QFN package manufacturing
- Customer SMT compatible package format
- Testability on individual cube package

Conclusions

We demonstrated new concepts of package stacking technology by Side Mount Package with advantages of easy manufacturing with existing HVM technology and successful implementation for ultra high memory density packaging solution for SSD application. Brief process for high package stack up and board level interconnection are; first, QFN single package configuration by typical die stacking technology with wire bonding and die attach film material on QFN lead-frame. Second, QFN package stack by adhesive layer, and third, QFN package stack up by adhesive layer and the exposed pad is aligned on one area of the package stack up. Finally the solder balls are attached on the exposed pad array for board level interconnection. Total 8 QFN packages are stack up by conventional adhesive layer

and use side wall pad array with solder ball formation is being used for board level interconnection. It provides package stacking solution for any memory capacity in meeting flexibly and quickly for data business market needs.

Acknowledgments

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