

High Accuracy Placement Enabling High Density and Fine Pitch in 3D-IC with High Density TSV, with Chip to Wafer (C2W) Bonding Approach

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Abstract

With the advent of 3D-IC and the increased Packaging density, the introduction of Through Silicon Via technology and the associated High Accuracy Placement and Bonding Challenges introduce new requirements to make Chip to Wafer population a reality. It becomes even more critical when Chip Sizes increase while the Bumps dimensions or the TSV pitches decrease. The paper describes the know how acquired in Bonding High End Infrared Imager, either with In-Situ Reflow or Thermo-Compression Techniques which are compatible with interconnection metal-to-metal or with creation of inter metallic (i.e. Cu-Cu, CuSn). The Thermo-Compression will be illustrated by a technique of micro insertion into indium for an imager application.

1. Introduction

The 3D-IC Integration enables the continuation of Moore's law [1]. Wafer bonding techniques have been used for decades in various areas of microelectronics. The use of Wafer to Wafer bonding implies that chip dimension are identical for all layers and the yield decreased dramatically with the number of layers [2]. Die-to-wafer bonding is an attractive and promising method, in which chips from one wafer are diced and then joined to another die or to a wafer [3]. Thus, only good die are joined together and dissimilar technologies can be joined. With the introduction of high density Through Silicon Vias (TSV) with diameter down to 5µm and below, together with the chip size increase, the Chip-to-Wafer Post Bond alignment accuracy becomes more stringent. Not only lateral positioning is important, but the parallelism of the die with respect to the wafer becomes a critical parameter.

2. Chip-to-Chip and Chip-to-Wafer Bonding

Compare to Wafer to Wafer Bonding (W2W), Chip Stacking and Chip to Wafer (C2W) Bonding approaches suffer of a potentially lower throughput since each die is placed individually. Bonding can be performed individually or, if the process allows, globally after placing all Chips. The lower Throughput is balanced by the benefit of bonding known good die to known good bonding site of the wafer, increasing the yield significantly.

Additionally, the Chip-to-Wafer (C2W) assembly method enables mixing heterogeneous technologies, side by side or stacked. Chip-to-Wafer bonding is also used for wafer reconstruction, chip resizing and connection redistribution to achieve 3D Die-stack of different technologies [4].

Most of the bonding techniques used for die-attach or flip-chip bonding (fig. 1) can be applied:

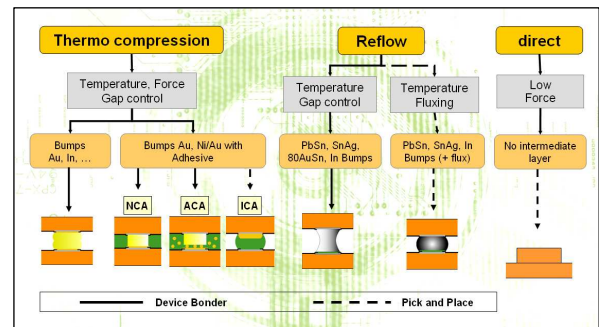


Fig. 1: Flip Chip processes

- Reflow soldering,
- Thermo-compression including Cu-Cu bonding [5],
- Insertion bonding [6],
- Thermo Sonic bonding,
- Adhesive Joining
- Fusion Bonding (heterogeneous integration) [7].

Throughput is increased when using collective bonding techniques:

- a. Reflow soldering can be performed in neutral gas environment or vacuum:

- At first step, chips are placed on the wafer using high throughput pick and place techniques,
- At second step, collective reflow of the populated wafer insures soldering as well as final chip-to-wafer self-alignment in a dedicated process chamber.

b. Thermo Compression bonding:

- Collective bonding can be applied to thermo-compression using a tacking step,
- Then a press with heating chucks completes the bond collectively.

3. Example of TC Bonding: Imaging Arrays

Two main flip-chip joining techniques are generally used for the fabrication of heterogeneous imaging arrays [8].

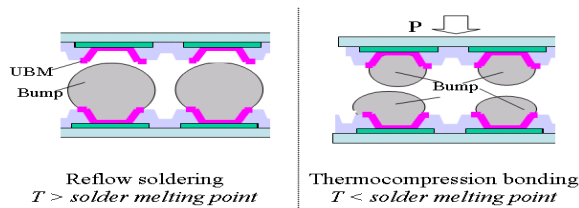


Fig. 2: Flip-chip techniques (imaging arrays)

When high pin count (i.e. 10k connections per mm²), low pitch (i.e. <10μm) complexity is required, the classical C4 reflow soldering technique (Fig. 2a) do not allow balancing the chip planarity defects, which leads to unconnected bumps. The CTE mismatch can also be a major issue due to high solder reflow temperature (for heterogeneous materials X, Y mis-registration can approach pitch value at soldering temperature)

The Thermo-Compression technique (Fig. 2b), by using force and plastic deformation of solder bumps, can compensate Z non-planarity. High Pressure is required, which can induce local overpressure defects or generate shorted bumps during compression. X/Y CTE mismatch can also be a problem if compression temperature is set too high.

a. Insertion approach

Reference [9] describes a new “insertion” flip-chip technique using micro-tubes (fig.4) and solder lands (fig.5) to aim at achieving ultra fine pitch (< 10 μm) and high bumps count (2000x2000) connections.

Process scenario

The following global process scenario was then developed: Chip #1 is processed with soft solder

lands, and Chip #2 with “insertion” tips/micro-tubes. Then, after a classical alignment the metal micro-tubes arrays are inserted into solder lands arrays at low temperature and low pressure. This process is:

- **Flux less:** The gold plated micro-tubes break the native solder oxide film establishing an immediate electrical contact. No flux cleaning is required
- **Low pressure:** Thanks to the sharp micro-tubes geometry and high indium solder ductility, insertion forces have to be reduced (<0.5mN/connection) like the local overpressure. Applied forces can be handled by conventional flip chip bonding equipment even for high very pin counts (i.e.: > 4 millions connections)
- **Room temperature:** CTE mismatch issues are suppressed; the bonding step can eventually be completed by solid-solid diffusion

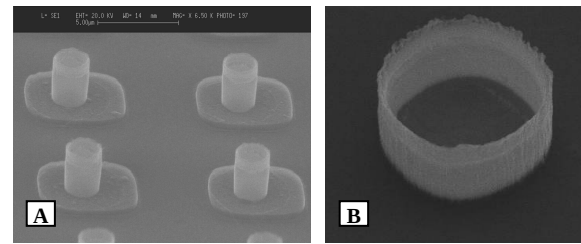


Fig.4: μtubes fabrication results - Top Views

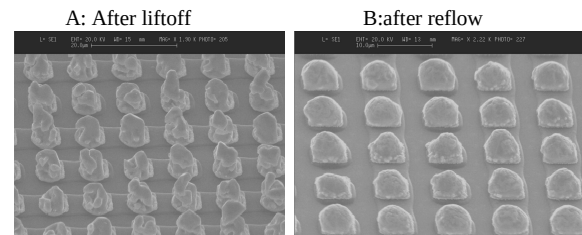


Fig. 5: SEM images of 10μm indium solder bumps made by lift-off technique

b. Flip chip by insertion: process development

As-built chips were readily assembled by insertion with 0.5mN applied load per connection, this resumes to 2kN applied load per chip for 4. 106 total vertical connections. First electrical results showed that parallelism during insertion was a critical parameter. Next section evaluate how parallelism control during insertion can influence connection yield

Parallelism control

The room temperature, low force assembly process was developed using the SET FC300 type machine. Chip parallelism can be controlled by 2 ways evaluated in this paper (Fig. 8 & 9).

- Type 1-Pure optical parallelism (Fig. 6): upper chip is held by a rigid (flat) holder tool, chips parallelism is tuned prior to thermo-compression thanks to the integrated optical autocollimator. Parasitic parallelism offset can occur between alignment position (separated chips) and insertion position (chips in contact).
- Type 2-Optical parallelism + Auto Leveling (Fig. 7): upper chip is held by a specific “Self Leveling holder tool” which can deform under applied load. Optical parallelism is still performed in upper position (same as 1) but, during the insertion step, the Auto Leveling tool can deform mechanically if load proves to be non uniform. This allows spreading uniform load, recovering parallelism between mated chips surfaces without X, Y in-plane misalignment.

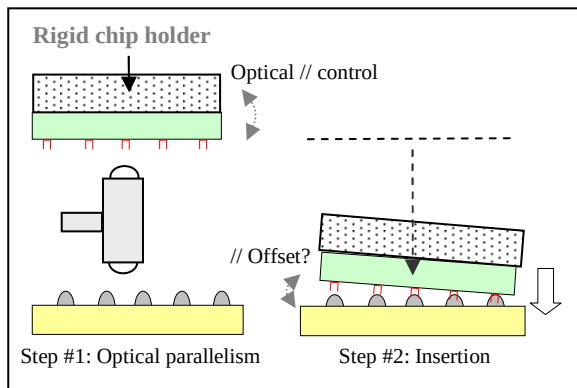


Fig. 6: Chip 1 = parallelism without auto levelling

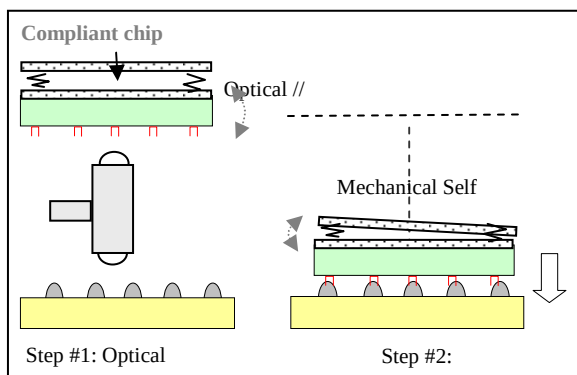


Fig. 7: Chip2=parallelism aided by mechanical auto

The two parallelism principles were evaluated and compared on two hybridized chips using the SET FC300[®] bonder in thermo-compression configuration at 2kN insertion load (i.e. 0.5mN/connection). The alignment capability of the bonder is a primordial parameter and pre-measured misalignment proved to be less than $\pm 0.5 \mu\text{m}$ at the 2kN compression force required in our application, chip parallelism was pre-tuned in alignment position

thanks to the built in autocollimator (spot diameter 8mm, pre-leveling accuracy of $25\mu\text{rad}$).

The bonding requirements for high density and fine pitch of the Infrared imagers are similar to the new demand for the 3D interconnect technology using high density TSV.

4. Equipment

Depending upon the interconnection density and the selected bonding technology, either pick-and-place machines or high accuracy die/device bonders are used for attachment of the die to the wafer or to the previous die.

For 3D-IC integration, the increased density of the Through Silicon Vias (TSV) requires submicron post bond accuracy and consequently Ultra High Accuracy Chip-to-Wafer (C2W) Bonder.



Fig. 8: SET-FC300 High Accuracy (0.5 μm) Die/Flip Chip Bonder

The SET-FC300 (fig. 8) features 0.5 μm post bond accuracy using in situ thermo-compression; it has the potential of 0.25 μm when tacking at room temperature.

The increase in density of bumps or TSV also impacts the parallelism requirement during placement and/or bonding sequences. The addition of a self leveling stage to an accurate die/Flip chip bonder (fig. 9) enhances the bonding yield by improving the Chip-to-Wafer leveling without any loss in XY Accurate.

The Self levelling system is a flexure stage buildt in such a way that the pivot point corresponds

to the surface of the component being built. This proprietary system accommodates bonding force up to 400 kilogrammes while allowing automatic tip and tilt during the thermocompression sequence with a sensitivity as low as 0.76 mN.m per microradian. It can compensate up to 100 microradian, but thanks to the active preleveling available on the system, at the maximum, only 20 microradians may have to be compensated.

The positive action of the self leveling system has been demonstrated by a micro-insertion technique applied to infrared sensor at CEA/LETI.

This technique has the advantages of requiring lower force [10], but need tighter control of the parallelism. It also enables soldering for ultra fine pitch of large devices [9].

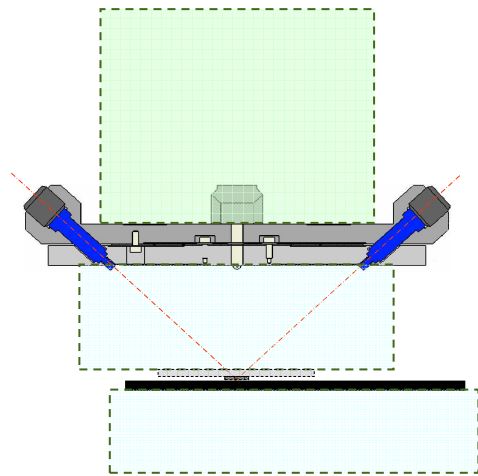


Fig. 9: Self leveling system as used on the SET-FC300 Accurate Die/Flip Chip Bonder

5. Conclusions

Mixed “Pick & Place / Collective Bonding” processes technique can insure high throughput when decoupling operations. 3D-IC at wafer level using chip-to-wafer bonding method can guarantee high density packaging, thanks to the submicron post bonding accuracy of the assembly technology. Increased density requires higher placement accuracy and tighter control of the parallelism; yield improvement is obtained by using self leveling capability.

6. References

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