

Novel Multi Chip Packaging Method Using Stochastic Self Assembly

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Abstract

The objective of this project was to apply a self-assembly process in the development of a functional battery assisted passive (BAP) tag. A multifunctional sensor using RF signals was designed and fabricated. Multiple ASIC and OTS IC dice were placed in a multi layer flexible carrier by applying a self assembly method and packaged to archive inexpensive micro sensors. The interconnections were made using printable conductive inks to replace previously used thin film processes and to reduce costs. This flexible package consists of more than one polymer substrate with the devices embedded in it and connected to each other and are finally covered by polymeric planarization layers where the traces are printed on leading to the package terminal of the device.

The RF system can receive an RF signal, store the required info, and respond to stored information when prodded to do so through an RF signal. The flexible package consists of a polymer substrate with the device embedded in it and covered by a polymer. The polymer cover layer protects and sandwiches the device between the substrate and itself. The interconnection from the chips to the package terminals is provided using vias in the cover-layer polymer. The package terminals on the cover-layer surface interconnect with the device through the vias in the cover-layer over the terminals on the device. Metallization is accomplished using a photolithography process.

Keywords: Flexible electronics, self assembly, redistribution layer, miniaturization, RF, micro-sensors, semiconductor packaging.

Introduction

The key to miniaturization of electronic devices lies in the development of technologies to fabricate high density interconnects and packaging methods which can assemble small bare dice in least volume of space as possible. Traditional printing methods and copper etching methods can produce

conductive traces on a circuit board with feature sizes as small as 100 μm . Several direct-write methods have been developed to produce conductive traces in the 10-100 μm range. Similarly, several stochastic as well as deterministic methods have been developed to assemble bare dice on to a circuit board. The most commonly used deterministic assembly method used in the industry today is the

pick and place method. This method can assemble up to 34,000 components per hour on a circuit board with accuracy as small as 95 μm [1, 2]. However, most pick and place machines or chip shooters are limited to assembly of components of size greater than a millimeter because van der Waals, surface tension and electrostatic forces of attraction in submillimeter sized components are significant compared to the gravitational force acting on the component resulting in placement inaccuracies[3]. In order to assemble sub-millimeter sized components, several stochastic self assembly methods have been developed. One of them is Fluidic Self Assembly (FSA[®]).

The principles and description of the FSA[®] process has been described elsewhere[5]. FSA[®] and associated processes have been previously investigated for application to inexpensive micro-sensors. The existing self assembly methods are used to assemble a single bare die on to a part-printed/hybrid flexible circuit board. Much as we would like to have the least number of components in an electronic device, it may not be possible to do so as most devices are made of several active components (ICs) and passive components (resistors, capacitors, inductors, transformers, etc.) and therefore forming a *hybrid microcircuits*. The term *hybrid microcircuit* is derived from the use of more than one technology to fabricate the flexible electronic devices [5]. Although a lot of research has been done to deal with all the methods individually, the integration of all these technologies to fabricate a fully functional micro-sensor presents its own challenges.

Multilayered Self-Assembly for Microsensor Applications

This paper presents a novel approach for assembling a functional battery assisted passive (BAP) tag by applying stochastic self assembly methods such as FSA to assemble bare dice on both sides of a flexible circuit board. This process applies a novel design of trapezoidal shaped dice which are self-assembled on both sides of a flex board. At first a Redistribution Layer (RDL) is fabricated on commercially available dice such that the orientation of the die after the assembly process does not affect the functioning of the circuit. The concurring

receptors are fabricated on both sides of a thin polymeric flexible substrate using the hot embossing process. The dice are then assembled in the receptors using a self assembly process such as FSA[®]. The trapezoidal shaped dice are interlinked through and traces fabricated using the traditional screen printing process. Finally, this sub-assembly is assembled on a rigid circuit board to form a completely functional BAP tag.

The most important advantage of this design is that although this device uses commercially available off the shelf (OTS) chips the use of the RDL increases the efficiency in the self assembly process. Also, the FSA process is used to assemble three different trapezoidal shaped dice on both sides of flex board forming a multi-layered device hence proving that versatility of the self assembly process to fabricate multilayered and multiple chip circuit boards.

Sensor Design

The BAP tag was designed to work as a multiple sensor for sensing temperature and acceleration and to transmit the data to a receiver at ultra high frequency. Major components included in the device were temperature and acceleration transducers, Charlie-8 modem IC developed by Alien Technologies, Inc., our own proprietary Tenali ASIC, a OTS memory IC, antenna, passive components and a battery. As illustrated in Figure 1&2 below the BAP tag has a flex circuit sub-assembly consisting of the processor, memory and modem ICs self assembled on two sides of a flexible substrate. The ICs have a redistribution layer on top of them which make the interconnect pads symmetrically positioned in such a way that regardless of the orientation of the ICs in receptor sites, the pads will make contact with interconnect traces that form the I/O to the PCB. This works a major advantage for the stochastic self assembly process where the orientation of the ICs in the receptor sites cannot be controlled for square and rectangular dice. This subassembly was integrated with a rigid PCB containing the transducers, power supply, antenna and passive components.

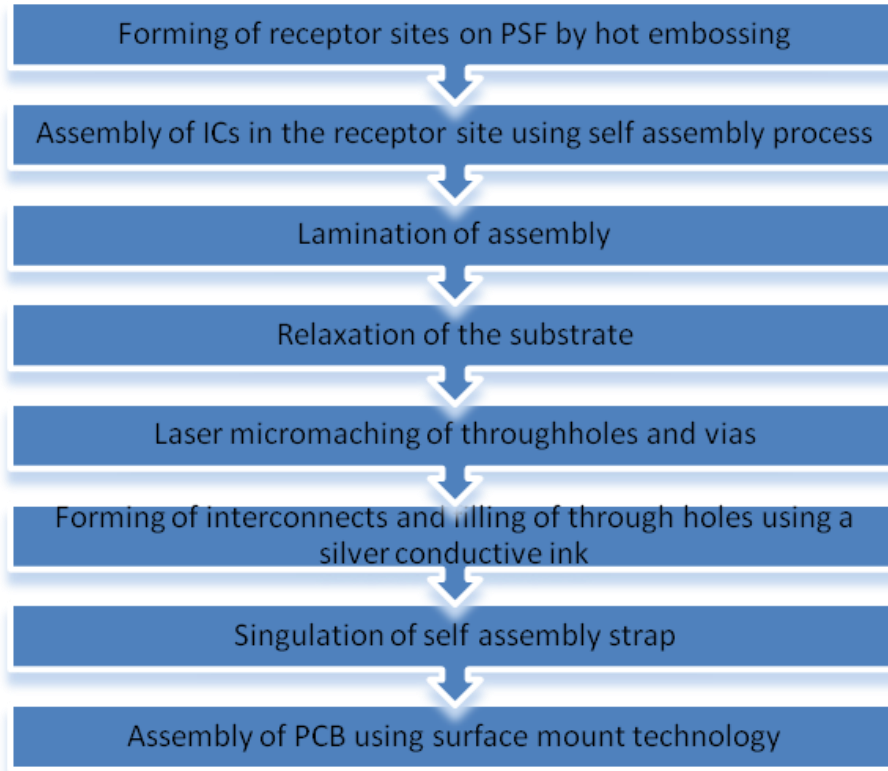


Figure 3: Process flow diagram for fabrication of BAP tag.

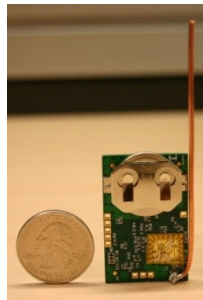


Figure 1: Picture of the BAP tag next to a quarter.

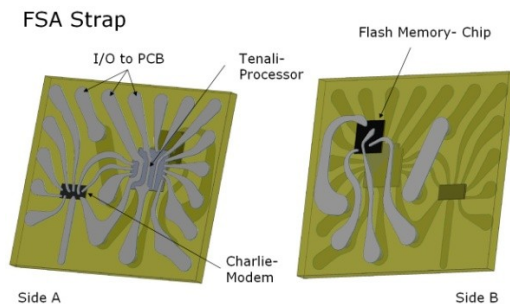


Figure 2: Schematic showing both sides of multilayered FSA subassembly strap.

Sample Preparation

The process for preparation of the BAP tag is illustrated in Figure 3. A 10 mil thick polysulfone (PSF) substrate was hot embossed at 220° C. The surface of the embossed PSF substrate was treated with corona in order to improve its wettability and adhesion properties. The processor, memory and modem ICs are assembled into the hot embossed receptors on both sides of the substrate using a self-assembly process. The assembled substrate was then laminated on both sides using a hot film laminator. Since the lamination process induces stresses on one side of the substrate, it gets warped after each lamination step. Due to this the substrate had to go through a relaxation step in which it was rolled in the opposite direction of its curve. The through holes and via holes in the substrate was micromachined using a 248 nm Optec excimer laser. Interconnect traces were screen printed on the substrate surface and the via holes were filled with a syringe using Electrodag® PF-050 advanced polymer thick film silver conductor by Acheson Electronic Materials

and cured at 121 °C for 15 minutes. The flex circuit was then carefully singulated using a laser.

The singulated flex strap is assembled on the PCB using a conductive adhesive. The passive components, transducers and power supply on the PCB were assembled using surface mount technology while the antenna was hand soldered on to the PCB during the prototype fabrication.

Characterization and Inspection

The prototype fabrication of the self assembly strap involved visual inspection after every processing step. At first, a redistribution layer was fabricated over the memory and modem chips. As shown in Figure 4, the modem chip has twelve input-output pads located on the edges of the die. This made the chip unsuitable for stochastic self assembly as the orientation of chip was important for the

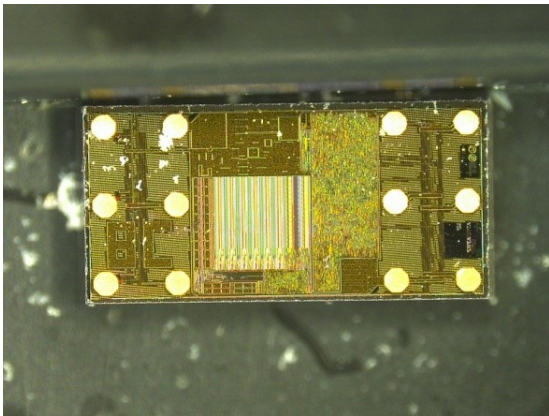


Figure 4: Image of the Charlie modem before redistribution layer is fabricated.

proper functioning of the device. The introduction of redistribution layer on the chip made interconnect pads to be positioned symmetrically at the center of the chip and hence making it compatible with stochastic self assembly (Figure 5). Similarly, a redistribution layer was fabricated on OTS memory chip which had four input-output pads on its edges. As shown in Figure 6&7 the pads were redistributed symmetrically at the center such that they became compatible with the stochastic self assembly processes. The Tenali processor already has a notch on its edge and therefore, its is self assembled in

only one orientation. Hence, it does not need a redistribution layer (Figure 8).

Similar visual examination methods were used to inspect the self assembly of chips in the hot

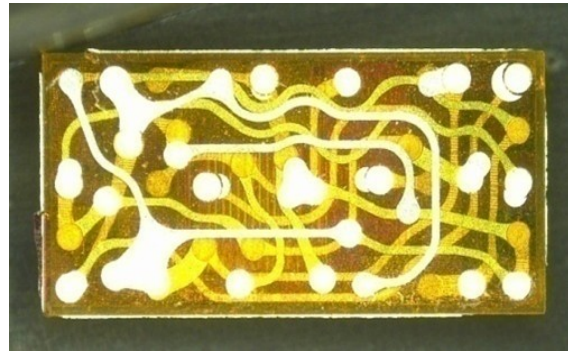


Figure 5: Image of the Charlie modem after redistribution layer is fabricated.

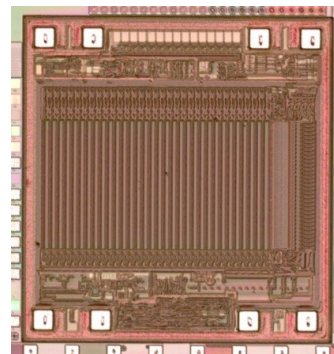


Figure 6: Image of the memory chip before redistribution layer is fabricated.

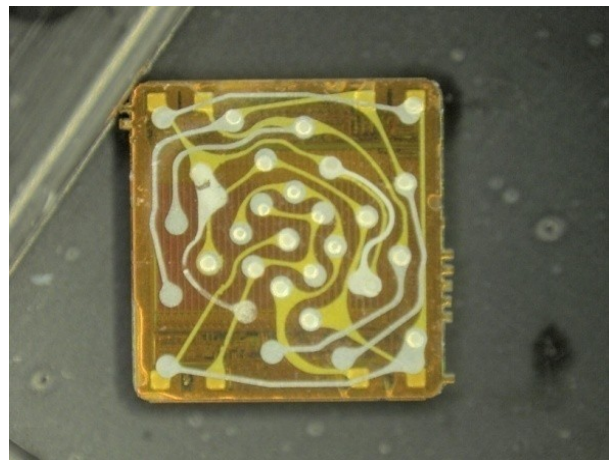


Figure 7: Image of the memory chip after redistribution layer is fabricated.

embossed polysulfone surfaces. The self assembled strap was then mounted on the rigid board using conventional surface mount methods and tested. After the functional testing the strap was dismounted from the rigid board and molded in a resin chuck which was grinded and polished to obtain the the cross-section profiles.

Results and Discussion

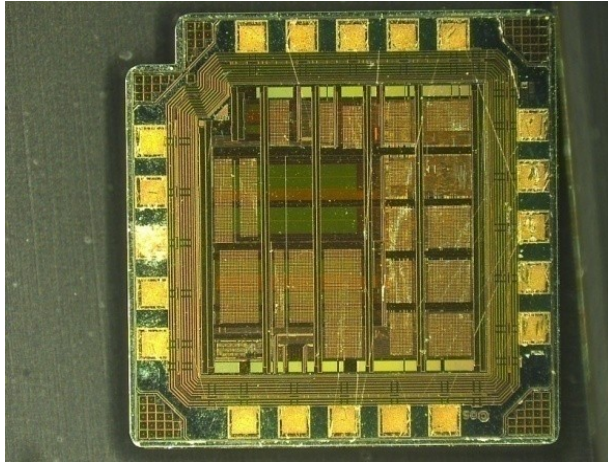


Figure 8: Image of the Tenali processor with a notch on its edge to which leads to its self assembly in one orientation only.

Initial results from the functional test clearly indicated that this hybrid approach can be used to fabricate a completely functional device. However, out of the first few prototypes tested only a fraction demonstrated partial functionality while the others were unable to show any transmission of signals at all. As illustrated in Figure 9, the primary reason for a number of failures was identified to be the improper filling of via holes between the pads of the redistribution layer and the conductive trace pattern. Another cause of failure was found to be the damaging of the pads of the redistribution layer during the ablation of via holes with an excimer laser. In order to eliminate these problems, a syringe based method to deposit silver conductive polymer thick film into via holes was introduced. This aided in the elimination of these problems. Also shown in Figure 10 is the Tenali chip embedded into a hot embossed receptor site. The figure illustrates that the assembly of the Tenali processor chip was successful and there was no linear or angular

displacement observed during the self assembly process. This demonstrates the capability of the self assembly process to assemble bare dice of sub millimeter size into receptor sites.

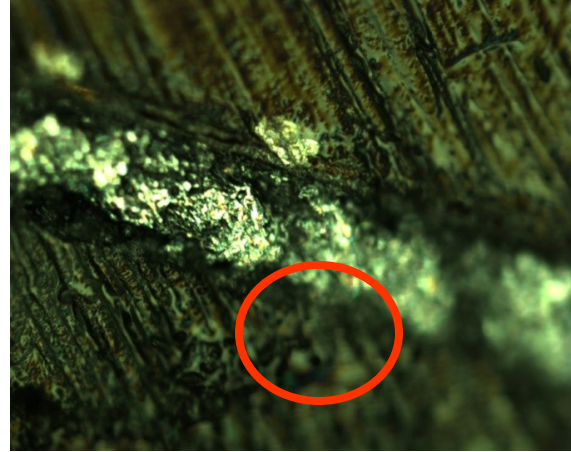


Figure 9: High magnification image the cross-section of the self assembled Tenali chip demonstrating the unsuccessful filling of the via hole.

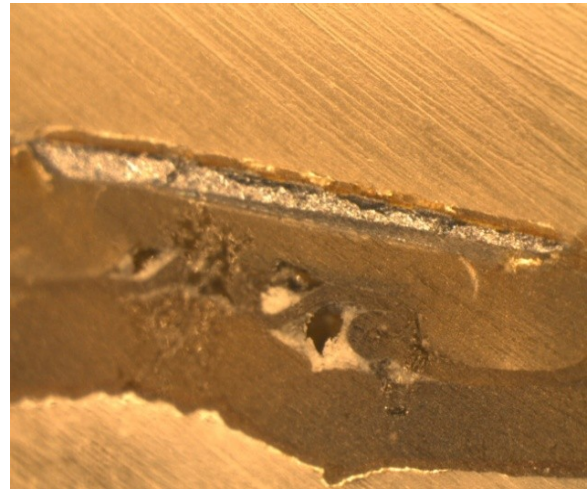


Figure 10: Cross-sectional profile of a packaged Tenali chip in the receptor site.

Conclusions

Preliminary tests performed have indicated that the hybrid method of using the redistribution layer over self assembly chips can be successfully used to fabricate a fully functional hybrid microelectronic device. From our previous research experience we know that the individual technologies, which are, the use of redistribution layer, fine line printing using thick film technology,

self assembly of bare dice into substrates, via hole filling and surface mount technology when applied separately will work as expected. However, the combination of so many processing steps into a single product presents its own challenges. The most common problem faced during the assembly of the micro sensor was the filling of the via holes with a silver conductive ink. A syringe based process used for dispensing the silver ink into the via holes was found to give better results. Further research must be carried out to identify and minimize the modes of failure in this process.

Acknowledgements

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