

Design and Reliability of μ PILR™ Package-on-Package (PoP)

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Abstract

Manufacturers are increasingly challenged to meet reliability, performance, form factor and cost objectives for today's enhanced mobile electronics. 3D packaging is fast becoming the package design of choice to overcome the technical limitations of conventional interconnect technology. 3D packaging solutions are available in several forms, some of which are chip-stack, package-in-package (PiP) and package-on-package (PoP). Each version has its own advantages and disadvantages, with chip-stack and PiP offering smaller size and higher internal IO, and PoP offering greater yield and system flexibility.

In this paper, the current design possibilities of PoP for leading-edge, feature-rich mobile electronic applications are presented. The impact of package miniaturization on memory and logic package IO is presented. The design trade-offs of different designs and their features and limitations are listed. A new form of interconnect called the μ PILR platform is presented in the PoP format. This technology is characterized by 3D interconnects made of solid copper that enable high aspect ratio interconnects, which enable higher IO and finer pitch for the top layer and larger gap between bottom IO for more trace escapes on the main board.

To characterize this technology, the μ PILR PoP solution was fabricated and tested for reliability. Assembly results have shown that the SMT yield at fine pitch is significantly higher as compared to that of conventional solder ball PoP. Thermal cycling and drop tests results show the μ PILR PoP solution to have high reliability, especially for drop tests. Failure analysis has shown that the μ PILR technology interconnect acts as a crack growth inhibitor and therefore increases the lifetime under dynamic loading.

In conclusion, the design, analysis and reliability results show that μ PILR PoP technology meets industry requirements for miniaturization without compromising yield or reliability.

Introduction

CSP has been the main enabler of microelectronics systems miniaturization over the last two decades. Over the last few years, 3D packaging has extended packaging miniaturization through placing multiple chips (2-5) within the same footprint of a single chip

package. The most common 3D package is the chip stack package where multiple chips are placed over each other and wire-bonded to the substrate before molding. The drawbacks of this approach are compound yield issues, chip size differences and wire-bonding complexity of multiple chips to the same substrate.

To overcome these limitations, the industry moved to stacking packages on top of each other. This approach is most suitable for stacking identical and low IO chips, and hence was first used for DRAM stacking [1]. That approach was extended to be used also for mixed chips stacking, especially for the digital computing portion of wireless mobile systems. Depending upon the particular choice of chips (baseband/applications processor and DRAM/NAND/SRAM memory) and vendor, the PoP continues to evolve [2,3] as shown in Figure 1.

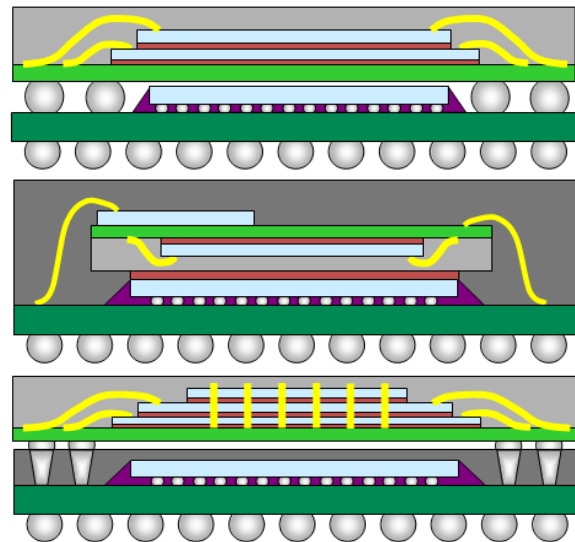


Figure 1: A few 3D packaging approaches for mobile computing

The main purpose of PoP is to enable miniaturization through packaging of multiple chips. The requirements to achieve this goal are:

- Fine pitch IO for the stacked packages so that the package size can remain as small as possible while providing 150-200 IO for the top packages

- Good reliability under shock/impact to withstand multiple drops
- High manufacturing yield to minimize compound yield losses
- Flexibility of matching different top and bottom packages to support multiple sourcing and product differentiation and
- Conventional processes and materials for low cost

When the current PoP solutions are compared against these requirements, it is noticed that each of them has advantages and limitations. For example, the solder BGA stack has the advantages in yield, flexibility and low cost, but has limitations in IO and pitch. On the other hand, the PiP/chip stack has high IO and fine pitch (wire-bonds), but has limited yield and flexibility.

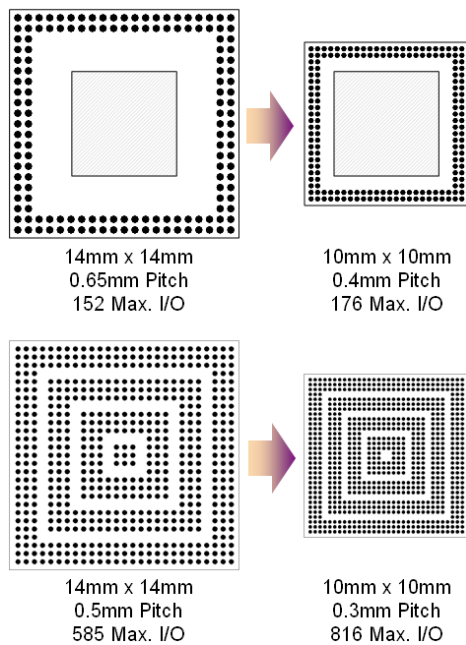


Figure 2: The interconnect requirements to enable package miniaturization

To determine the extent of benefits through pitch reduction, a design study is shown in Figure 2 and Tables 1 and 2. The current PoP package in the industry is shown on the left. With IO pitch reduction, not only can the package size be reduced to about half of the original size, but the IO can still be high enough to meet future needs. The key enabler for this pitch reduction is the package interconnect.

To be able to obtain all the advantages, a PoP structure is needed that is composed of discrete stacked packages for flexibility, utilizes conventional processes for high yield and low cost, offers fine pitch for top packages to continue the miniaturization trends, and has

good reliability under drop testing. In the following sections, the μ PILR PoP solution is presented that has all of the above mentioned benefits.

Table 1: The top package IO

Top Package Body Size	0.65mm Pitch	0.5mm Pitch	0.4mm Pitch
14mm	152	200	256
12mm	128	168	216
10mm	104	136	176

Table 2: The bottom package IO

Bottom Package Body Size	0.5mm Pitch	0.4mm Pitch	0.3mm Pitch
14mm	585	916	1584
12mm	432	672	1200
10mm	297	468	816

μ PILR Interconnect

Details of the μ PILR interconnect platform and its manufacturing method have been published before [4]. As shown in Figure 3, it is a 3D interconnect structure made of solid metal such as copper that is formed through the etching of a sheet of metal. This method offers very coplanar interconnects that can be made at fine pitch. The dimensions can be varied depending on the design.

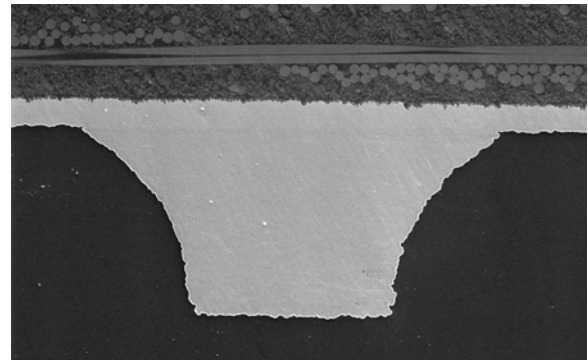


Figure 3: μ PILR interconnect as package IO. It is 125 μ m tall and has a base of 175 μ m at a pitch of 400 μ m.

One of the key advantages of the μ PILR interconnect platform that enables fine pitch and high aspect ratio is illustrated in Figure 4. For a conventional solder ball stack, it is not possible to clear a gap of 0.3 mm (the bottom package thickness) since a solder ball with a minimum of 0.4 mm diameter is needed and it will cause shorts if built at 0.5 mm pitch. For the μ PILR solution, a solder ball of 0.3 mm diameter is enough to form the interconnect, and after reflow it becomes

columnar thereby allowing for finer pitch than 0.5 mm. The assembly and reliability results of the high aspect ratio (columnar) interconnect will be presented in the following sections.

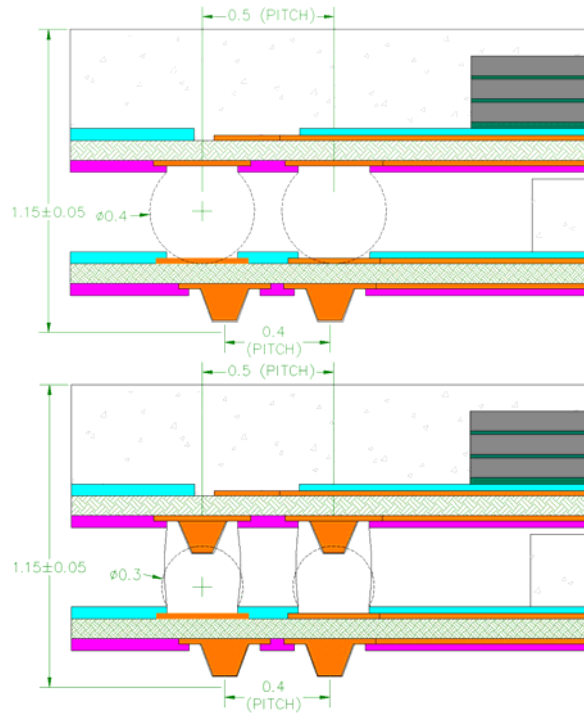


Figure 4: The PoP interconnect size for solder bump and μ PILR interconnects.

Test Vehicle Design

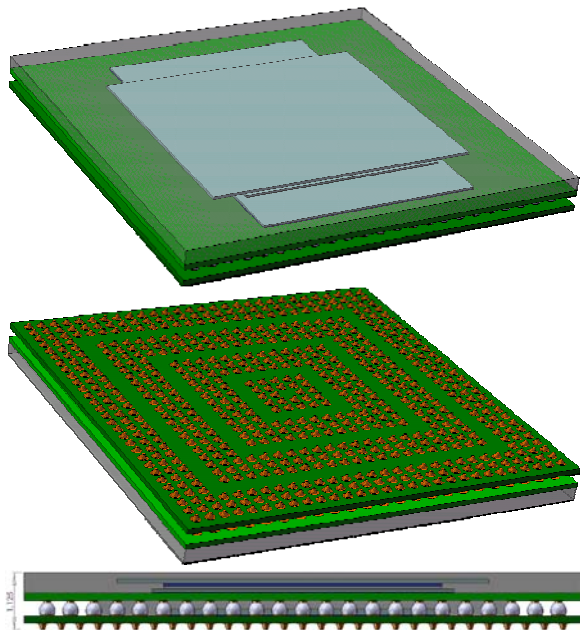


Figure 5: μ PILR PoP test vehicle design

A daisy-chain test vehicle was designed to quantify the assembly and reliability of the μ PILR PoP solution. The design is as shown in Figure 5 and the details are given in Table 3. In summary, the top package, which is typically used for a memory subsystem, has 168 IO arranged in two rows of 0.5 mm pitch around the package perimeter. The bottom package, which is typically used for a baseband or mobile applications processor, has 672 IO at 0.4 mm pitch arranged in a depopulated area array.

Table 3: μ PILR PoP test vehicle design details

μ PILR PoP details	memory (top) package	logic (bottom) package
Size (mm)	12x12	12x12
Thickness (mm)	0.757	0.52
Chip size (mm)	9.41x6.7 (3 stack)	6x6
IO	168	672(bottom) / 168 (top)
Pitch (mm)	0.5	0.4 (bottom) / 0.5 (top)
μ PILR height (mm)	0.12	0.12
SM opening (mm)	0.27	0.27 (bottom & top)
Bump diameter (mm)	0.275	0.275 (bottom) / 0.3 (top)
Bump height (mm)	0.225	0.15 (bottom) / 0.225 (top)

The daisy chain layout is as shown in Figure 6. Multiple daisy chains were made to accurately determine the location of failure. The daisy chains were divided into two groups, critical and non-critical. Typically, the corner IO are designated as mechanical interconnects only and their failure does not impact the functional performance of the system. For this reason, the corner IO (4 in each corner) of the bottom package were part of a separate daisy chain and it was designated as non-critical. All the other IO were part of critical daisy chains. This allowed for tracking of failures at the corner IO separately from the rest of the IO.

Test boards for drop testing and thermal cycling were designed to the specifications outlined in JEDEC standard JESD22-B111. The test boards had via on pads (VOP) and were 250 μ m in diameter and NSMD with a copper organic solderability preservative finish. A sample test board is shown in Figure 7. The test boards were designed to be connected with cables such

that in situ resistance measurements can be done during thermal cycling and drop tests.

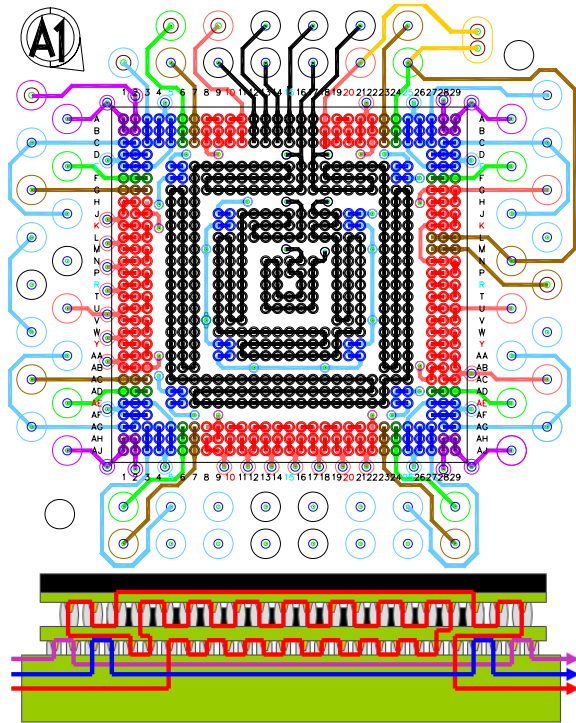


Figure 6: The daisy chain nets for the bottom package. Only the purple nets (4 IO in each corner) are non-critical and all others are critical. For the top package, all IO are part of the critical nets.

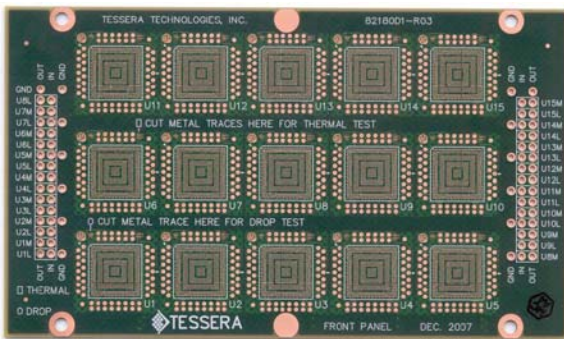


Figure 7: The test board for drop and thermal cycling tests

Package Assembly

The μ PILR substrates were fabricated using ROHS-compliant glass-reinforced FR4 dielectric materials. The μ PILR substrates were assembled into test packages using conventional package assembly processing and materials. The test vehicle used three mechanical silicon chips in the top package and one mechanical silicon chip in the bottom package. A compliant chip attach material and filled epoxy

overmold was used in both the top and bottom packages. The bottom package is shown in Figure 8.

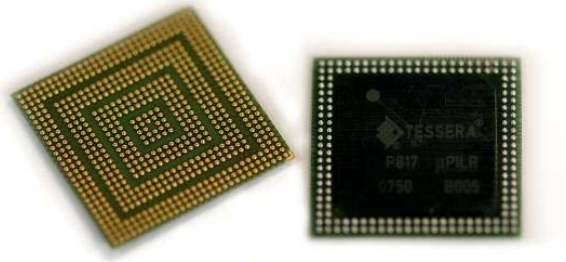


Figure 8: The bottom package after assembly

The μ PILR PoP test vehicle was stacked on the reliability test board using high-volume SMT equipment, and is shown in Figure 9. The SMT process was performed in the following sequence:

- solder paste was applied to the reliability test board using a stencil
- the logic package was placed over the solder paste on the test board with a high-volume pick-and-place machine
- the memory package was dipped into a paste containing both flux and solder particles
- the memory package was placed directly on the logic package
- the PoP stack was put through a solder reflow process

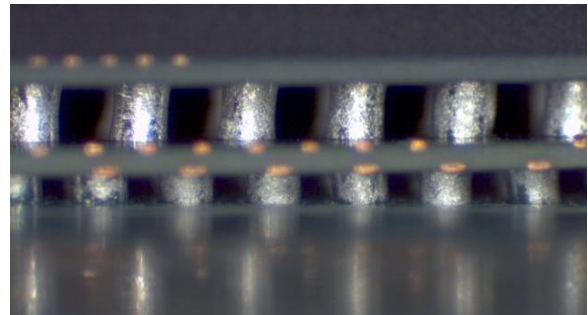
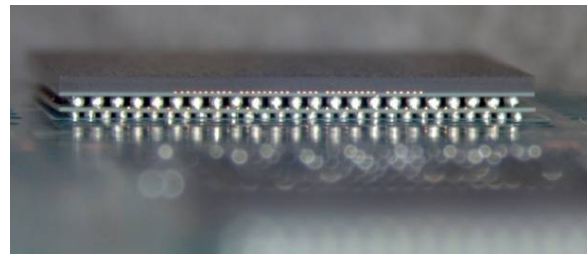


Figure 9: The μ PILR PoP on the test board after the SMT process

No package underfill was used subsequent to the SMT process. All solder used in the study was SAC 305. The substrate pad and μ PILR interconnect finishes

were Ni/Au electroplated. Figure 10 shows an SEM image of the cross-section of the completed μ PILR PoP test vehicle after the SMT assembly process. The top package solder joints at 0.5 mm pitch are approximately column-shaped, which helps in reducing the risk of solder bridging, especially at finer interconnect pitches. The bottom package solder joints at 0.4 mm pitch have a very low profile of less than 150 μ m.

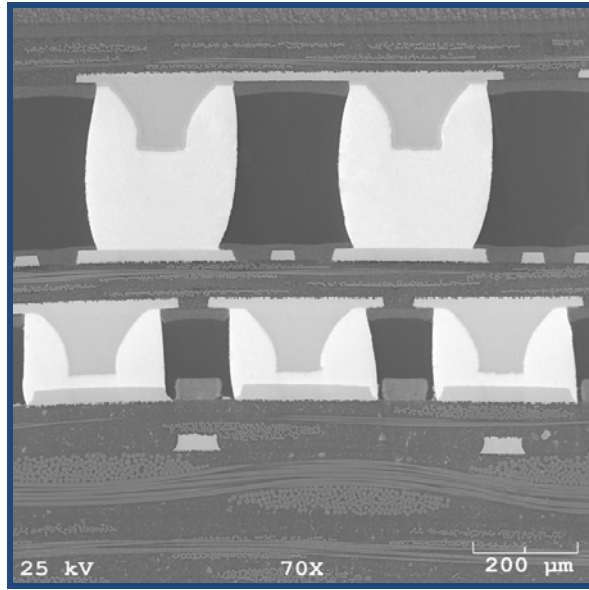


Figure 10: The μ PILR PoP cross-section

In assembly trials of 0.4 mm pitch area-array devices, it was found that the presence of the μ PILR copper pins can help improve SMT yields of the package-to-board interface by reducing the incidence of solder bridging vs. a more conventional BGA package with standard solder pads. Figure 11 shows the SMT results for μ PILR PoP solution. The yield was 100% with no solder bridging or opens. The assembly was also done for conventional PoP with solder ball interconnects. Extensive solder bridging was found, and the results are shown in Figure 12. It is suspected that the SMT yield benefit for the μ PILR interconnect arises from the enhanced solder wetting of the copper pin combined with the mechanical stand-off that keeps the logic package away from the test board during the reflow process.

Reliability Testing

Following the SMT process, the μ PILR PoP solution was tested according to JEDEC drop test standard JESD22-B111, as well as thermal cycling from -40°C to 125°C per IPC-9701 TC3 specifications. Drop test components were subjected to a peak load of $1500\text{ g} \pm 100\text{ g}$, with a peak pulse duration of 0.5 msec. The test boards were assembled with all 15 test sites fully populated.

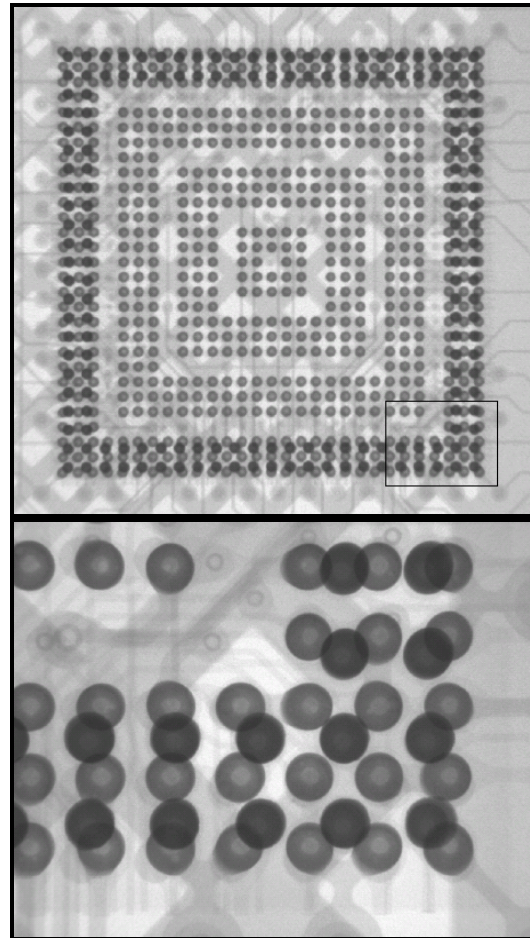


Figure 11: The x-ray images of the μ PILR PoP assembly show no solder bridging.

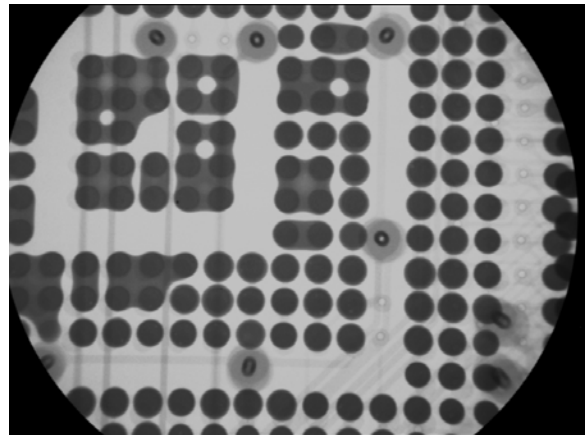


Figure 12: The x-ray images of the solder ball PoP assembly show extensive solder bridging.

Figure 13 shows a Weibull plot of drop test results for the critical package nets. The B_1 life was 73 drops and the characteristic life (η) was 457 drops for the μ PILR PoP solution. This reliability level is more than

twice the target of 30 drops per the JESD22-B111 standard, and is accomplished without the need for package underfill. But for the conventional PoP with solder balls, the B_1 life is 0.117 drops and the characteristic life (η) is 53 drops. This shows severe limitation for the conventional PoP at fine pitch and it would require an underfill to be reliable.

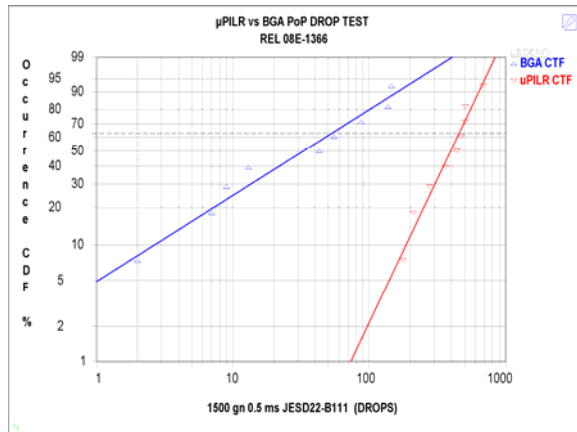


Figure 13: Drop test results for μ PILR and BGA PoP packages for critical nets

The observed failure modes are shown in Figures 14 and 15. In actuality, the first failure in the μ PILR PoP solution was not the interconnect but the test board. The test board dielectric under the pad cracked causing a trace break. For the conventional PoP, the first failure was typically a solder joint crack at the package pad. The reason of such high reliability in drop for the μ PILR interconnect is due to high fracture toughness from crack inhibiting nature of the 3D μ PILR shape [5].

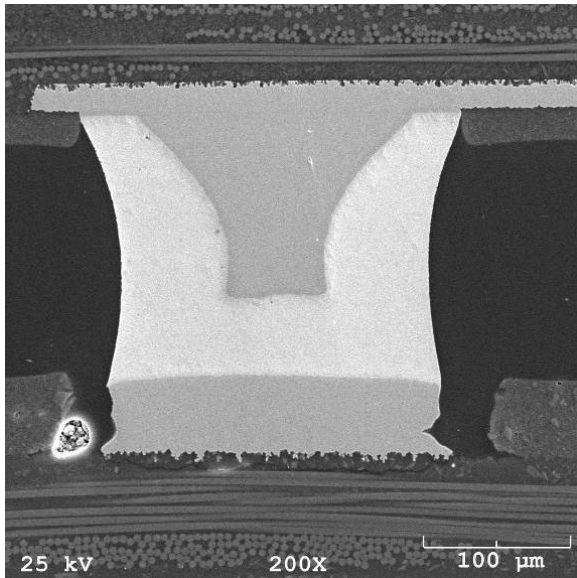


Figure 14: Typical first drop test failure mode for μ PILR PoP was test board cracking under copper pad

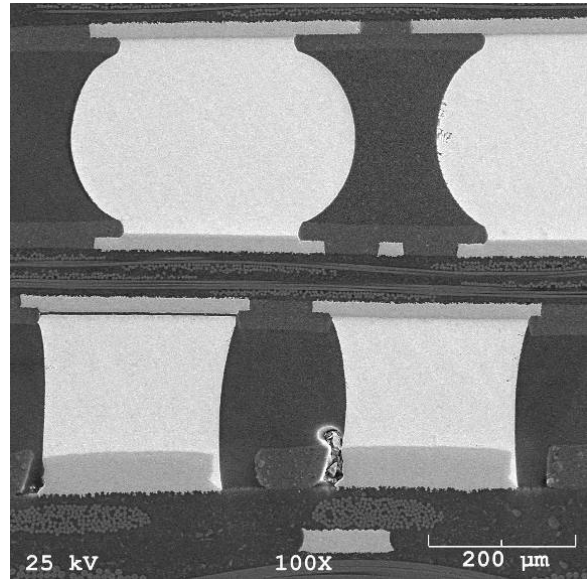


Figure 15: Typical first drop test failure mode for BGA PoP was solder joint cracking on the bottom package.

For thermal cycling from -40°C to 125°C , there were no failures observed for the μ PILR PoP solution up to 2500 cycles.

Conclusion

The package miniaturization efforts have been ongoing in the industry over the past two decades since the advent of CSP. But the demands for miniaturization are growing with increasing functionality in mobile systems as they are very sensitive to form factor and weight. 3D packaging has become the mainstay in this application space, especially for the digital computing portion. PoP is the preferred solution due to its low cost and flexibility. But it has fine pitch and reliability limitations. To overcome these limitations, a μ PILR interconnect solution was presented that meets the objectives of 3D packaging in terms of size, IO pitch, number of IO, yield, flexibility and cost.

The μ PILR interconnect consists of an array of solid copper structures that are coplanar. Due to their 3D nature, they offer fine pitch capabilities while maintaining the ability to span gap between stacked packages.

A design study was presented that showed that 0.4/0.3 mm pitch are needed to reduce the package size by half, from the existing 14mmx14mm size to 10mmx10mm size. The assembly details of PoP were presented and the results showed that the μ PILR PoP assembly is approximately 100%, whereas conventional PoP assembly showed extensive solder bridging. It was surmised that the SMT yield benefit for the μ PILR

interconnect arose from the enhanced solder wetting of the copper pin combined with the mechanical stand-off that kept the logic package away from the test board during the reflow process.

The drop testing was carried out according to JEDEC specifications. The μ PILR PoP solution showed very good reliability with B_1 life of 73 drops and the characteristic life (η) of 457 drops, which is more than twice the target of 30 drops per the JESD22-B111 standard. The failure mode was test board cracking rather than μ PILR PoP failure. The conventional PoP performed poorly under the same drop test conditions with B_1 life of 0.117 drops and a characteristic life (η) of 53 drops. This implies that the conventional PoP requires underfill to be reliable. There were no failures observed up to 2500 cycles under thermal cycling from -40°C to 125°C.

In conclusion, this study covering design, analysis, assembly and reliability testing show that package miniaturization can continue with advances in 3D packaging and the μ PILR platform offers one technological solution to achieve the packaging miniaturization, performance and cost goals.

References:

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