

## Multi-components integration in a SIP

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### Abstract

*Components with different nature and forms are more and more integrated in the reduced space of the SIP. To ensure the required operating performances, the management of the positioning of the last components in the package becomes a key step in the design flow. In this paper, some steps of the design, conception and manufacturing process of a SIP are proposed. The choice of the package, the electronic system configuration and the integrated components natures are treated by considering the final environmental constraint of the SIP. The cavity of the package is studied to appreciate perturbations phenomena's that can reduce the SIP performances. Particular cavity comportment is studied in accordance with the positioning of a component. The impact of the presence and location of a QFN package in the environment is analyzed with the support of EM simulations to better understand the SIP implantation step.*

Keywords: SIP, SMD, Package

### I: Introduction

Many domains turn to the use of SIP solutions to achieve sub systems which need more control functions interfaces. Thanks to the upgrade of the operating frequency of electronics devices, SIPs become fast and more appropriate for higher integration level. SIPs combine a large panel of technology [1] providing high quality solutions and offering comfortable control for signal management. For validations, Final test are prove to be more efficient than testing all components one by one before the integration process [2]. However, the integration of several components in a same package constitutes a delicate operation for high frequency applications.

In this paper, we propose the main steps and considerations for the package design of the System In Package (SIP). A SIP for phase shift and output level controls with level detector in X band applications is developed and used to illustrate our approach. It's typically used to drive signal for Electro-Optical-Modulators. Its design is performed considering the multi-component integration in a package. First we describe the system block diagram, and then the packaging is introduced by considering its physical parameters, such as package to chip transition design and components positioning inside the package. Several design examples and results are finally provided.

### II: System design and validation

To ease the SIP control, DC regulator and voltage level convertor using 'Silicon' technology are implemented in the system. The microwave components implemented come from GaAs technology using different processes. The system configuration was, in a first time, validated by cascading the components demo boards. Components have been placed to optimize the overall linearity operation and the phase distortion during the output level control. The major contributor of the phase distortion has been identified to be the last amplifier stage of the system when it reaches its compression operation. Furthermore, an output interface combined with the natural filtering response of the output amplifier attenuates typically the second and third harmonics down to -40dBc.

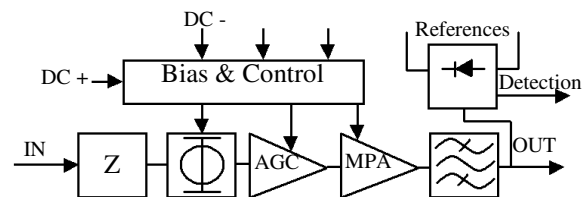


Fig.1: Block diagram of the SIP

We have analyzed the performances of each function one by one and we selected the components which could meet the system specifications. Finally, we selected 60 components to be integrated in the SIP.

Customer constraint oriented us to the choice of a 16mmX16mm SMD package.

### III: Package technology definition

The SIP package was designed to be Surface Mount Device. It consists in reporting components like chips, transmission lines,..., on a carrier which is a metalized dielectric substrate allowing input and output connections by via transitions. To complete the package, metallic belt and cover must be reported by soldering. System environment constraint imposes the use of a partial metallic package. This way, the SIP is providing a shielding from perturbations. The carrier also must offer "good" thermal dissipation properties in order to support the fabrication process. Ceramics are highly used for package fabrication because their compatibility with a lot of precise metallization techniques, simplifying multi-components implantations. During operation, the SIP temperature can change because of external environment condition and active devices dissipations. Ceramics provide excellent thermal dielectric constant stability, low losses and are compatible with thick film technology. This is the main reason why we choose ceramic for the carrier. Furthermore, plated copper on thick film Technology can provide additional thermal dissipations capability. The figure 2 presents the schematic of the SMD package.

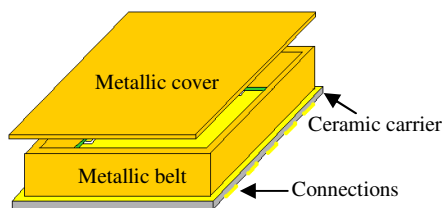


Fig 2: Schematic of the SMD Package

### IV: Important consideration for package design

We see several parameters in which two relevant parameters to discuss for the transition design and the location of components in the package.

#### IV.I: Transition design

The RF performances of a SIP are significantly depending on the type of the package. For high frequency applications, input and output connections of the package constitute key components. We are considering the use of SMD package for upper frequency range applications (Ku, Ka). We decided to focus our design effort on via transition in order to improve the microwave performances of this package. For more than 10 years, some studies have

demonstrated that to improve package performances, the transition topology must provide low insertion losses ( $IL < \sim 0,075\text{dB/GHz}$ ) and low return losses ( $RL < -10\text{dB}$ ). In 2004, one study has demonstrated that back to back structure using via transition could greatly work from DC to 50GHz [3]. Then, in 2006 other study demonstrated some via transitions working from DC to 70GHz [4]. In our cases, we target these results for frequency from DC to 20GHz. The study using a 3D commercial EM simulator based on the finite element method has been done by considering three models configurations:

- I: The first model is a standard back to back microstrip transition.
- II: The second model is a reflective model of a hermetic shielded package transition.
- III: The third model is the back to back configuration of the second model.

Each model contains a metallic platform and an auxiliary substrate. Coaxial ports are modeled to be sure that the structure is excited by a transverse electromagnetic mode. The first model (fig. 3) is a technology reference which can be use to evaluate performances of the via transition. The figure 3 describes the model and presents a photograph of the back to back structure.

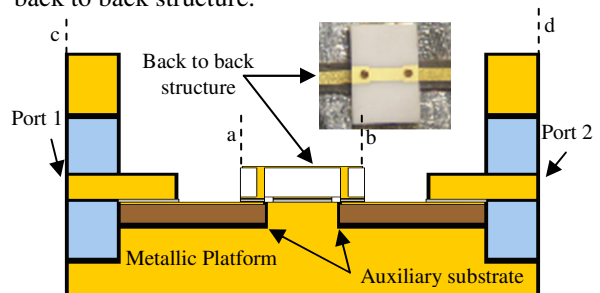


Fig 3: Schematic of the back to back structure

The back to back structure has been designed to have substrate thickness of  $380\mu\text{m}$ , via diameter of  $200\mu\text{m}$ , line width of  $250\mu\text{m}$ . The construction of the back to back structure was fabricated on thin film technology using an alumina substrate. The auxiliary substrate is a Duroïd 5880 with a thickness of  $128\mu\text{m}$  and a line width of  $380\mu\text{m}$ . Reference planes for measurement and simulation of each structures are respectively indicated by a,b (measurement) & c,d (simulation) axes on figures 3, 6, 8. The figure 4 presents a comparison between simulated and measured S parameters.

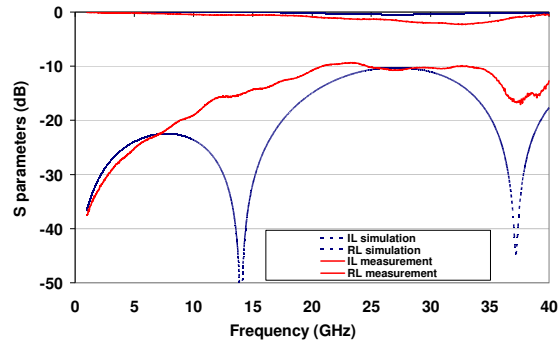
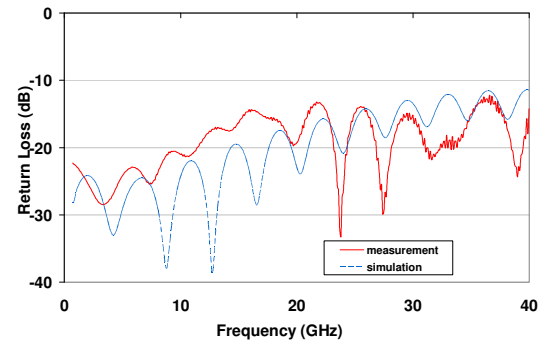


Fig 4: S parameters of the back to back configuration.

Due to the small size of the structure, a Transmission Reflexion Matching calibration has been done on plane a & b in order to simplify the measurement. Considering the different reference planes for structure and model, we observe a good similarity between each results. The maximum insertion losses are  $\sim 2.3$  dB at 33 GHz and the maximum return losses are  $\sim -9$  dB at 22 GHz. This kind of via transition could be considered for high frequency applications. However, we observe that the back to back configuration offers a partial estimation of transitions for SMD package. Note that, some parameters like the ground plane between input and output, the gap at the end of the transition and the metallic area used to fix the belt, are not considered. We decided to configure a new package transition taking into account the connection between the end of the transition and some component reported inside the package. The second and the third models are complementary. They are used to consider package elements like “the finite top pad dimension”, the ground plane area on the carrier surface, the bonding wires connection between the end of the conventional transition and a resistive load.

The methodology consists in using the second model (fig.6) as initial hint for third model. The second model only simulates the reflection losses parameters and therefore uses reduced simulation resources and design process time. When the second model reaches good simulation result, we can use the third model (Fig.8) which confirms insertion losses by doing mirror operation of the reflective model, and replacing the resistive load element by a microstrip transmission line model with a characteristic impedance  $Z_0 = 50 \Omega$ . The resistive load model has been designed to achieve maximum return losses  $< -10$  dB from DC to 40 GHz. The next figure (fig. 5) presents return losses results of simulation and typical measurement of the  $50 \Omega$  resistive load.

Fig 5: Comparison between the measured and simulated  $50 \Omega$  load return losses.

Measuring the  $50 \Omega$  load element imposes us an important length of coaxial transmission line which is not considered in the calibration and may explain ripple in the band. The Figure 5 demonstrates that the measured return losses are matching the simulated result providing performances better than 13 dB at 40 GHz. The second model described in fig 6 is interesting because all the interconnections are taken into account from the input coaxial port to a  $50 \Omega$  load which represents a  $50 \Omega$  matching input of a standard MMIC.

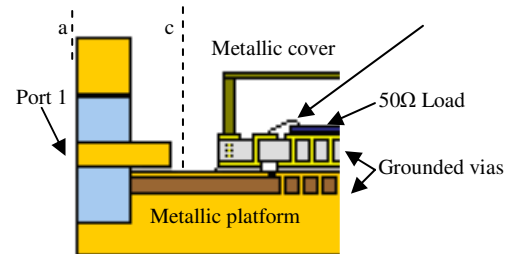


Fig 6: Description of the reflective configuration

The length of the metallic area is  $500 \mu\text{m}$  to allow soldering of a  $300 \mu\text{m}$  metallic wall for covering the package. Three parallel bonding wires connect the top pad to the load to reduce serial inductance of the connection. The figure 7 presents return losses results of simulation and measurement of the structure.

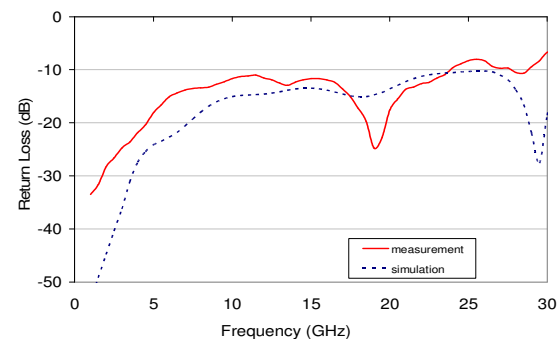


Fig 7: Comparison between the measured and simulated return loss of the reflective configuration.

The measured results are matching the simulated results providing maximum return losses better than 10dB at 23GHz. A capacitive perturbation at high frequency is influenced by the presence of the metallic area. This perturbation could be the origin of the return losses growing after 27GHz [5]. The third model described in figure 8 is the back to back configuration of the second model.

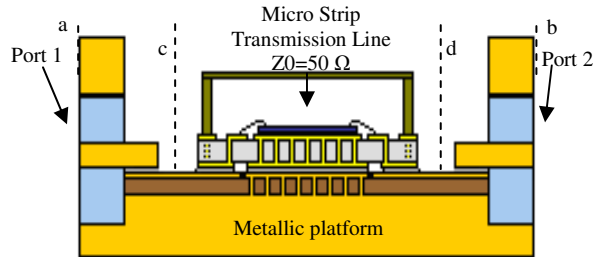


Fig 8: Description of the transmission configuration

The microstrip transmission line is a duroïd 5880 substrate with a thickness of 127μm and line width of 380μm. The figure 9 presents the S parameters of the transmission configuration.

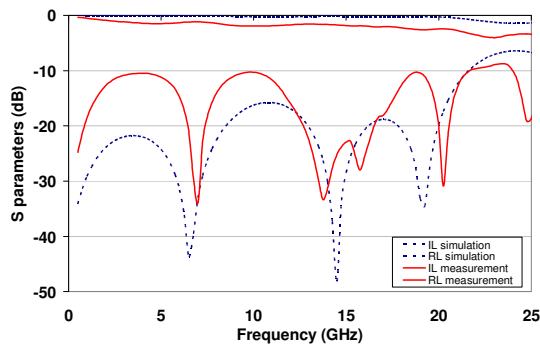


Fig 9: S parameters of the transmission configuration.

The measured results include the losses of the line and the coaxial transmission which are not considered in the calibration. At 20GHz, return losses are better than 10dB and the insertion losses are 2.5dB. From this result, we conclude that this method for transition development is greatly usable for SIP design. To conclude on this part, all this models allows us to understand that finally a package input is a succession of wave-guides. The key element to achieve small reflective losses is the transitions matching between each wave-guide. We have determined that our design method requires a succession of four wave-guide transitions which are described on figure 10:

- coaxial to microstrip transition (1)
- microstrip to stripline transition (2)
- stripline to via transition (3)
- via transition to bonding wire (4)

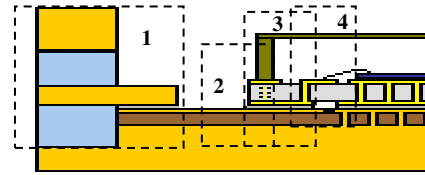


Fig 10: succession of wave-guide transitions

To simplify the analysis, the coaxial to microstrip transition has been modeled by considering 50 Ω of characteristic impedance. During the study, we observed that the matching of the structure was better when the width of the line in the stripline guide had a small size. Considering the dimension of the gap between this line and the lateral ground plane, two different cases of matching can be demonstrated:

- The first case of matching takes part when the ground plane is far from the line.
  - The second matching takes part when the gap between the line and the ground plane has a dimension equivalent to the width of the line.
- These two guides could be approximated to a microstrip wave-guide in the first case and to a coplanar wave-guide in the second case. In both cases, the characteristic impedance of the wave-guide should be close to 80 Ω to limit the return loss.

#### IV.II: Location of components in the package

It is necessary to introduce in the SIP integration a key component of the microwave structure which is a “Quad Flat No lead” packaged device. Using a QFN package component in a SIP production process simplifies the control method of the function, before integrating the component in the final package. However, this introduces a new consideration of the interconnection option between the QFN package and the other unpackaged components in the SIP. To minimize the connections losses and the perturbation risks, we decide to report the QFN on a thick film ceramic using a standard soldering process. This ceramic called “mother board”, which support other components likes DIEs, SMDs, and thick film resistors is then reported on the carrier. In order to improve thermal dissipation, other components like amplifier with Automated Gain Control (AGC) function and Middle Power Amplifier (MPA) are integrated in die form and are directly reported on the carrier ground plane. Three MMIC amplifiers are chip to chip interconnected and placed very close from each other. For high gain configuration, the stability of the system becomes sensitive to the output matching. To solve this problem, a lumped impedance matching is made at the package output to

decrease return losses at the end of the Microwave structure. The stability of the SIP is a crucial parameter and we need to know if the package operations of a QFN component influence the performance of the SIP.

The goal of this study was to place the QFN packaged device at the optimum position in the metallic package cavity in order not to disturb the SIP performances in the frequency range application. To achieve that, we consider the influence of the unloaded and loaded package cavity on the  $TM_{101}$  mode of the cavity which is the nearest mode in our SIP frequency bandwidth.

### V: Theory approach for component integration in the package

The package dimensions define a closed volume which can be considered as a cavity. Due to the presence of transmission line in the cavity, some modes could be excited. When the cavity is unloaded by components, quality factor and resonance frequency are defined by its physical dimensions. However, when the package is loaded by components, it is almost impossible to estimate the cavity modes parameters without EM simulation support. The presence of components in the package is reducing free space and is modifying the cavity functioning. Some configurations of loaded cavity can disturb the system operation. Considering the unloaded cavity, we determined the quality factor (Q) and the resonant frequency ( $F_{101}$ ) of the  $TM_{101}$  mode for an air filled cavity using respectively equations 1, 2 and 3 [6].

$$\text{Eq.1} \quad Q = \frac{1}{\delta} \times \frac{\frac{n^2}{a^2} + \frac{p^2}{l^2}}{\frac{n^2}{a^2} \left( \frac{2}{a} + \frac{1}{b} \right) + \frac{p^2}{l^2} \left( \frac{2}{l} + \frac{1}{b} \right)}$$

$$\text{Eq.2} \quad \delta = \sqrt{\left( \frac{1}{\pi \times F \times \mu \times \sigma} \right)}$$

$$\text{Eq.3} \quad F_{n,m,p} = \frac{C}{2 \times \pi} \times \sqrt{\left( \left( \frac{n \pi}{a} \right)^2 + \left( \frac{m \pi}{b} \right)^2 + \left( \frac{p \pi}{l} \right)^2 \right)}$$

Considering that ' $\delta$ ' is the skin depth, ' $\mu$ ' the magnetic permittivity and ' $\sigma$ ' is the electrical conductivity. ' $C$ ' is the light speed.

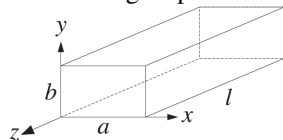


Fig 11: cavity parameters

For  $a = l = 15\text{mm}$ , and  $b = 2\text{mm}$ , we found  $Q=2507444.5$  and  $F_{101}=14.14\text{GHz}$ . This frequency is out of the X band (8GHz-12GHz) which is our first

application domain consideration. We used EM simulations support to simulate the model of the cavity including a transmission line to link input and output connections.  $TM_{101}$  peak perturbation was observed at 14.1GHz. Considering the last model, we added a rectangular dielectric structure to approach the functioning of the cavity loaded by a component with the same dimension as the QFN package (4mmX4mmX1mm). Then we moved the X and Z positioning of this model inside the cavity. The figure 12 describes the cavity configuration.

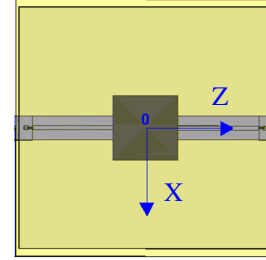


Fig 12: cavity configuration when  $dX=dZ=0$

The figure 13 presents the values of the  $F_{101}$  in accordance with the X and Z coordinates of the center of the rectangular model in the cavity.

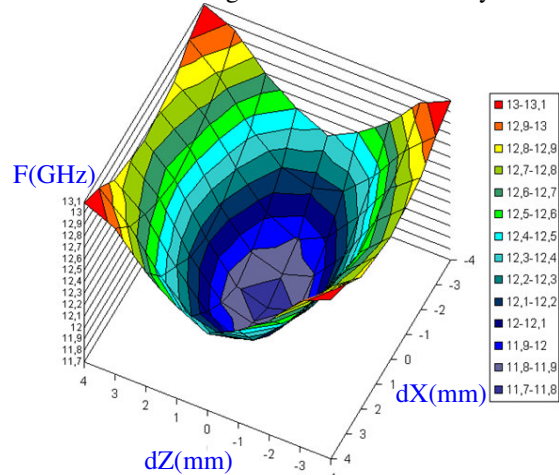


Fig 13:  $F_{101}=F(dZ \text{ and } dX)$

The value of the  $F_{101}$  moved from 11.7GHz to 13.1GHz, the minimum value of the  $F_{101}$  is achieved when the component is placed at the center of the cavity. In this case, the rectangular dielectric model of the QFN is highly coupled to the  $TM_{101}$  mode of the cavity decreasing Q. We observed that for  $dZ=0\text{mm}$  and  $dX < 2\text{mm}$ , the variation of the frequency  $F_{101}$  is not linear. In this case, the rectangular model is placed near the transmission line, which is influencing a high coupling between the two models resulting in a dielectric variation of the moving model. When  $dX$  and  $dZ > 2\text{mm}$ , the coupling between the two elements is low and the variation of the frequency  $F_{101}$  increases linearly

according to  $d$  extension. The figure 14 presents  $Q$  variations in accordance with  $d$  extension.

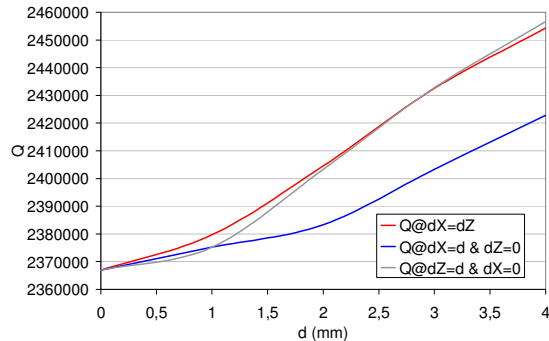


Fig 14:  $Q=F(d)$  for  $dX=dZ=d$ ;  $dX=d$  &  $dZ=0$ ;  $dZ=d$  &  $dY=0$

Introducing a component in the cavity modifies the cavity functioning. Everything looks like if the insertion of a dielectric model in the cavity increases the cavity dimensions. In accordance with the  $dX$  and  $dZ$  variations of the dielectric model, the  $a$  and  $l$  dimensions (fig.11) of the cavity can be reconsidered. The quality factor of the cavity  $Q$  as well as the frequency resonance  $F_{101}$  will be modified. From these results, we deduced that placing the QFN component near the package metallic belt increase the potential frequency resonance of the  $TM_{101}$  mode out of the SIP frequency range operation.

To conclude on this part, placing components in a metallic package are loading the cavity of the package and influencing some cavity modes parameters. We have demonstrated that considering positioning of components could be decisive for SIP validation. The integration of packaged components with proportions  $> 1/30$  of the cavity volume could influence the  $TM_{101}$  frequency mode. In accordance with the increase of the average dielectric constant of the packaged component, the frequencies of the  $TM_{101}$  decrease. It has been observed that this frequency is also dependent of the positioning of the component in the package.

## VI: Conclusion

A new model of transition for SIP has been defined. The proposed model is based on a reflective configuration. Good correlations have been demonstrated between the measurements and the obtained simulation results.

The simulation results of our study demonstrated that positioning an high volume components near the wall of the cavity helps to control the influence of the component implantation on the mutual coupling through the  $TM_{101}$  mode.

Reflective configuration model for transition design and location components in the package are new considerations, which greatly contributed for future implantation improvement. We are currently working on higher frequency SIP and planning to present the SMD package results for 40GHz applications.

## References:

- [1] System-in-Package, a combination of challenges and solutions, P. Cauvet, S. Bernard and M. Renovell. 12th IEEE European Test Symposium, 2007.
- [2] SiP-Test: Predicting Delivery Quality, Alex Biewenga, Frans de Jong, NXP Semiconductors, Eindhoven, The Netherlands, 2007, International test conference.
- [3] High performances of shielded LTCC vertical transitions from DC up to 50 GHz, Rosine Valois, Dominique Baillargeat, Member, IEEE, Serge Verdeyme, Member, IEEE, Markku Lathi, and Tuomo Jaakola, IEEE transactions on microwave theory and techniques, vol 53, n°6, June 2005.
- [4] Ultra-Wideband Shielded Vertical Via Transitions from DC up to the V-Band, T. Kangasvieri, J. Halme, J. Vahakangas, and M. Lahti, 1st European microwave circuit conference. P2, fig.3.
- [5] 50GHz Broadband SMT Package for Microwave Applications, Katsuyuki YOSHIDA, Takayuki SHIRASAKI, Seigo MATSUZONO, Chihiro MAKIHARA, 2001, Electronic Components and Technology Conference
- [6] Electromagnetic Waves and Antennas, Sophocles j.Orfanidis, 2008.