

# Challenges of Supporting 3D IC and 3D Package Integration in the Design Space

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## Abstract

*The continued push for maximum functional and physical density in the smallest volume for the lowest cost has designers leveraging state-of-the-art 3D IC and 3D package integration schemes. In the last two years designers and manufacturers have seen a number of new integration technologies become viable -- TSV, Face-to-Face, and traditional wire bond die stacking in the IC space; PoP, PiP and TMV (through-mold-via) in the packaging space. Likewise, the boundaries between IC and package have started to blur, such that silicon itself has become a substrate material and an additional mechanism for 3D IC integration.*

*Design tools that have traditionally fallen into tidy domains of IC, Package, and Printed Circuit Board are not only being asked to support integration within their domains, but integration and co-design across domains. This paper will outline the challenges and progress that package and PCB tools have had in moving from representing flat, layer based designs in one domain to being able to describe and support the complicated design hierarchy and 3D integration across multiple domains. We will also examine what capabilities designers will need in the future. Designers need to capture and maintain the partitioning and connectivity of the system, as well as being able to represent the manufacturing capabilities now available in the virtual design space. Likewise, the tools must not only be able to represent the 3D integration, but be able to export that design intent to analysis and complimentary design tools.*

## I. Introduction

### *A Brief History: Supporting the 3D Integration in the Design Space*

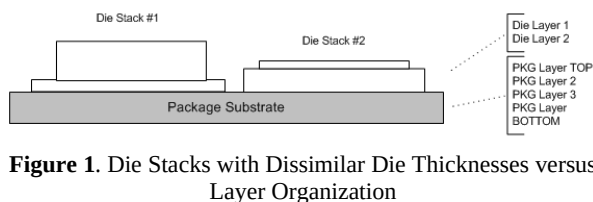
Over the years we have seen a progression in package design. When a package design tool was first required, designs were typically one-die mated with one-package, or they looked very much like tiny PCBs with a handful of different components, including the die. The most common attachment mechanism was wire bond-- welding tiny wires from the perimeter dielectric openings of the die to the substrate on which the die was attached. As die became larger, and grew in their power requirements and number of I/O, a new attachment style (C4 or flip chip) was implemented which used "bumps" or tiny solder balls to attach the die face down to the package substrate. Perimeter I/O signals could be connected to the package, as well as placing bumps in the interior area of the IC design to provide direct access of power to the core cells.

It was predicted that flip-chip would soon eclipse wire bond as the primary attachment and connectivity mechanism in mainstream packaging. However the manufacturing engineers were able to take the first step in 3D IC integration and stack die in what would be called a SiP (system in package). Die were mounted on top of each other, in some cases, with spacers placed in between. The bottom die in the stack could be flip-chip or wire bond, and then the successive dies placed on top of the first die were typically wire bond. There was now resurgence in wire bond manufacturing technology as die were thinned and stacked to create these integrated modules. SiP also provided flexibility in enabling designers to pull together die of different function, technology and materials into one system, rather than trying to represent and manufacture it into one large piece of silicon. Die still, however, only had connections on one side, and the only way to provide direct die to die connections was by placing die face-to-face, typically with a pairing that had one die larger than the other, with the larger die providing access for connections to the substrate. TSV (Through-Silicon-Vias), a process of creating a connection from the active side of the die to the

back side of the die, finally enabled die to be stacked and to have direct connections to other die.

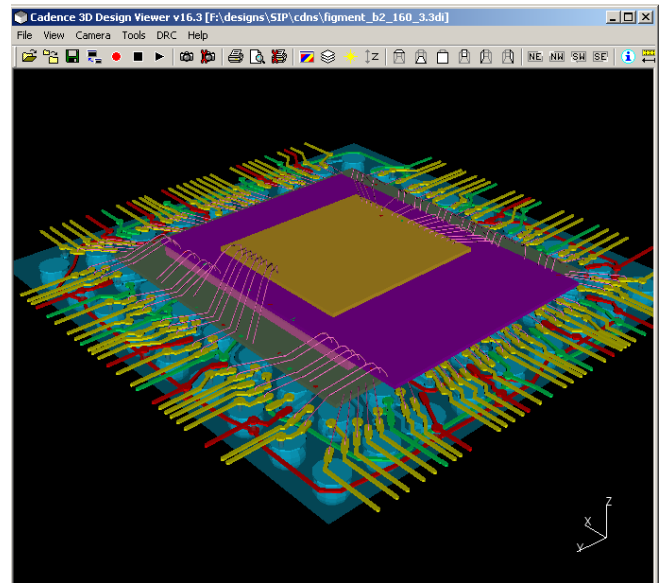
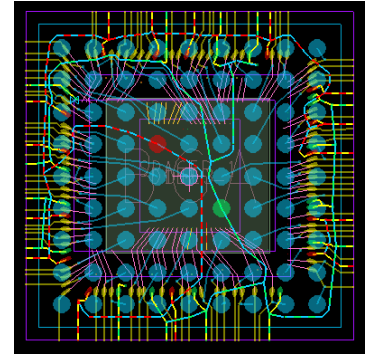
The original PCB design tool was sheets (layers) of translucent vellum (plastic) and colored pencils. When the capability was re-created in software, the PCB tools were also layer-based. This architecture has worked well for decades. Even when adapted to IC package design (adding die objects and wire objects on top or on the bottom of a substrate) the layer-based architecture could support these design entities because they could be abstracted into 2D layer-based objects and meet the requirements of the designer. One might compare this transition with that seen in the field of animation – frame-by-frame hand-drawn animation transitioning to computer generated animation, with a similar emphasis on 3D rendering and more visual content.

This layer-based architecture works fine until you start to create multiple stacks of die in a design; the homogeneous layers cannot fully represent dissimilar stacks of die with different die thicknesses. How can one layer of one thickness in a design “stack-up” represent two dies in two different stacks with two different thicknesses at the same die position? (see Figure 1)



**Figure 1.** Die Stacks with Dissimilar Die Thicknesses versus Layer Organization

Likewise, the process of stacking, in general, drives wire bond patterns and interference issues that cannot be checked and resolved in a two-dimensional design space – using accurate wire curvatures, and matching the curvature of the bonds generated by the wirebond tool, must be leveraged to determine if a design is even manufacturable on the bonder. This cannot be accomplished in a 2D top-down view:



**Figure 2:** 2D versus 3D design view

In Package 3D integration (most notably, PoP (package-on-package) PiP (package in package), and TMV (thru-mold via), this integration drives the design tools to not only maintain one “design” in the database, but at least an abstract of a second or third, quite possibly the entire system, included with the first. A similar methodology is now required in the IC design space; with the manufacturing capability to create TSVs (Through Silicon Vias), the design tools must also be able to support multiple die databases, or at least abstracts of them, to coordinate the placement and assignment of TSV bumps.

## II Requirements of Design Tools to support 3D integration

### Connectivity Management

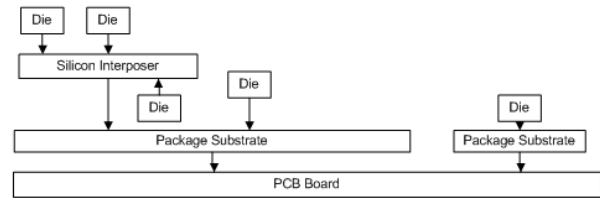
Designers need system level organization and management of connectivity. Integration implies complexity; designs

now include multiple units of integrated circuits, discrete components, parameterized components, and package substrates and a PCB connected together into a system, not by single or small groups of connections, but by high-element count groups of connections (possibly thousands). The designer needs to manage this complex connectivity, often with dissimilar net names on the individual components that must be connected and mapped together in the overall system. A schematic may work in such a design, or a portion of the design, where component counts are high and pin counts are low, but due to the size of signal buses and the breadth of connections between components, it may not be the best mechanism. Likewise, managing a design that encompasses all three design domains, often times with signals that have net names and pin names in each of the three design spaces that are all different, but all need to be connected together, is not a task best suited for a schematic. A table-based approach to capturing connectivity is more straight-forward in this example.

#### Co-design, System Planning

The system will likely include fixed, off-the-shelf components, but more importantly include die, packages, and substrates (both PCB and interposers) that are subject to design changes within the context of other components. Being able to make assignment and placement changes at all levels of the design hierarchy to resolve physical conflicts and meet signal integrity constraints is mandatory at this level of integration. There must be an ability to make changes in one domain that ease issues in another, or more likely, find the best possible combination that eases issues in both.

Most, if not all tools in the IC, PCB and package design space were initially created and architected to design a single IC, board, or package at one time. With the increase in activity in 3D IC and 3D package integration, designers now need tools that enable design of that integration within the domain, as well as co-design with other domains. An IC tool not only needs to plan the placement and routing of a single IC, but now needs to address the planning and placement of TSVs within the current die as well as a stack of die. In the packaging space, tools must now account for PoP and PiP technologies, as well as co-designing the package with the IC, the PCB, or both. The complexity of these devices demands that the tool architecture facilitate the design of one with respect to another.



**Figure 3:** Example of a Hierarchical System Design

#### 3D Organization and Hierarchy

There is now substantial encouragement in the overall EDA design arena to move from discrete design domains (IC, Package, PCB) and provide a common design environment that addresses all of them, both in initial system planning (where abstracts of different components are sufficient, and design planning and partitioning is done), to final implementation, where detailed representations of each level of hierarchy can be viewed and analyzed. An environment is desired where the system can be viewed and managed at various levels of abstraction, or at least coordinates and merges different canvases together. The user will want to act upon multiple databases in the same design space, as well as databases in dissimilar spaces.

One may argue that a single, common database across all the design spaces is needed, but that may not be the case. It is very likely that there are system designers within an organization who have a broad understanding of IC, package, and PCB domains to envision and partition a design at a high level of abstraction. It is not likely, however, that there will be one designer that has a high level of expertise in all three, or even two. It is more likely that the system will be managed and designed by a team, and will need a design environment that allows a team of designers in each respective expertise to negotiate over the interfaces and close on the final design.

#### RDL and Interposer

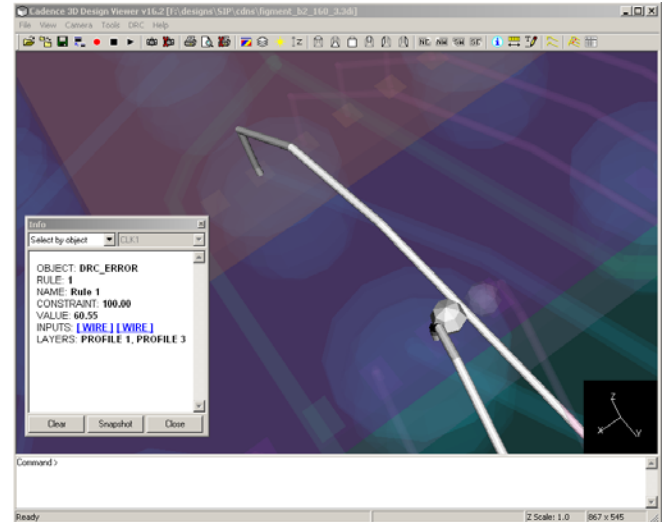
Another mechanism for 3D integration that is seeing increased popularity but poses some interesting challenges for designers is the use of silicon interposers. A section of silicon wafer is used as a substrate for single or multiple integrated circuits. It may provide a single layer of routing to redistribute IC connections to bumps, or it may include TSV, multiple routing layers on both sides, discrete components, parameterized components, and possible active regions as part of its manufacturing. RDL (Redistribution Layer) routing (i.e. routing on the last layer or layers of metal on an IC) can convert a wire bond die to a flip chip die (by routing the perimeter I/O connects to a flip chip bump matrix on the die), can make a single die a CSP (chip-scale-package), again, by routing from the I/O outputs to the

bump locations staying within the die outline, and can be the physical manifestation of co-design (sorting the IC output pins to bump assignments using the last RDL layers, staying within the die outline). Silicon interposers provide a mechanically stable platform for integration (because the “substrate” and die have the same mechanical expansion rates), and can typically be manufactured with older design rules in fabs used for older process nodes.

The challenge for the designer is that the interposers can now be manufactured by a variety of methods, and may follow “pure” IC design rules (fixed line width and via size per layer, orthogonal or 45 degree routing, metal striping, etc), or classic PCB/IC Packaging design rules (circular vias, variable line width and via size, any-angle routes, full-metal fills), and quite possibly a little of both. Based on the manufacturing technology leveraged for the design, a number of different design tools (from different domains) might be the “correct” design tool to design and implement an interposer --- it may fall in IC or package. The only real requirement is that the designer gets to an artwork format (e.g. GDSII) that can be used to generate the mask.

### 3D Viewing and Design Rule Checks (DRCs)

The 3D integration of ICs as well as substrates requires that not only does the designer have to run DRCs within each portion of the design, but between portions of the design, both physically and electrically. With the ability to accurately represent the curvature of the design bond wires and the emphasis on dense stacking, the designer must be able to represent and examine the design as it exists in 3D space, and look for spacing and assembly violations in the same space. The designer must also insure once the final system is assembled, there are no physical interferences and no signal issues due to the proximity of other components, traces or substrates. No longer can an EDA designer lay out a complex SiP wire bond design with 2D “rules of thumb” given to him or her by the wire bond manufacturing engineer. Density requirements mandate that the EDA designer use accurate representations of the wires in design, and use curvatures that the manufacturing engineer can match in production. Likewise, once the design is set, the system designer can use the accurate curvatures in any subsequent spatial or SI analysis on the design.



**Figure 4:** a 3D DRC has been run on a stacked die design wire bond pattern. The faceted sphere “marker” indicates that two wires have a 3D spacing violation between them.

### Electrical, Thermal, and Signal Integrity (SI) Analysis

Obviously, there is the necessity of extracting and modeling the critical nets and power distribution in a system that may cover multiple design domains, each with geometries that vary by one or two orders of magnitude in size from domain to domain. Any tools in this space must allow the user to examine the interaction between nets in the same domain. However, due to the spatial compression of the design, and close physical proximity of other design elements, we must also examine the interaction between structures in the design (two die placed face-to-face, as an example).

Based on the order and placement of the 3D IC or 3D package integration, power may have to channel through one component of the overall structure to feed another. Any simulation and modeling of overall power distribution and quality must look at the entire structure and account for the upstream components.

Each EDA design tier (IC, Package and PCB) has their own specific analysis tools, optimized for the scale of the design geometries as well as the speeds that the signals are travelling. Whereas it is unlikely that one single tool could be used to extract a signal path that passes through IC, package, and board, the tool set should be able to parse the path into its respective areas, use the appropriate tools to extract, and build a single extract topology that models the entire path accurately.

### Additional Analysis, Design Export

It is unlikely that a user will work in a single design environment that addresses each and every aspect of bringing a design to fruition: Thermal expansion and heat

dissipation, sudden g-force and harsh environment simulation, mechanical stress and assembly interference analysis, wire deformation due to molding compound injection, power distribution and integrity are a few of the design aspects that must be analyzed. A mechanism must be in place to enable additional tools outside of the EDA space to extract the required information and analyze the design at all its different levels of hierarchy.

### III Summary

Recent years have seen a rapid acceleration in leveraging 3D IC and package integration manufacturing technologies to meet the size, cost, functional, and performance requirements of consumers. IC and package design EDA tools will need to leverage existing co-design and layout capabilities, as well enhance their 3D capabilities to meet these challenges.