

Monte Carlo Simulation of Void Concentrations in Surface Mounted Solder Joints

Jacob C. Burke, John W. Evans and Kamili Jackson

NASA Goddard Space Flight Center

Greenbelt, MD 20771

301-286 9236

jacob.c.burke@nasa.gov

Abstract

At certain concentrations, voids inside soldering joints can decrease the reliability and the life of the joint. This study employed Monte Carlo simulation to study the distribution of void concentrations in critical areas of passive chip components. Results show that destructive concentrations of voids occur in critical areas of the joint with increasing probability, as the process produces voids in excess of 10%.

Introduction

Changes in material sets to achieve goals for reduced emissions and to reduce environmental impacts to vital resources, continues to foster challenges to assembly processes. Water soluble fluxes, for example, provide for advantages over solvent based fluxes, in control of emissions and treatment of process effluent. However, defect rates tend to increase in joints with lead free alloys and alternative flux chemistries in comparison to conventional materials [7]. Voids in joints are one of these defect types, which have prompted the need for new standards and inspection criteria.

There has been considerably focus in recent years on studying the effect of voids on the service of surface mounted joints employing SnPb alloys and with the emergence of Pb free alloys. Voids are of concern, particularly for Surface Mount Technology (SMT), as joints must perform both structural and electrical functions. Voids may provide a long term hazard due to the potential for reduced fatigue life.

While criteria governing defect definitions and allowable amount of voids for some joint types have emerged in IPC documents [1, 2], the topic remains unresolved for high reliability applications.

In this initial study, the objective was to assess the minimum risk for various levels of void concentrations that emerge from the assembly process. The probabilities of occurrence of a defined defect were determined, using a simulation based upon the expected probability distribution of void sizes and the maximum level of void concentrations. The result is intended to influence decisions about the allowable levels of voiding for high reliability applications.

Macro-Void Formation and Effects of Macro Voiding

It is generally accepted there are several types of voids with distinct causes [3,4]. Macro voids are the most recognizable defect and among the most common type void occurring in

surface mount joints, and are the focus of this initial study. This type void is usually smooth walled and spherical but may range to a 'pancake shape' depending on solder thickness. These types of voids arise during reflow primarily from entrapped volatiles present in the fluxes combined with wetting effects. They are generally detectable by x-ray inspection. The remainder of this paper focuses on macro voids and the term "voiding" hereafter will refer to this type of defect. For a general discussion of other void types and their circumstances of formation and effects, the reader is referred to literature [3,4,6].

Figures 1 and 2 show typical x-ray images of voids in assembled solder joints. Void size and void concentrations can be measured from x-ray images. The sizes of macro voids can vary significantly from about 10 microns up to 200 microns, or more, depending upon the type of joint, pad size and processes [5]. The amount of voiding in a given process is usually measured in terms of percentage of solder pad area and depends heavily on processing and joint geometry.

The control and mitigation of macro void formation depends in large part on the flux constituents wetting and reflow thermal conditions. Poor wetting of surfaces, paste oxidation and increased surface tension are likely to promote macro void formation. Higher temperatures and longer dwell times at preheat and reflow tend to reduce macro voiding [7]. Modeling of void formation has shown thermal gradients also promote voiding and influence undesirable void agglomerations [8].

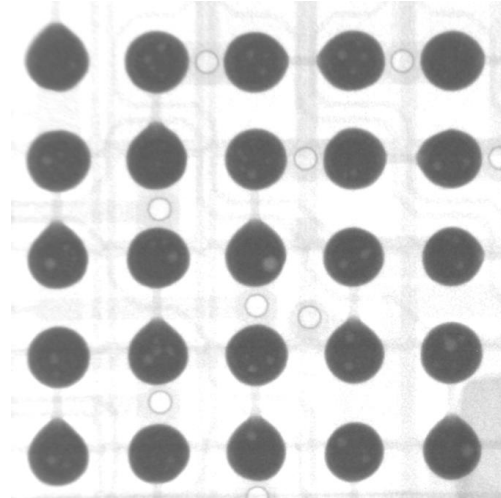


Figure 1. Voids in Ball Grid Array joints. (Courtesy of C. Hunt, NPL)

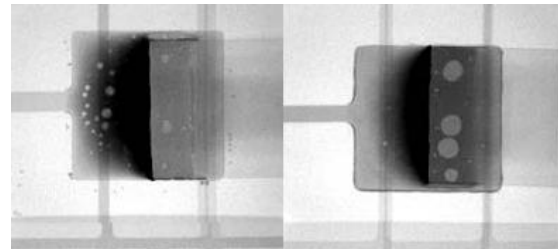


Figure 2. Voids in chip component solder joints. Note the differences in void concentrations beneath the chip terminations (Courtesy of C. Hunt, NPL).

The effects of voids have been studied by modeling and through experimental methods. Voids can expect to reduce fatigue life of surface mount assemblies depending upon the extent of the voiding. The location, size and amount of voiding will determine the effect on fatigue life [9]. Hence, it is of concern to high reliability applications to understand the limits necessary to minimize risk of failure.

Finite element models with fatigue modeling can afford the ability to study individual joints under varying loading conditions. Detailed crack propagation models have shown that defects consisting of void concentrations on the order of 10%-15% will begin to reduce the fatigue life of BGA joint with about 15% life reduction expected for 10% voiding for voids occurring in critical areas [10]. Studies on chip resistor joints have shown a 16% reduction in life for void fractions of 13% [11].

Experimental studies have shown that voiding has no measurable effect on fatigue life up to a maximum of 15% voiding [12]. Others have reported that no measurable effects occur up to 25% voiding. (This is the maximum allowable voiding in IPC-610-D and is the maximum allowable interface defect allowed by IPC-7095 Class 1).

While some of the experimental studies are statistically credible, a potential problem with experimental studies is that it is very difficult to have a sufficient sample size that contains a meaningful number of destructive defects that can statistically affect the sample size variations on fatigue life. The measurable effects of the voids upon the sample population may be difficult to determine in a normal test population since all voids are not contributors

to reliability reduction. Unfortunately, for high reliability applications this makes the assessment of voids and risks difficult. Hence, simulation is an important supplemental technique.

In determining the effects of voiding, the definition of a defect is very important. As emphasized, the location of voids is important. Voids are likely to be relatively benign if they are not located where they contribute to damage. For voids to be problematic they must not only be of a significant concentration, they must also be located as to interact with the strain field developed in the joint; this is the region where cracks initiate and propagate. *Critical areas* are defined in Figure 3 for example ball joints and chip components, typical of SMT joint dimensions.

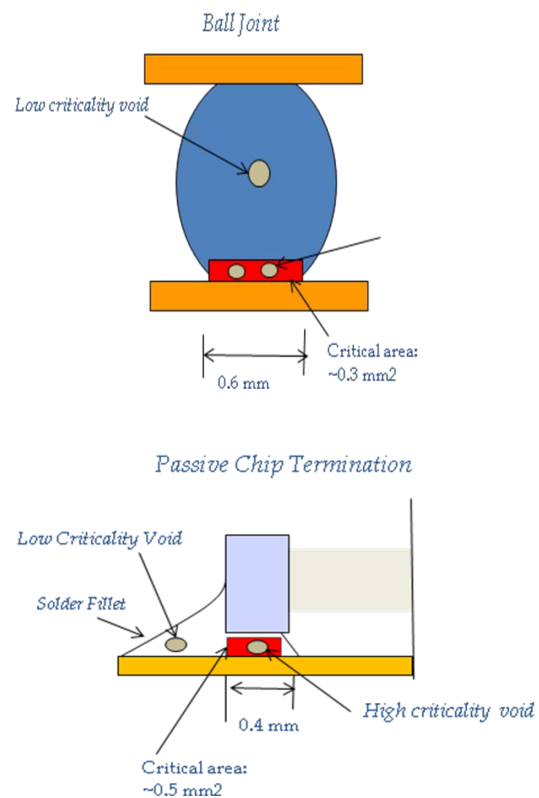


Figure 3. Critical defect regions in SMT solder joints. For chip parts cracks initiate under the chip

terminations defining the critical area to be the portion of the joint under this termination. Cracks in ball joints initiate near the interfaces of the ball and pad defining the critical regions in these locations.

Defect Models

Defect models can be created for different joint types and defect types. These defects can then be studied in relation to their strain concentration, fatigue interactions and frequency of occurrence. In this initial study, a defect was defined for chip components exceeding 25% voiding in the critical region of the joint. This is illustrated in Figure 4 with the shaded area in the critical region representing 25% of the critical region to show proportionally the allowable voided area. Other types of defects can be defined and are currently under study.

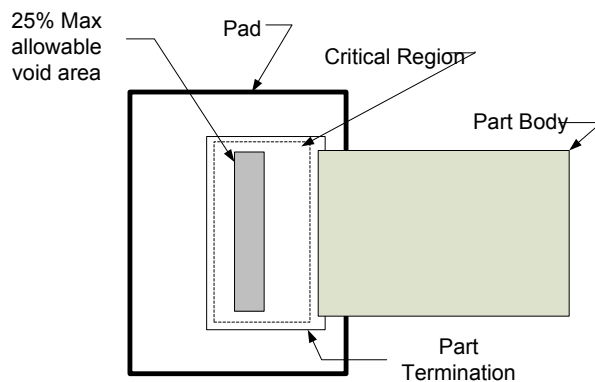


Figure 4. Example of defect definition representing 25% of a critical region under the termination of a chip part. This is the area where cracks initiate. Note the fillet would not be included in the defect definition in this case. The shaded area represents 25% of the critical region for comparative purposes.

Monte Carlo Simulation of Void Defects

Monte Carlo simulation was used to assess the frequency of occurrence of the defined defect. The model simulated the random placement of voids on multiple soldering pads. The process of simulation begins as the first pad is defined. Initially, a void was sampled from a defined void size distribution. By use of a random number generator, the process mandates the assignment of a location on the soldering pad to correspond to the void size. Thus, the first void will have been placed on the pad. These steps are repeated multiple times populating voids within the constraints of the pad up to a defined level, representing a particular process.

Several constraints were placed on the simulation according to observations of x-rays of void populations. No two voids were allowed to intersect. If the combination of the size and location of the void is found to infringe upon the area that a previous void enclosed, the void was discarded and the process of generating the next void proceeded. In addition, no void was allowed to form within 10% of the pad edge and any void partially within the critical region was counted as a contribution to the defective condition. Therefore, its total area was counted.

After a void was found to be free of intersection with all other previously placed voids, the running total of void area and the total void area within the critical region (CR) was incremented. After running the pre-defined number of pads, the totals were calculated along with appropriate statistics and a distribution of void area constituting the defect was estimated. This process of generating voids on pads was repeated until the defined number of pads to be simulated was reached.

The random number generator used in this model was necessary for both the sampling of void size and random placement of voids. The simulation was performed on a macro-enabled spreadsheet which constrained to implementation of the random number generator provided by the “Rnd” function in Visual Basic. This pseudo-random number generator was tested and for all practical purposes, a true set of random numbers was generated and determined to adequate for the purposes of this type study.

The void size distributions measured from actual void observations will fit a log-normal distribution [13]. In Monte Carlo Simulations, the triangular distribution is often implemented for input parameters [14]. It can approximate a skewed distribution, with a simple closed form CDF which can be used to sample for the simulation. In this case, the triangular distribution was used to represent the population of void sizes. The parameters of the distribution used in this study are a result of observations of the occurrence of void sizes and comparisons to other studies in the literature [5, 15]. The constructed input distribution for voids ranged from a minimum in diameter of 20 microns to a maximum of 210 microns, with the mode, or the most likely having a diameter of 46 microns.

Simulation Results

Numerous simulations were executed on typical solder pad sizes with typical surface mount resistor terminations. The occurrence of the defined defect, exceeding 25% void area in the critical zone, was tracked. Finally, various processes in terms of maximum percent voiding were evaluated in terms of the probability of defect occurrence.

A sample histogram of a single simulation output is shown below. This particular simulation was executed for 15,000 pads with 10% maximum voiding (each pad was simulated to contain at least 10% void area).

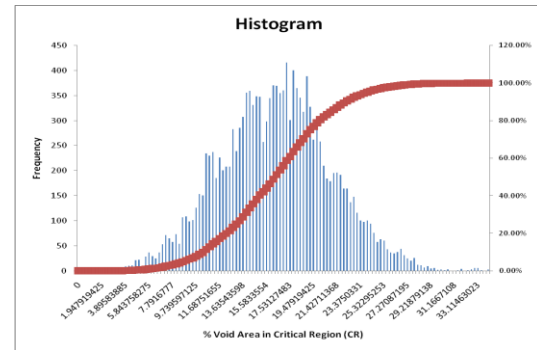


Figure 5. A sample Monte Carlo simulation output for percent void area in the critical zone of a chip capacitor mounted to a Printed Wiring Board on a 1.0 x 1.25 mm pad.

The results of this particular simulation gives a Mean Percent Void Area in the critical region of the joint, under the chip part termination, of $\mu = 16\%$ with the Standard Deviation $\sigma = 4.7\%$. Note that the mean is higher than the maximum void area per pad of 10%. This due to the fact that voids partially located within the region were considered to constitute a part of the defect and their whole area was included in area calculation.

Table 1. Typical Simulation Output for 15,000 pads

Results	Min	Max	Mean	Std. Deviation
# of Voids	6	22	13.06	2.55
# Voids in CR	0	13	5.72	1.82
V Area - CR	0	0.13	0.065	0.018
% Void Area - CR	0	34.02	16.19	4.69

Output data were evaluated according the best fitting distribution. Above 10% the distribution best fits a normal distribution. However, some kurtosis is evident. Below 10% the best fit distribution was lognormal as values of the parameter of interest cannot be less than 0. Based on the distribution we then find the probability of the critical region exceeding the defect criteria of containing greater than 25% voided area. In the case, shown above for 10% voiding, the probability of exceeding the defect criteria is about 2.8%.

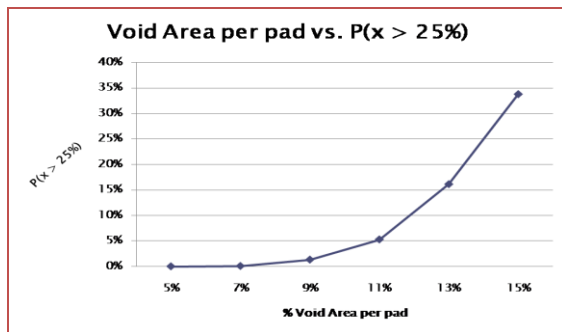


Figure 6. Probability of defect occurrence for increasing voids per pad arising from different processes.

The probability of defect occurrence versus various processes, defined by maximum voids per pad, is shown in Figure 6. This series of simulations utilizes the same input void size distribution described above for a 1.0 X 1.25 mm pad size, with a typical chip resistor.

This result can be used to make inferences about process control versus risk of defect occurrence for this type of joint. Clearly, attempting to control a soldering assembly process to yield voiding below about 10% maximum per pad, has significantly diminishing returns. Above 10-13% maximum voiding per

pad, the risk of forming a detrimental defect rises rapidly.

Conclusions

Monte Carlo simulation was used to evaluate defect occurrence in the form of void accumulations in critical areas of solder joints. Based on a likelihood of occurrence of a defect of 25% or greater void concentration on a typical chip resistor mounting, simulations indicate the *risk is near minimum* at 10% maximum voiding across pads in the assembly process. There are rapidly diminishing returns in trying to control the process below 10%. However, clearly risk of defects rapidly increases above 10-13% maximum voiding across pads. Interestingly, this correlates to results of experimental studies that show no measurable effects of voids on thermal cycling reliability below 10-13% maximum voiding [12].

This study does not support maximum criteria of 25% voiding for this type of joint. In order to avoid what are accepted to be detrimental concentrations of voiding in critical joint areas, the process must be controlled to produce lower concentrations of voiding to reduce the likelihood of defects.

Additional studies of other defect types and joints are planned using Monte Carlo simulation. These types of defects will be related to their potential for propagation under thermal cycling loads.

Acknowledgement

The authors would also like to thank C. Hunt of the NPL for his comments.

References

- [1] IPC-7095
- [2] IPC-610 D
- [3] W. Engelmaier, "Voids in solder joints—Reliability", *Global SMT and Packaging*, 6.1, January, 2006.
- [4] R. Aspidiar, Voids in Solder Joints, SMTA Northwest Chapter Meeting Presentation, September 21, 2005.
- [5] L. Li, Y. Rao, J.K. Lin, "Pb Free Solder Paste Reflow Window Study for Flip Chip Wafer Bumping", *Proc. of International Symposium on Advanced Packaging Materials*, 2001.
- [6] D. Ormerod, Y.H. Yau, J. Wyszchen, Root Cause Analysis and Elimination of Immersion Silver Plating Defects on PWBs Through Process Optimization, *circuitree.com*, Nov. 2006, <http://www.enthone-omi.com/docs/CircuiTreeNov2006ImAgStudy.pdf>.
- [7] P. Biocca, "Lead free defects in reflow soldering", [http://www.emsnow.com/cnt/files/White%20papers/Lead free Reflow Defects %20How to Prevent Them.pdf](http://www.emsnow.com/cnt/files/White%20papers/Lead_free_Reflow_Defects_%20How_to_Prevent_Them.pdf), February 15, 2005.
- [8] R.L. Panton, J.W. Lee, L. Goenka, A. Achari, "Simulation of Void Growth in Molten Solder Bumps", *Journal of Electronic Packaging*, ASME, Vol. 125, September 2003, pp 321-334.
- [9] M. Yunus, K. Srihari, J.M. Pitaressi, A. Primavera, "Effect of voids on reliability of BGA/CSP solder joints", *Microelectronics Reliability*, 43 (2003), pp 2077-2086.
- [10] T. Terasaki, H. Tanie, "Fatigue Propagation, Analysis for Micro Solder Joints with Void", *Proc. International Symposium of Electronic Materials and Packaging*, Dec. 11-14, 2005.
- [11] K. Tagaki, Q. Yu, T. Shubutani, H. Miyauchi, M. Shiratori, Y. Noro, "Study of Thermal Fatigue Life Casued by Dispersion of Solder Joints, IEEE, 2008.
- [12] M. Wickham, M. Dusek, L. Zou, C. Hunt, "Effect of Voiding on Lead- Free Reliability", NPL Report DEPC MPR 033, April 2005.
- [13] H. Leidecker, unpublished work, 2009.
- [14] G. Hazelrigg, *Systems Engineering: An Approach to Information Based Design*, Prentice Hall, 1996.
- [15] C. Shea, R. Raut, L. Picchione. Q. Chu, N. Tokotch, P. Wang, "BGA Solder Void Correlation to Via-in-Pad, Via Fill, Surface Finish and Lead Free Solder-A Preliminary Review, Part Three", *Proc. SMTA*, 2006.