

Silver Epoxy Filled Via Analysis for High Reliability RF MCM Microelectronics

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Abstract

The use of thin film ceramic substrates containing laser drilled and electroplated vias attached to a ground plane with electrically conductive epoxy is a common design approach used for RF MCM's products. This construction technique requires the vias be filled or plugged with an adhesive material to prevent the electrically conductive epoxy from flowing up through the via and onto the top surface of the thin film substrate metallization pattern during the installation of the substrate into the housing.

After completing the assembly of the RF path, the path is "tuned" to optimize output power based on the assembled "as built" configuration. Performance characteristics are tested and reviewed for "in family" results during the processing of high reliability products used in space applications. An indication of degradation in RF performance was identified prior to hermetically sealing the modules during "pre-seal" screening (temperature and mechanical extremes). The data suggested that the output power from the modules was "out of family" by comparison to the expected result.

Utilization of a fishbone diagram resulted in several potential root cause investigations that were launched in parallel to repair the RF power anomaly. The "out of family" conditions were corrected and the degraded ground path root cause was verified. A finite element analysis of the electroplated ground via was developed, mechanical and thermal testing was conducted to repeat the failure mechanism. At the conclusion of the investigation, it was determined the via thin film metallization failed under load caused by the CTE of the silver epoxy used to fill the via. The failure rate was found to exceed the allowable reliability criteria.

An alternate material for via plugging was selected and tested to validate that the manufacturing solution met the product life expectations.

Keywords: Thin Film Ceramic Substrates, Thin Film Vias; Silver Epoxy Filled Vias; RF MCM; Via Cross Section, CTE

Background

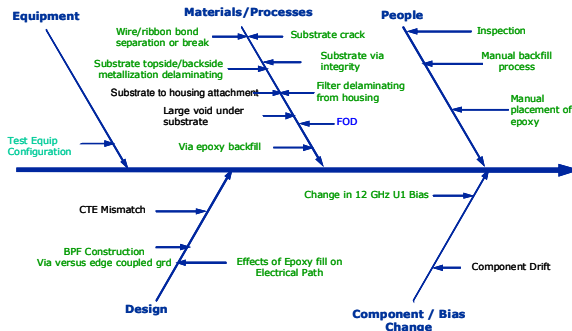
During a review of RF test data, a single channel in an RF Module indicated a drop in power of 1 db which was identified as an "out of family" test result. A redundant and adjacent channel did not exhibit the power degradation observed, verifying that the testing configuration was within specifications. The "out of family" product was exposed to numerous epoxy cure cycles at 125°C and 150°C. In addition, the product experienced 20 temperature cycles from

-55°C to 125°C. Two additional products within the production lot showed similar RF power degradation anomalies on other channels. An investigation into the root cause was initiated that resulted in the generation of the fishbone diagram shown in Figure 1.

A detailed investigation involving comparison of the failed RF path and a "good" RF path identified the potential for a grounding problem. An increase in RF power was

observed when the filter pole ground vias were manually probed with an insulating tip; the filter is shown in Figure 2.

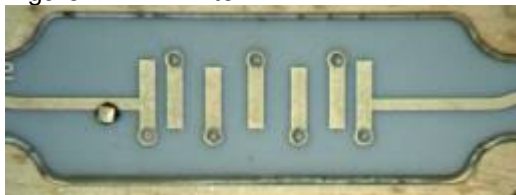
Figure 1. Fishbone Analysis Diagram



This RF power value was similar to data collected from the initial product “turn on”. In addition, this RF power value did not return to previously observed “out of family” output readings. Therefore, the band pass filter (BPF) was identified as the source of reduced RF power in the assembly; photos of the via topside is shown in Figure 3.

To better understand the resistive ground path failure mechanisms as it related to the product manufacturing process, three thin film suppliers were contacted as resources. None of the three suppliers could identify a processing and/or manufacturing step that correlated to the reported failure mode. One supplier suggested the process of filling the vias with silver epoxy had been reported as a problem by a customer, but could not comment on the details of the failure.

Figure 2. BPF Filter



BPF Filter construction

The BPF filter is processed by laser drilling vias through the alumina substrate. Sputtered TiW is then used as a seed layer on the alumina prior to gold plating. The TiW is sputtered using a two step process, one from the topside of the alumina and the second from the bottom side of the alumina, Figure 4.

The BPF filter pattern is etched and the topside of the via is reinforced with a 'catch pad perimeter' to increase the contact of the top metallization to the via walls, Figure 4.

Figure 3. Via filled with Silver Epoxy

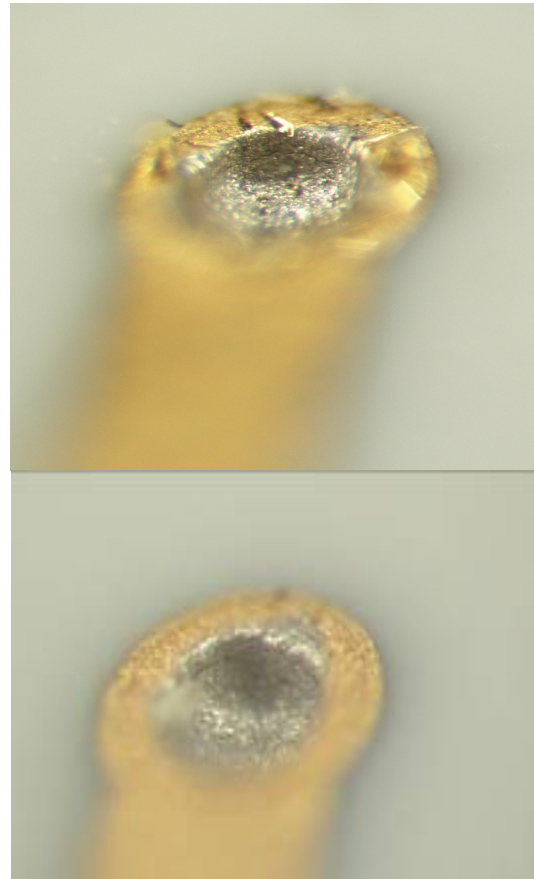
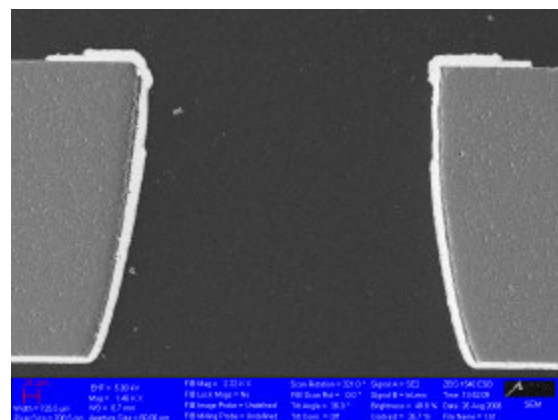


Figure 4. Metallized Via cross section



Mounting in the RF Hybrid

The BPF filter is mounted to the RF Hybrid base using silver epoxy per MIL-STD-883, method 5011. Prior to placing the filter into the hybrid, the via holes are filled with the same silver epoxy used for substrate attach and then cured. This prevents the wet silver epoxy attachment material from squeezing up through the via holes during attachment (scrubbing motion) to the hybrid base. The resulting bond line is approximately 0.003" with the vias partially filled, Figure 6.

Figure 5. Via front and back side views



The BPF filter showing the "out of family" RF power loss was removed from the RF module and cross sectioned, Figures 7 and 8. The via fill exhibited hair line cracks near the top of the epoxy fill. After completing the cross-section, it was evident that the metallization separated from the via wall, Figure 8.

Figure 6. Filled via cross-sections

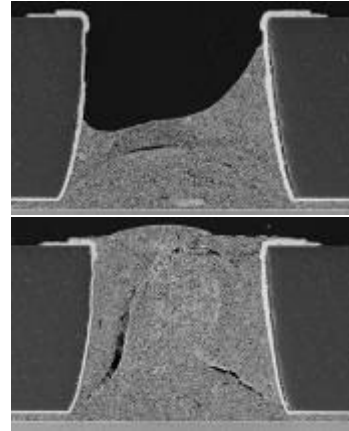
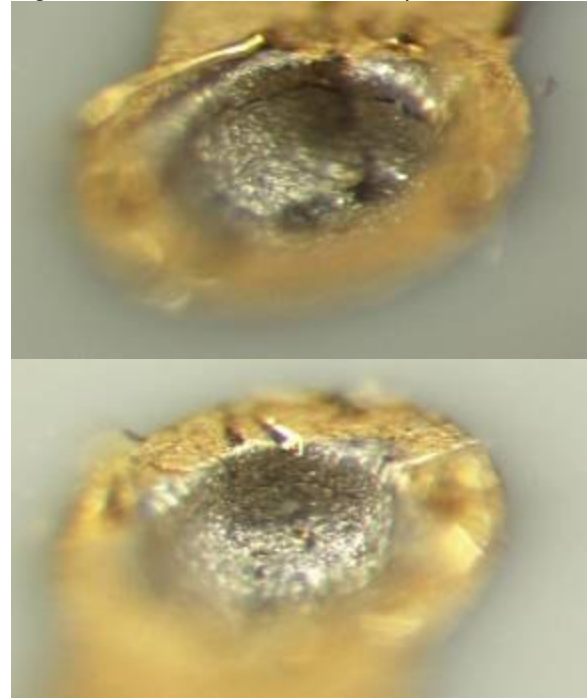


Figure 7. Failed BPF filter vias top side view

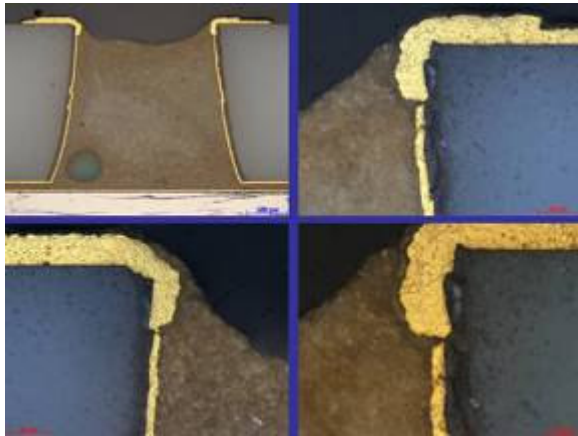


The root cause of the RF power degradation was identified as a crack/separation within the via metallization at the top of the epoxy fill/cure line. FEA modeling was used to determine any reliability risks and to better understand the loading conditions associated with the interaction of the epoxy fill with the via metallization.

Modeling of Via and Fill Material

A Finite Element Model (FEM) of the via (no epoxy), via filled with 50% silver epoxy, and via filled with 100% silver epoxy was created to

Figure 8. Failed BPF filter via cross section



determine if the resulting strain on the gold via metallization could result in the observed failures. The TiW adhesion strength was not analyzed in the model since the gold plating thickness was >1000X thicker than the sputtered TiW. Shown in Figure 9 is a summary of the boundary conditions used for the analysis with the graphical results presented in Figures 10, 11, 12, 13, and 14.

The results of the FEM indicated that a 100% epoxy filled via can produce strains on the gold via metallization that exceed a 1% to 2.5% range. Relatively thin plated gold metallization can crack when thermally induced strains exceed the stated range. The vias that failed were epoxy filled to a value exceeding 75%.

Based on the results of the FEM and inconsistency of the fill for the via plugging process, a search for an alternate “plugging” material with CTE's similar to alumina were investigated. Two materials were identified and the evaluated using supplier recommended processing.

Verification of Failure

Since the FEM is only a single data point and does not provide cumulative defect analysis, test samples with a total of 100 vias (from two suppliers) were subjected to 2X Life testing conditions to establish the failure PPM. The samples were fabricated using the manufacturing method of backfilling the vias with epoxy, curing the via fill at 125C, and mounting the substrate with epoxy onto a housing and curing at 125C. The samples were then subjected to temperature cycling, -55 to 125C,

for 116 cycles and 300C bake for 1 hour to simulate 2X life expectancy. A failed via was defined as a crack or separation of the via wall metallization as observed during cross-section review.

Figure 9. Material Boundaries [1]

Gold stress versus strain data from Mechanical Properties of Structural Films

- For gold plating annealed at 200 °C for 1 hour
 - $F_{tu} \sim 25$ ksi
 - $F_{ty} \sim 22$ ksi
 - Elongation to failure > 2.5%
- For gold plating without annealing
 - Higher strength
 - Elongation to failure > 1%

Figure 10. Boundary Condition [2]

- **Analysis from 125°C to -55°C**
 - 84-1LMI adhesive properties at 25°C were used
 - $\alpha = 55$ ppm/°C (below 103°C)
 - FEM loads, initial conditions, and reference temperatures
 - Body temperature load = -55°C
 - Initial temperature = 125°C
 - Reference temperatures
 - Gold, substrate: 65°C
 - Adhesive, carrier: 125°C
- **Analysis from 65°C to 200°C**
 - 84-1LMI adhesive properties at 25°C were used
 - $\alpha = 150$ ppm/°C (above 103°C)
 - FEM loads, initial conditions, and reference temperatures
 - Body temperature load = 200°C
 - Initial temperature = 65°C
 - Reference temperatures
 - Gold, substrate: 65°C

Figure 11. FEM of Via

- Nonlinear thermoelastic analysis of gold plating without adhesive in the via for temperature range of -55 to 125C
 - Gold plating strain is 0.30% at -55°C
 - Gold plating failure strain is 1% – 2.5% (for no annealing and annealing for 1 hr @ 200°C)
 - Substrate gold plating is annealed for 30 min @ 200°C

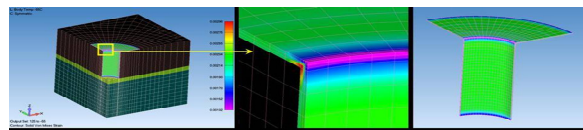


Figure 12. FEM of Via with 50% epoxy fill

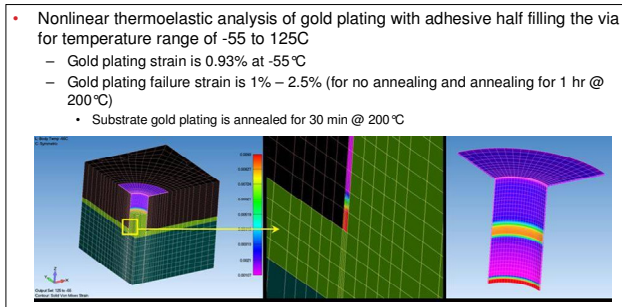


Figure 13.. FEM of Via with 100% epoxy fill

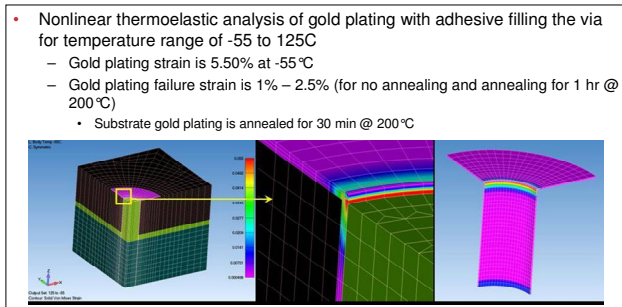
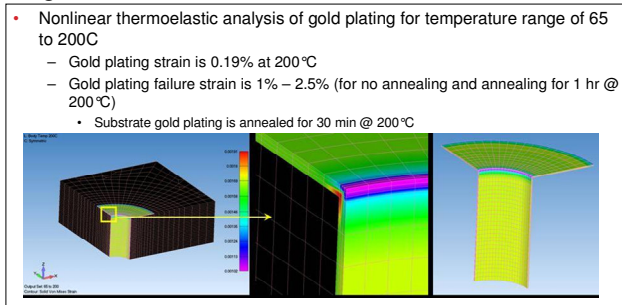


Figure 14. FEM of Gold Film at T=200C



Multiple cross-sectioning locations (25%, 50%, 75% into via) of each via was performed to verify Figure 9. Mechanical properties of gold film that the crack or break in the via metallization could be observed. A total of 22 vias out 100 via sectioned failed. The results indicated that any via filled with silver epoxy >40% caused the via metallization to exceed its elongation limits resulting in a fracture of the via metallization. Figures 15 and 16 show the examples of the failures in the via metallization.

Figure 15. Post Temperature Cycling Via Fill <75%

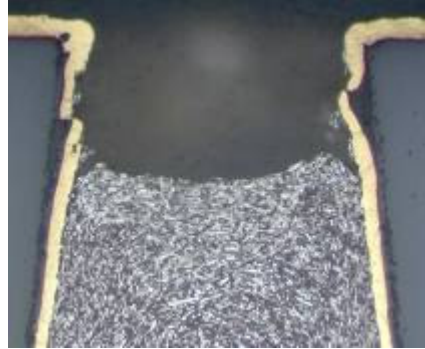
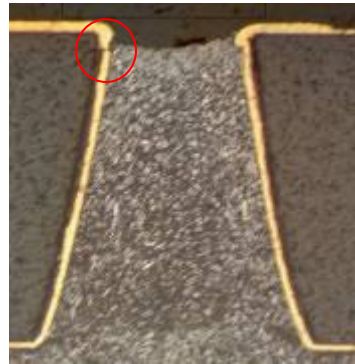


Figure 16. Post Temperature Cycling Via Fill less than 90%



Verification Using a CTE Compliant Plugging Material

Thin Film patterned substrates from three suppliers were used to fabricate verification samples. A total of 103 vias were processed with the new via fill materials.

The samples were subjected to 116 temperature cycles, -55 to 125C, followed by 300C bake for 1hour, and then cross sectioned to examine the via metallization. All the samples passed and examples of the cross sections are shown in Figures 17, 18, and 19.

Figure 17. Compliant Via Fill Material

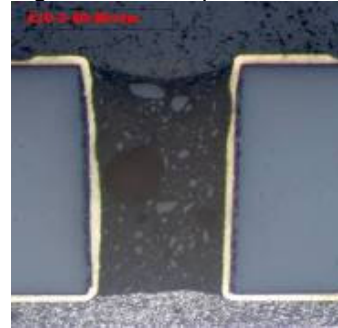


Figure 18. Compliant Via Fill Material

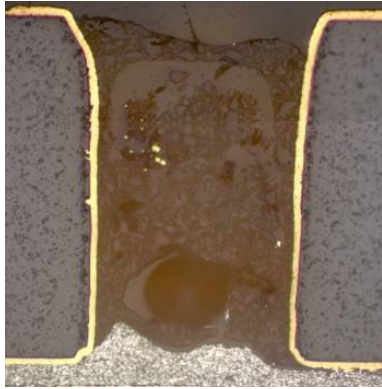
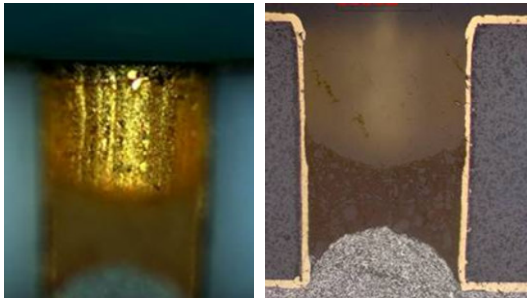


Figure 19. Compliant Via Fill



Conclusion

The relatively high CTE of the silver filled epoxy used to plug the vias induced strains on the gold via metallization which exceeded allowable limits when the product was exposed to temperature cycling.. These strains resulted in crack formation in the vias which in some cases increased the resistance of the ground path and degraded RF performance.

The selection of a “via plugging material” to prevent epoxy squeeze-out onto the top surface of a substrate must consider the thermal expansion of the material and aim to match the CTE of the substrate material (alumina). The selected material must be tested using representative coupons to ensure that the vias will survive the mission environments of the application over the life of the product. Understanding and validating the affect of via plug materials on the reliability of gold plated via structures is an essential part of the design and production of high reliability electronics for space applications.

References

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- [2] Abelbond, 84-1LMI Datasheet, Abelstik, Rancho Dominguez, CA 90221, 07/2001