

Interconnection Design and Impact Life Prediction Subjected to Board Level Drop Test

Chan-Yen Chou, Chao-Jen Huang, Tuan-Yu Hung, and Kuo-Ning Chiang

Advanced Microsystem Packaging and Nano-Mechanics Research Lab. PME

Advanced Packaging Research Center

National Tsing Hua University, HsinChu, Taiwan 300, R.O.C.

Phone: 886-3-5742925 Fax: 886-3-5745377

E-mail: knchiang@pme.nthu.edu.tw

Abstract

In this study, the objective is to develop a proper impact life prediction model for stress-buffer-enhanced package which has a specific failure mode, the fatigued metal trace, during board level drop test. The so called stress-buffer-enhanced package applies a thick and soft buffer layer to protect solder joints; however, metal traces embedded inside the buffer layer are instead broken. The fatigued metal trace is not common for board level drop test, and there are few life prediction models to predict the performance of the package. Unlike thermal cycle test, the dynamic response of drop impact is irregular and not cyclic; therefore, the concept of cumulative damage is considered in the life prediction model. The results showed that the cumulative plastic strain of metal trace could accurately predict impact life. Besides, the interconnection designs are then proposed in this study. Results show that the curved trace layout and the sandwich structure can greatly enhance the drop performance of the stress-buffer-enhanced package.

Key words: drop test, life prediction, fatigue, trace failure

1. Introduction

Accompanying the increasing popularity of portable and handheld products, high reliability and high resistance of drop impact capability of handheld products becomes a great concern for semiconductor and electronic product manufacturers. It is more and more important to study the dynamic response of packages during the mechanical shock caused by customer usage in portable devices and mobile applications. In line with this, the board level drop-test regulations formed by JEDEC [1], [2] were published to assess drop performance for surface mounted IC package.

About the study of board level drop test, several researches have been published. Tee et al. [3] proposed "Input-G method" to reduce the huge computation amount of drop test simulation. The input-G method ignores the drop table, fixture and contact surface, and instead, the impact pulse is taken as input acceleration loading at 4 screws of test board. Chiang et al. [4] proposed "Modified Input-G method", which considered the effect of screw tightness. The residue stress caused by tight screw condition was applied on the test board. Results showed that the drop performance was lowered when the screw tightness became worse. However, few studies mentioned about the life prediction model for board level drop test. Because

of the highly uncertainty of the drop test and the lack of precise simulation model, it is difficult to develop a stable life prediction model with good experimental correlation. Tee et al. [5] proposed impact life prediction model using the maximum peeling stress of critical solder as failure criteria to determine the drop life of packages. Results showed that the characteristic impact life is a more consistent parameter compared with first-failure life, as the process and testing variation is minimized through averaging test data.

In this research, the board-level drop test, failure analysis, dynamic simulation, and impact life prediction model are established. Afterward, the structural optimal design is carried out to improve the drop test performance of packages. The stress-buffer-enhanced package [6]-[8], which has high reliability for both drop test and thermal cycle test, is chosen as the test vehicle of the prediction model. For a better understanding, Fig. 1 illustrates the sketch of the stress-buffer-enhanced package. The IC chip is attached on the chip carrier. Filler polymer is applied around the chip, disclosing the package's capability of fanning out connections. Afterward, the redistributed interconnects are laminated on a soft and thick dielectric layer. The whole package is finally mounted on a PCB board by solder joints. The thick dielectric layer provides a stress buffer to protect solder joints from mechanical

deformations. However, the metal traces within stress buffer layer suffered relatively larger deformation because of the greatly deformed dielectric layer.

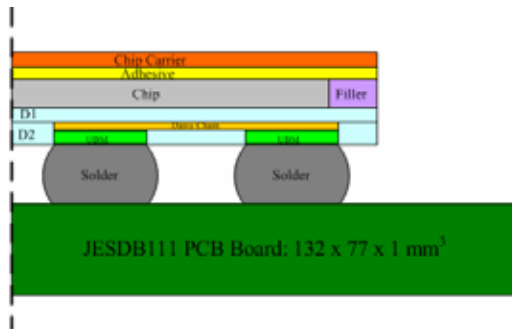


Fig. 1: Illustration of stress-buffer-enhanced package

2. Drop Test Experiment and Results

The drop test experimental setup is illustrated in Fig. 2. 15 stress-buffer-enhanced packages (5mm x 4.5mm) were mounted on standard JEDEC drop test board (132mm x 77mm x 1mm). In this study, JEDEC B111 drop test condition B was adopted. The peak acceleration, pulse duration and drop height are 1500 G, 0.5 ms and 112 cm respectively. A multi-channel real-time electrical monitoring system was utilized to observe the input acceleration of drop table and the in-plane strain at the center of PCB simultaneously. Subsequently, a multi-event detector system was installed to measure the dynamic resistance of daisy-chained packages.

The drop test result is shown in Table 1; from this, several phenomena different from foregoing board level drop test studies were observed. The position of first failure was located at corner chip (U1) which varied from that of previous studies [3] which was located near the center of PCB (U3, U8, U13). The drop test analysis for conventional WLP disclosed the solder joint cracks along intermetallic compound (IMC) layer as the main cause of failure; in this study, however, fatigued metal traces in packages instead of solder joint fractures were perceived to be the reason of failure. It was thus presumed that the soft stress buffer layer absorbed the impact, thereby ensuring that the solder joints are protected. Nevertheless, the metal traces within stress buffer layer suffered relatively larger deformation.



Fig. 2: Drop test experimental setup

Because the failure mode of stress-buffer-enhanced package focused on the fatigued metal traces, the configuration of trace layout becomes a significant factor affecting the impact reliability of this package. Therefore, two kinds of trace layout, the straight trace and the curved trace, were then experimented. The fatigued metal trace failures were recorded as shown in Fig. 3. And the experimental results were listed in Table 1. In Table 1, P1 represented packages pass 90 drops, while P2 represented packages pass 240 drops. Interestingly, the failure occurred in the order of U1, U11, U5, and U15. The experimental result is caused by the asymmetric configuration of solder joints and trace layout, shown in Fig. 4. Figure 4 shows the straight trace layout which has sparse solder joints at bottom-left corner. The U1 package has relatively the shortest distance between the sparse solder joint area and the fixed screw. As a result, the impact wave from the screw attacks the weak sparse area directly, causing the first failure of U1 package. Therefore, in this research, we assume that every position of the packages, i.e. U1, U2, ..., U15, should be treated as an individual experiment during board level drop test, even though they are all mounted on the same test board.

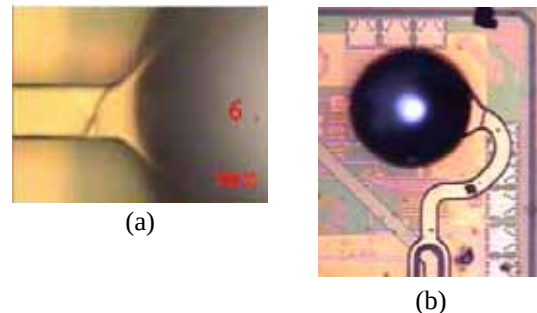
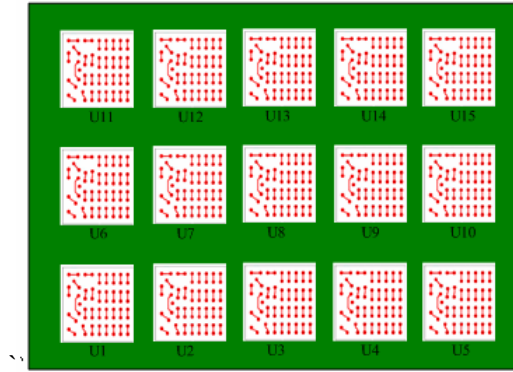


Fig. 3: Failure analysis of fatigued metal trace (a) failure of straight trace (b) failure of curved trace

Table1: Experimental results of board level drop test

Straight Layout	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15
Board#1	58	P1	47	P1	31	P1	P1	P1	P1	P1	25	P1	26	66	26
Board#2	67	P1	72	P1	39	P1	P1	P1	P1	P1	29	85	36	75	25
Board#3	48	72	53	P1	46	P1	P1	P1	P1	P1	20	P1	26	46	21
Board#4	71	P1	53	P1	42	P1	P1	P1	P1	P1	18	P1	29	41	25
Curved Layout	U1	U2	U3	U4	U5	U6	U7	U8	U9	U10	U11	U12	U13	U14	U15
Board#1	116	P2	138	P2	P2	P2	P2	P2	P2	P2	151	P2	P2	P2	196
Board#2	129	P2	P2	P2	217	P2	P2	P2	P2	P2	161	P2	P2	P2	239
Board#3	102	P2	166	P2	127	P2	P2	P2	P2	P2	102	P2	P2	P2	221

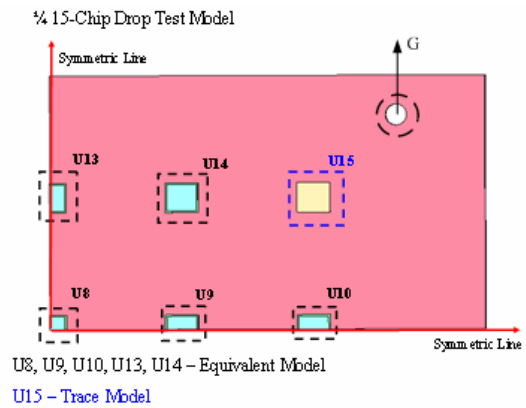
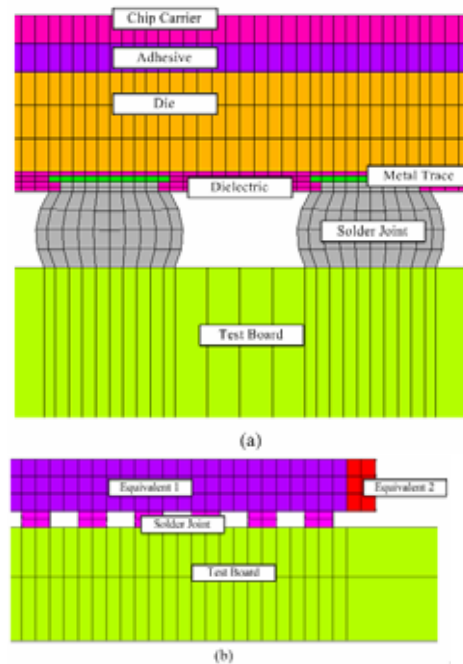
**Fig. 4: Relations of trace layout and board position**

3. Drop Test Finite Element Modelling and Analysis

From the aforementioned results, the experimental data revealed that every package on the test board should be treated as an individual experiment, because the dynamic responses of the packages are all different. In the finite element modelling, the quarter model of the test board with 15 packages mounted on it was constructed using FEA software LS-DYNA, shown in Fig. 5 and Fig 6. Several simplifications were applied to reduce the extremely large calculation of the finite element model. For the correlation package, i.e. package U15, the detailed finite element model was built, while simplified finite element model was applied for the rest of the packages, i.e. packages U8, U9, U10, U13, and U14. Figure 6(a) shows the detailed model include the chip carrier, adhesive layer, die, filler polymer, dielectric layer, metal trace, solder joint, and test board. Figure 6(b) shows the simplified finite element model; the solder joint was considered as a rectangular column. Besides, the complicated structure of the stress-buffer-enhanced package was replaced by equivalent material obtained by rules of mixture [9]. Equivalent1 layer represents the replacement material for the die region, and equivalent2 layer represents for the filler polymer region.

The confirmation of the equivalent model is shown in Fig. 7, representing the strain response of test board. Results show that the strain variation between complete model and equivalent model is within acceptable range; however, the computational

time can greatly reduce from 438 hours to 57 hours. Yeh et al. [10] also proposed similar simplification procedure, resulting in a good validation.

**Fig. 5: Finite Element Modeling of Test Board****Fig. 6: (a) Illustration of trace model, (b) Illustration of simplified model**

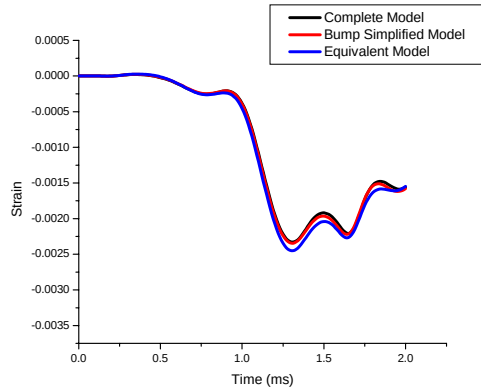


Fig. 7: Confirmation of equivalent model

For ensuring the accuracy of dynamic simulations, the experimental validation with simulation result was performed. The acceleration of package U15 (package side) was validated in this study. Because package U15, the detailed model, was chosen as the correlation of life prediction model, the more accurate of the simulation result of package U15, the more reliable of the impact life prediction model. Figure 8 shows the acceleration validation of package U15. The validation shows good agreement between experimental data and simulation result. Based on the simulation results, the development of life prediction model was made as described in the following section.

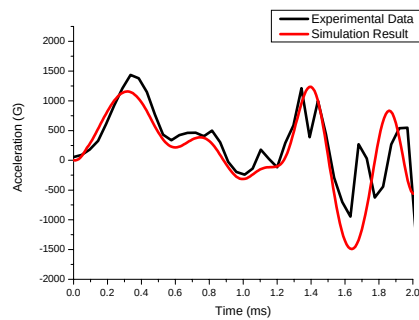


Fig. 8: Validation of acceleration at package U15

4. Impact Life Prediction Model

In order to quantitatively estimate the impact performance of packages, five drop experiments, 2 straight trace layout and 3 curved trace layout, were selected to construct the related finite element model as shown in Fig. 9. According to the aforementioned experimental results, every position of the packages, i.e. U1, U2, ..., U15, should be treated as an individual experiment during board level drop test due to their asymmetric trace layout and solder joint distribution. Case1 and case2 represented models of straight trace layout at different position, U1 and

U15. Case3, case4 and case5 represented models of curved trace layout at different position; especially, case5 has a thinner dielectric layer. Besides, in order to decrease the computation amount, all the five cases only have one critical trace where the failure was frequently observed in drop experiments, shown in Fig. 9.

All the simulations were conducted from 0ms to 6ms, which represented the period of the fundamental natural vibration of test board. The simulation results are shown in Fig. 10. Results show that large plastic strain concentrated at the neck area between metal trace and pad. Besides, the effective plastic strain responses on traces are shown in Fig. 11. The strain response would be the foundations of the impact life prediction models.

Fatigue fractures are the most commonly identified kinds of failure of structural metals. It is defined as the phenomenon of failure of a material under cyclic loading. However, the dynamic responses of board level drop test, i.e. the strain response at metal trace, are irregular and not repeated. The conventional Coffin-Manson relation [11] may not be suitable for the impact life prediction. According to the cumulative damage theories [12], [13], the fatigue fracture is considered to be a process of damage accumulation until a certain maximum tolerable damage. In other words, fatigue is an exhaustion process of a material's inherent life. Therefore, the impact life prediction model is developed based on the cumulative damage theories.

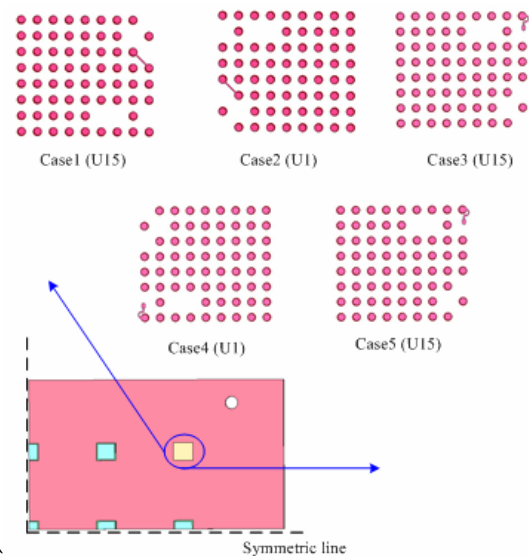


Fig. 9: Illustration of correlation models

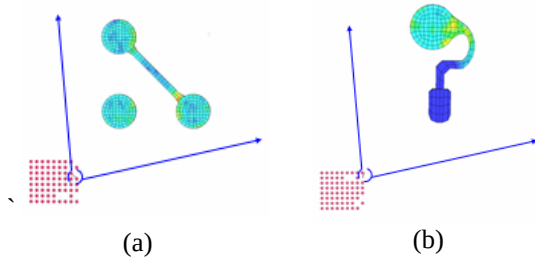


Fig. 10: Strain distribution of metal traces (a) straight trace (b) curved trace

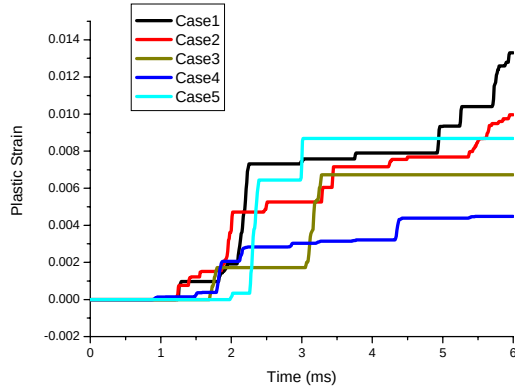


Fig. 11: Maximum effective plastic strain propagation of metal traces

Table 2: Metal trace impact life prediction results

	Trace Layout	Position of Package	Dielectric Thickness (μm)	Experimental Characteristic Life (Drops)	Predicted Characteristic Life (Drops)
Case1	Straight Trace	U15	40	24.82	-----
Case2	Straight Trace	U1	40	64.77	-----
Case3	Curved Trace	U15	40	128.46	-----
Case4	Curved Trace	U1	40	234.21	298.7
Case5	Curved Trace	U15	30	72	77

Through the proposed impact life prediction model, one can determine the drop impact performance of a specified package quantitatively. This approach provides both accurate simulation comparison and absolute impact life prediction. Moreover, designers may execute computational experiments to greatly reduce expensive experiments, and accelerate time-to-market procedures. However, similar to most finite element models, the value of plastic strain obtained from dynamic simulations depends on the element size and other modelling assumptions. The uncertainties of board level drop test are also affecting the reliability of this impact life prediction model. There are no universal correlation parameters; similar situations occurred in thermal cycling predictions. For more accurate impact life predictions, it is suggested that both

The impact life prediction models proposed in this study is related to the cumulative plastic strain, shown in Eq.1. In Eq.1, $\Delta\epsilon_{pl}$ represents the incremental plastic strain in every time step; C_1 and C_2 are correlation parameters.

$$N_f = C_1 \left(\sum \Delta\epsilon_{pl} \right)^{C_2} \quad (1)$$

Following, case1, case2, and case3, were chosen to estimate the correlation parameters, C_1 , and C_2 . After correlations, C_1 and C_2 are determined to be 57.64 and -2.049 respectively. Case4 and case5 were chosen to be the predicted models using the anterior correlation parameters. Table2 list the prediction results. The characteristic life in Table 2 was obtained using Weibull distribution. Results show that there is a good correlation for impact life prediction model. Accordingly, the cumulative plastic strain is suitable for the impact life prediction model, because the failure of drop test belongs to low cycle fatigue which is dominated by plastic strain.

dynamic simulations and drop experiments need to be detailed considered.

5. Interconnection Design

The interconnection design of the stress-buffer-enhanced package is accomplished in this section. It is known that the failure mode of the stress-buffer-enhanced package focuses on the fatigued metal trace. As a result, the trace layout design becomes an important issue in this study. Several interconnection designs including trace layout design, sandwich structure, and chip size /package size design are proposed to enhance the metal trace reliability.

Trace Layout Design

In this section, two different trace layout designs, the straight trace (I-type trace) and the curved trace (S-type trace), are investigated to elucidate the improvement of drop performance of stress-buffer-enhanced package. Figure 12 and shows the modeling of I-type and S-type trace layout respectively. Besides, each type further has horizontal and vertical trace layout design.

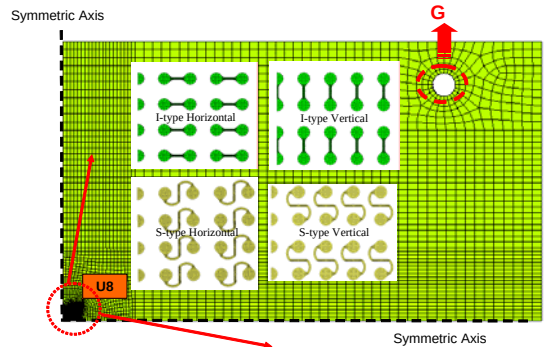


Fig. 12: Trace Layout Model

Simulation results of plastic strain distribution at traces are shown in Fig. 13. The experimental failure modes are also compared with simulations. The major loading exerted on traces is from the relatively displacement of adjacent solder joints along the long axis of test board, i.e. the direction of horizontal trace layout. As a result, the loadings on horizontal I-type trace layout are stretching loads, while the loadings on vertical I-type traces are shearing loads. The loadings on S-type traces become more complicated. From the simulation result, one can tell that the loadings on horizontal S-type traces are shearing loading, while they are bending loading on vertical S-type traces. The S-type trace layout provides extra buffers when the traces are deformed by the solder joints and dielectric layer during drop impact. The simulation results also indicate that the plastic strain of S-type trace layout only occurs at the neck area between trace and pad. The S-type trace layout can release lots of stress concentration because of its high flexibility. Figure 14 shows the plastic strain propagation of traces. The maximum plastic strains of S-type traces are all smaller than that of I-type traces.

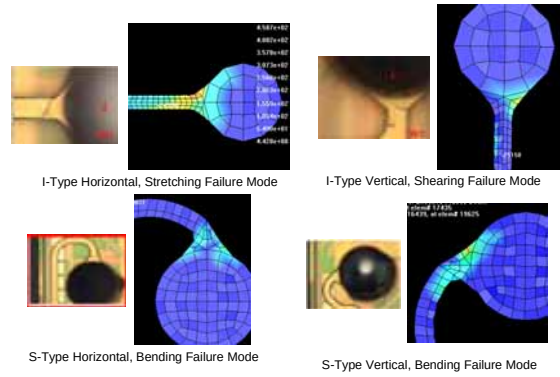


Fig. 13: Plastic strain distribution of traces compared with experimental failure mode

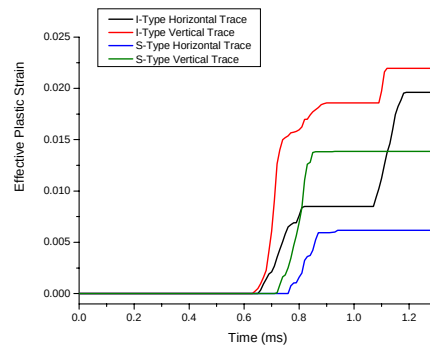


Fig. 14: Plastic strain response of trace layout design

Sandwich Structure Design

The stress-buffer-enhanced package provides a good stress buffer to protect the solder joint. However, the deformation of soft dielectric layer becomes much larger than the conventional wafer level package. The metal trace embedded in the dielectric layer becomes a dangerous portion during drop impact. For a compromise between the reliabilities of solder joint and trace line, the “sandwich structure” is proposed as a structural improvement for the stress-buffer-enhanced package, shown in Fig. 15. The so-called sandwich structure is to laminate one more lamination on the top of stress buffer. This lamination is a dielectric layer with much higher Young’s modulus, such as PI, BCB materials.

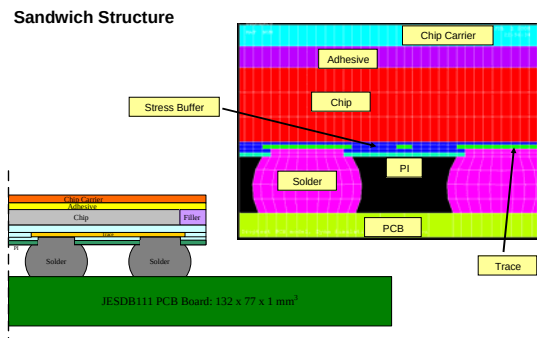


Fig. 14: Illustration of sandwich structure

Figure 15 shows the comparison of plastic strain at trace between stress-buffer-enhanced package and sandwich structure. One can observe that the plastic strain of sandwich structure is much reduced. The trace of sandwich structure reveals brilliant reliability because the PI layer can “hold” the stress buffer from large deformation. For the inspection of solder joint reliability, the solder joint is well protected because the thickness of stress buffer layer is the same as the original model. That is to say the sandwich structure can improve the trace reliability, as well as keep the performance of solder joint at the same time.

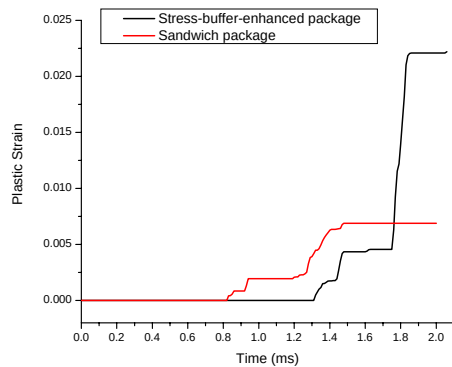


Fig. 15: Plastic strain response at trace for sandwich structure

● Chip Size /Package Size Design

The stress-buffer-enhanced package is the one with fan-out capability. Traces and solder joints can be placed outside the chip to the filler area. The Young's modulus of the filler polymer is similar to the dielectric layer, which means the filler area is actually a big stress buffer with 190 μm thickness (the thickness of chip layer). Therefore, in the filler region, most of the impact loading is absorbed by the filler polymer. Both solder joint and trace line can be well protected.

Based on the concept, the small chip size design is proposed in this section. The small chip size can increase the filler area. In the original design, the chip size is 4.5mm x 4mm, while the package size is 5mm x 4.5mm. For the small chip size design, the chip size reduces to 3.5mm x 2.5mm, shown in Fig. 16. Figure 17 shows the plastic strain at trace for small chip size design. One can see that the plastic strain is only 40% compared with original stress-buffer-enhanced package, indicating the effect of filler polymer. On the aspect of designer, the package size is suggested to be larger than the chip size. So that the outmost solder joints and traces can locate at the filler polymer region. As a result, the drop performance of outmost trace can be improved.

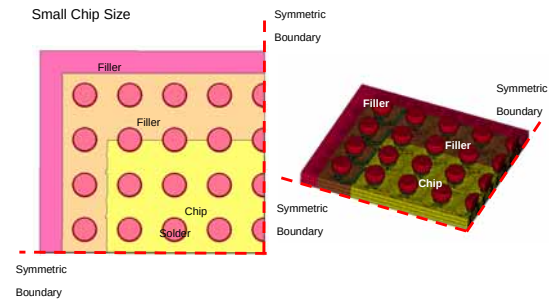


Fig. 16: Modelling of small chip size design

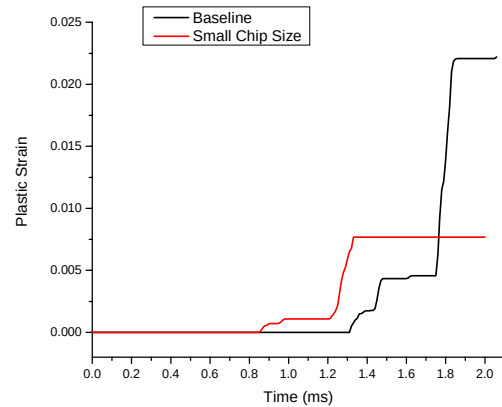


Fig. 17: Plastic strain response at trace for small chip size design

6. Conclusions

This study intended to develop a reliable impact life prediction model for metal traces which becomes a must to estimate the performance of packages subjected to drop impact. Several LS-DYNA simulations were conducted to elucidate the mechanical behavior of test board and packages. After validating the simulation results with experimental data, the development of impact life prediction model were then accomplished. The impact life prediction model was proposed using the cumulative plastic strain as failure criterion related to impact life. Results showed that the cumulative plastic strain is suitable for the impact life prediction model, because the failure of drop test belongs to low cycle fatigue which is dominated by plastic strain. There is good correlation between impact life predicted by simulations and measured by experiments.

Afterwards, several interconnection designs including trace layout design, sandwich structure, and chip size /package size design are proposed to enhance the metal trace reliability. In the trace layout design, it is recommended that the curved trace layout can release the stress concentration. The experimental results also indicate the curved trace layout is capable to bear higher drop numbers. The sandwich structure and small chip size design are proposed in this research. The so-called sandwich

structure is to laminate one stiffer lamination (PI, BCB) on the top of stress buffer. The trace of sandwich structure reveals brilliant reliability because the PI layer can “hold” the stress buffer from large deformation. For chip size design, the small chip size can increase the filler area. The Young’s modulus of the filler polymer is similar to the dielectric layer, which indicates that the filler area is actually a big stress buffer with 190 μ m thickness (the thickness of chip layer). When traces and solder joints are placed outside the chip to the filler area, reliabilities of solder joints and traces are much improved because the filler polymer absorbed a large portion of impact energy.

Acknowledgements

The authors would like to thank the National Science Council NSC97-2222-E-007-007-MY3 and Advanced Chip Engineering Technology Inc. for supporting this research.

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