

Continuous Au-Sn-Ni-Cu-Pb (ASN-CP) Layer Formation on Double Tin and Wicked Thick-Au/Ni Plated Printed Circuit Boards

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Abstract

This paper describes a thin (~200 nm) continuous intermetallic layer containing Au, Sn, Ni, and sometimes Cu and/or Pb (referred to as the ASN-CP layer) observed at the Ni-SnPb eutectic solder interface on both the pad and component sides of a completed solder joint after double tin and wicking to remove Au on thick Au over Ni-plated pads. The source of each of these elements within the layer was considered. Changes in the heat application method used during the tinning operations did not alter the layer formation, but the adjacent circuit geometry showed a noticeable effect. Circuitry with wider traces exiting the tinning location had a higher likelihood of containing the ASN-CP layer than pads with narrow traces. Finally, a thermal cycle life test was performed on solder joints containing the ASN-CP layer which indicated that the layer thickened over many thermal cycles and grew a secondary AuSn₄ intermetallic layer which adversely affected the fatigue behavior of the solder joints containing the layer. Thus when implementing a double tin and wicking processes on thick Au PCBs it is necessary to account for the geometry of circuitry adjacent to the solder interconnect locations, particularly in high stress locations where BGA, LCC or other limited-strain-relief package interconnects are made.

Keywords: Au-Sn Intermetallic, Double Tin & Wick, Au Removal, High Reliability Packaging, Soldering to Au

I. Introduction

The understanding that excess Au needs to be removed from solderable surfaces to prevent the formation of undesirable Au-Sn intermetallics is well established. As early as 1962, F. G. Foster documented some of the adverse effects of soldering to Au plated surfaces [1]. In 1965, JPL implemented a “tin and wicking” process for the solder cup area of electrical connector contacts used in wire harness construction [2]. In 1972, Ainsworth recommended “washing or wicking off” thick (>1.5 μm) Au to ensure the creation of mechanically reliable solder joints on printed circuit boards (PCBs) [3]. In 2000, Vianco and Kilgo showed that a “double tin and wick” process was necessary to ensure a robust Au removal process [4]. Today, J-STD-001D Requirements for Soldered Electrical and Electronic Assemblies and J-STD-001DS Space Applications Addendum provide clear guidance for Au removal on component leads and solder terminals on PCBs for High Performance Electronic (Hi-Rel) Products

(Class 3) specifying the use of double tinning or a dynamic solder wave process [5,6].

With this level of appreciation for Au removal, Au embrittlement associated failures should be a thing of the past. Unfortunately, the electronic packaging industry continues to battle embrittlement related failures. The issue becomes even more critical as large Ball Grid Array (BGA) and Leadless Chip Carrier (LCC) packages become more prevalent in high reliability applications. Their large relative size; high coefficient of thermal expansion (CTE) differential to PCB materials; lack of solder joint strain relief; and poor inspectability make them particularly sensitive to any degradation within their solder attachments. Depending on the environmental and life requirements of the application, most compliant leaded devices can tolerate a Au content within their solder joints up to 3 wt% [9]. For BGA packages on the other hand, Au embrittlement related failures have been observed in solder joints with Au content as low as 0.1% [7]. Therefore when thick Au removal is required on PCBs to be used with BGA packages or other limited-strain-relief components, a

robust Au removal process must provide nearly 100% Au removal to ensure the formation of reliable solder joints.

For the most part, the mechanics of Au removal from PCB surfaces have not changed since being developed over four decades ago. All Au removal techniques rely on the rapid dissolution of Au into molten Sn containing solder. Table 1 shows the rapid rate that Au is consumed into molten Sn at different temperatures. As the data suggests, the consumption rate is highly dependent on the temperature of the removal process. For relevant thicknesses of thick Au on PCBs from 0.7-3.5 μm , the Au is easily dissolved in <1 sec for hand solder operations above 235°C. On the other hand, infrared reflow with a max temperature of ~220°C requires significantly longer time on the order of tens of seconds to remove the same amount.

Table 1: Rate of Au consumption in molten Sn. [8]

Temperature	Consumption Rate ($\mu\text{m/s}$)			
Time = >	1 s	2 s	10 s	20 s
235°C	N/A	5	25	35
240°C	35	60	120	146
245°C	50	112.5	N/A	N/A
250°C	75	N/A	N/A	N/A

Italics indicate a linearly extrapolated value.

In the typical Double Tin and Wick process for PCBs, eutectic Sn-Pb solder (or some other Sn containing solder) is applied by hand, or silkscreened on in paste form, to the Au plated terminals then melted using an iron or infrared reflow oven. During this step a majority of the Au is dissolved into the molten solder. Upon cooling, Au-Sn compounds can form in the Pb-Sn matrix where local composition meets that of intermetallic phases dictated by the phase diagram [8]. Solder wick is then applied to the solder mound on the terminal pad and heated with an iron which melts the solder allowing it to get pulled into the wick by capillary action. Depending on the temperature of the liquid solder with respect to the intermetallic melting temperature, the Au-Sn intermetallics (Au-Sn, Au-Sn₂ or Au-Sn₄) may not liquefy during this step. Despite remaining solid, the fluid motion of the solder can sweep the poorly adhered intermetallic solids into the wick. This process is then repeated with the additional application, reflow and removal of solder. This second step is intended to remove any residual Au_x-Sn_y intermetallic phases on the surface that did not get swept away during the first wicking step and to dissolve any remaining Au from the surface.

A review of the Au content within the solder on the terminal through the double tin and wick

process using the typical Au weight percentage calculation method for the double tin and wick process for a nominal 2.5 μm (100 μin) Au plating thickness shows that the initial tinning operation would yield an embrittled solder joint in excess of the typical 3% rule of thumb value (see Table 2) [9]. Assuming a uniform distribution of Au_x-Sn_y intermetallic phases in the solder mound and an estimated 66% solder volume removal rate per wicking operation, the wicking and subsequent tinning operations bring the Au level remaining in the solder joint well below the acceptable level for most component classes (although not below the 0.1% level that may be required for BGAs).

$$\text{wt\%Au} = \frac{\text{wtAu}}{\text{wtAu} + \text{wtPbSn}} \times 100$$

Table 2: Weight % Au estimates for each step of the double tin and wick process for 2.5 μm Au plating.

After 1 st Tin	After 2 nd Tin	Final Solder Operation
5.40%	1.40%	0.50%

According to the Au-eutectic Sn-Pb phase diagram, this percentage of Au (0.5%) should be fully soluble within the Sn-Pb solder [8]. Unfortunately, cross section results from various double tin and wicked pads fail to support this result.

The intent of this paper is to describe the existence of a thin continuous “ASN-CP” layer which compositional analysis indicates contains Au, Sn, Ni and sometimes Cu and Pb present on pads originally plated with thick Au (>2.5 μm) that have been subjected to double tin and wicking processes to achieve Au removal. It will assess how variations in the tinning method effect the layer formation; hypothesize the mechanics behind the layer formation; and finally attempt to evaluate effects that the ASN-CP layer may have on the reliability of solder joints.

II. Experimental Procedure

In order to study the ASN-CP layer properties and evaluate how changes in the tinning process affects its formation, several Cu pads plated with Au ~3.5 μm thick plated over ~4 μm thick Ni were double tin and wicked to remove Au and prepare the pads for component soldering. Each pad is etched on a Polyimide, woven E-Glass constructed PCB. The pads have 3 types of planar geometry based on the pad size and trace width exiting the pad (see Figure 1). The 3 pad geometries will allow for an assessment of whether changes in the amount of Au available at the solder-Au interface affect the

layer formation. For each tinning step a single 0.5 x 0.5 x 0.1 mm eutectic 63Sn-37Pb solder tab was used. To simulate the final component solder operation a 3rd solder tab was reflowed on each pad and left in place. The pad distribution, processing details and sample names can be found in Table 3.

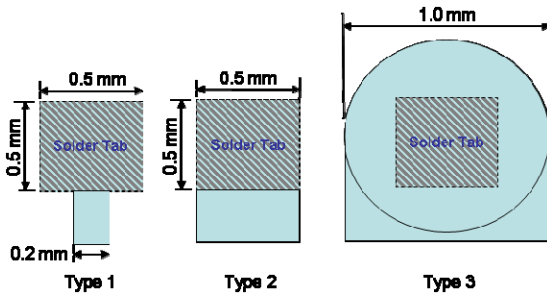


Figure 1: 3 Test pad geometries.

Table 3: Process details and identifiers used for tinning sample construction.

Sample Number:	#1	#2	#3
Sample Name	Reflow	Room Temp	Hot Plate 120°C
Tinned Pads	5	7	7
Pad Types (1/2/3)	2/3/0	4/3/0	5/1/1
Tinning Process			
PCB Temp.	218°C max	25-31°C	117-126°C
Time at Temp	31 sec	~1 sec	~1 sec
Operator	Oven	B	B
Wicking Process			
Temp.	R/T	R/T	117-126°C
Wick	Copper Braid	Copper Braid	Copper Braid
Operator	A	B	B
Pad Au Plating			
Mean Thickness (μm)	~3.5	3.56	3.46
Pad Ni Plating			
Mean Thickness (μm)	~4.2	4.43	4.10

Because of the sensitivity of Au's dissolution rate into Sn to changes in temperature, three different heating conditions were evaluated to assess if different tinning conditions affected the layer formation. Sample 1 pads were tinned using reflow infrared heating with a maximum temperature achieved of 218°C. Sample 2 was tinned using a 371°C soldering iron only. Finally, Sample 3 was heated to approximately the half-way point between room and the reflow oven temperature on a hot plate (~120°C) with reflow of the solder achieved by applying a soldering iron to the heated tab. For Sample 1, the solder was above its melting temperature for ~90 seconds and at the max profile temperature for 31 seconds. For Samples 2 & 3, the solder was molten for ~1 second for each tinning operation. The temperature profile of the reflow tinning operation can be seen in Figure 2. Also included are estimates for the maximum temperature achieved by the solder during the iron reflow operations which were derived using a grossly simplified lumped capacitance model for the solder

tab and copper pad [10]. A detailed finite element model similar to that presented by Tian et al would be required to get a more accurate temperature assessment [11]. The wicking operations for Samples 1 & 2 were performed at room temperature while Sample 3 was done on the hot plate.

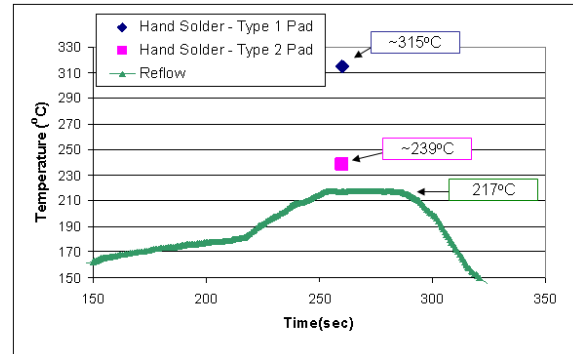


Figure 2: Solder reflow temperature profiles used.

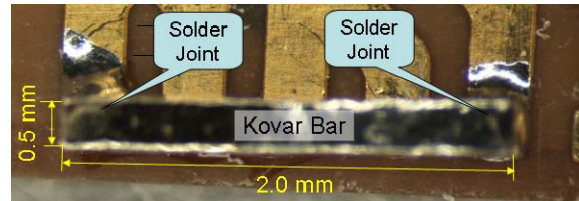


Figure 3: Life test bar soldered on double tin and wicked PCB.

In order to assess the effect (if any) of the ASN-CP layer on the reliability of solder joints, a thermal cycle article was constructed using four Ni-plated Kovar rectangular cuboid bars ($\alpha_c=5.86$ ppm/°C) which were solder tinned then soldered on both ends to room temperature double tin and wicked Type 1 or Type 2 pads on the same polyimide type PCB ($\alpha_s \sim 14$ ppm/°C) with similar surface finish (Au ~3.5 μm thick) used for the tinning testing described above. Control bars were also soldered to Type 1 pads on a separate polyimide PCB that would not be exposed to environments to allow for comparison with the thermal cycled solder joints. A single solder tab was used at each pad to form each joint and tinning was only performed on the pads where the bars were attached. A sample bar can be seen in Figure 3. The bars (0.5x0.5x2.0 mm) were sized to provide unconstrained CTE-induced displacements across the solder joints of ~2 μm for the 180°C temperature range of the thermal test.

The thermal testing consisted of cycling the article in a shuttle chamber from -55°C to +125°C with 30 minute hot dwells and 15 minute cold dwells. Since the intent of the thermal test was to cycle to failure, the number of cycles was not predetermined.

Using the predictive equation for a leadless surface mount component from Section 4.3 of IPC-SM-785, ~400 cycles would be required to achieve a failure rate of 25% [12]. At the end of 400 cycles, failures in a subset of the solder joints were observed and the test was halted.

All three tinning samples (Samples 1, 2, & 3), the thermal cycle article, and the bar attachment control were cross-sectioned, mechanically polished and characterized using FE-SEM and semi-quantitative EDS analysis.

IV. Results and Discussion

As can be seen in Figure 4, the ASN-CP layer is a continuous thin (~200 nm) layer separating the bulk of the solder from the Ni under-plate (accurate layer thickness measurements were not possible with the current samples due to the limitations of mechanical polishing). EDS scans of the layer show elemental distributions as follows: ~50 wt% Sn; ~20 wt% Ni; ~20 wt% Pb; ~6 wt% Cu; and ~4 wt% Au. Unfortunately the interaction volume of the electron beam with the sample surface is on the order of several microns and therefore significantly larger than the ASN-CP interfacial layer thickness. This condition results in excitation of neighboring regions such as the Ni plating or regions of the Sn/Pb solder. Thus accurate assessments of the compounds present within the ASN-CP layer will not be attempted except when the layer geometry allows.

The origins of the Sn, Ni, and Pb within the interfacial layer are relatively straight forward, but the sources of the Au and Cu are less obvious. The Sn-Pb and Ni within the layer are contributed by the 63 Sn-37 Pb eutectic solder and Ni under-plating, respectively. Some portions of these 3 elements are likely from the surrounding area and not actually contained within the layer.

The Au that is present originated from the Au plating present on the pad and remains within the interfacial layer in one of two possible forms that failed to be removed during the two wicking operations. One possible form is that of Au_x-Sn_y (or other ternary) intermetallics that may have formed during the initial tinning operation where the Au concentration was highest. The higher Au concentrations would have been adjacent to the pad's plated surface so they would have preferentially formed near it. If they formed in contact with the surface and they were a phase with a higher melting point at which the tinning operations were performed, they could remain in place through the second tinning operation. The second form is Au dissolved within the liquid solder. At 220°C, eutectic solder can dissolve up to ~15 wt% Au [8]. That percentage

drops to 1.5% at the melting point for eutectic Sn-Pb solder then to ~0.5% at room temperature. Excess Au would form Au_x-Sn_y intermetallics if the cooling rate allowed; otherwise Au would get trapped within the solder upon solidification... Based on the absence of the intermetallics within the bulk solder, it is believed that the Au concentrations are low enough (~1.5%) to prevent their wide spread formation. The pad specific results which will be discussed below indicate that the Au content on the pad has a possible additional source from the adjacent solder/Au boundary at the edge of the tinned area which could continue to replenish the Au supply in the double tin and wicked area.

For the Cu, EDS results of the Ni plating showed no evidence of Cu diffusion and there was no exposed Cu contacting the solder in the adjacent area. Thus it is believed that the Cu is introduced during the wicking operations where a copper braid is used. The form that the Cu takes within the layer is unknown.

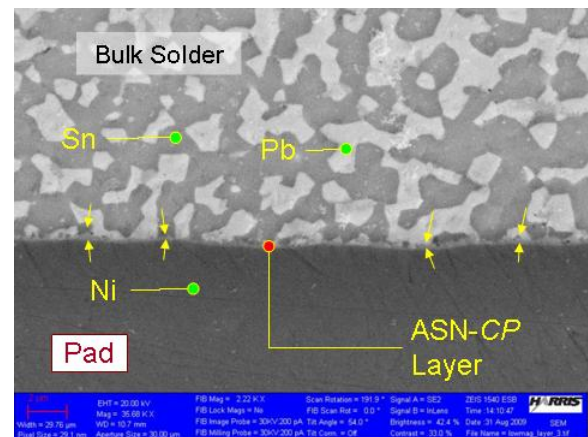


Figure 4: Typical FE-SEM cross section image showing ASN-CP layer located at solder/pad interface.

For a majority of the samples, EDS scans of the bulk solder showed only Sn/Pb. The exception is Sample 1 – Reflow. The bulk on its 5 pads uniformly contained a small percentage of Ni (1.7-3.9 wt%). One of its Type 1 pads showed Cu (1.6 wt%) in the bulk and 2 of the 3 Type 2 pads showed a similar Cu amount and a small percentage of Au (~3 wt%). The Ni is most likely diffusing from the surface during the extended time at temperature experienced by the Reflow sample. The bulk Au content results from the higher concentrations of Au in the applied solder during the tinning operations. Unlike the other 2 hand soldered samples where the solder remained localized in the pad area, the solder during the Reflow tinning operations had a tendency to spread out along the trace exiting the pad to the extent that at

the end of a tinning step the solder mount was found away from the pad getting tinned. This meant, particularly for the Type 2 pads, the same volume of solder was reacting with a greater volume of Au resulting in the higher residual Au levels.

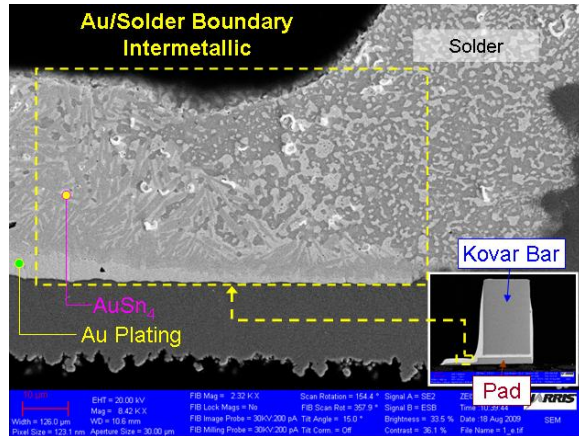


Figure 5: FE-SEM cross section image showing typical Au/solder boundary at the pad edge.

Variation of the three tinning heat application methods did little to change the resultant ASN-CP layer formation. The layer appearance when present did not deviate from the typical layer shown in Figure 4. Also the semi-quantitative microchemical analysis results remained fairly constant. A factor that did appear to play a role was pad geometry. A majority of the Type 1 pads regardless of tinning method, showed no evidence of Au present in the solder/pad interface layer whereas most of the Type 2 (& 3) pads did. The difference may stem from two possible factors. Since the cross-sectional area of the Au/solder interface at the edge of the pad, as shown in Figure 5, is larger in the Type 2 case, a larger portion of the Sn is consumed at the boundary during Au-Sn intermetallic formation leaving less Sn available to dissolve the Au away from the surface on the pad where it is required. This boundary may also continue to feed Au into the molten solder during the second tinning and final soldering steps. Also, as the temperature estimates for the hand soldering operations show (see Figure 2), there may be a significant temperature difference between Type 1 & Type 2 pads due to the increased copper mass in the Type 2 pad case, allowing for a time/temperature effect to influence the outcome. This explains why the Reflow samples which were at a slightly lower temperature for a much longer time had a reduced ASN-CP layer presence than the Hot Plate and Room Temperature samples for Type 2 pads.

As seen in Figure 6, the Control bar sample soldered to a Type 1 pad showed a similar solder

joint configuration as the tinning samples. The pad geometry factor remained consistent with the Control layers not showing a Au presence at the interface. An interfacial layer at the bar/solder interface also formed. It had the same composition as the pad layer including Cu despite not undergoing a wicking process indicating that the residual Cu on the tinned surface migrates around the joint during component soldering. Again, EDS scans of the bulk solder only contained Sn/Pb. Based on these results, the double tin and wicking process was effective in removing the Au from Type 1 pads agreeing with the results from the tinning samples. Thus it was concluded that the as-processed configuration of the thermal cycled Type 1 and Type 2 pad solder joints would match those described previously with layers forming on both the pad/solder and bar/solder interfaces.

Table 4: Distribution of tinning samples exhibiting ASN-CP layer by pad geometry shown.

Pad Type=>	Room Temp		Hot Plate			Reflow	
	1	2	1	2	3	1	2
Total Pad QTY	4	3	5	1	1	2	3
Percentage with ASN-CP Layer Present	0%	100%	20%	100%	100%	0%	67%
Percentage with Sn-Ni-Cu-Pb Layer Present	100%	0%	80%	0%	0%	100%	33%

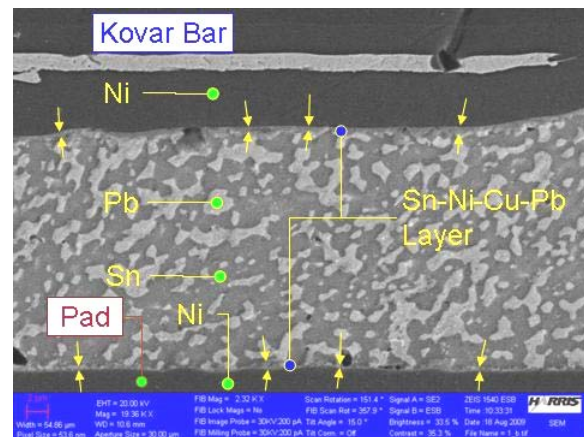


Figure 6: FE-SEM cross section image showing Control bar soldered to Type 1 pad.

Review of the thermal cycled joint cross sections revealed some interesting phenomena. As can be seen in Table 5, a bar soldered to a Type 1 pad, which should be Au free now shows the presence of Au in the pad/solder and bar/solder interfacial layers. Also, as can be seen in Figure 7, the layer's thickness has increased considerably, measuring ~2 µm thick on the pad side and ~0.5 µm on the bar side. In addition to the Au, its composition also showed an increase in Sn content and a corresponding reduction in Pb. This change may partially be attributed to the increased layer thickness

allowing for a more accurate elemental characterization.

Table 5: Weight% EDS results of solder/pad interfacial layers before and after 400 thermal cycles.

Pad Type =>	Type 1			Type 2		
Figure Label	"Phase" =>			"2"		
Interfacial Layer =>	1			1		
Element	RT	Control	=> Post 400 TC	RT	=> Post 400 TC	Post 400 TC
Au	-	-	=> 3.4	4.2	=> 7.6	21.8
Sn	53.0	50.8	=> 63.0	42.5	=> 59.8	57.0
Ni	23.6	27.8	=> 24.2	27.7	=> 25.4	2.6
Cu	4.9	11.5	=> 3.0	6.7	=> 7.2	1.1
Pb	18.3	9.9	=> 6.4	18.9	=> -	17.4

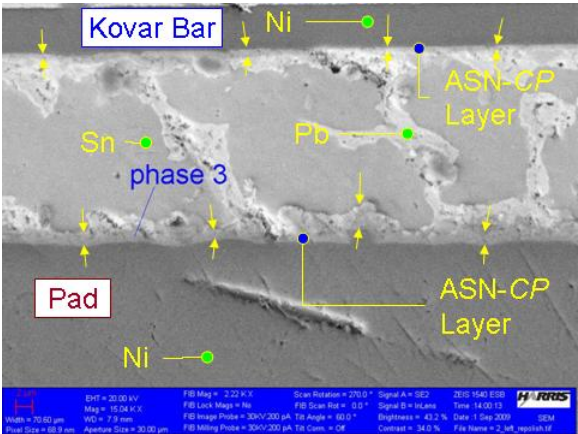


Figure 7: FE-SEM cross section image showing the Type 1 pad ASN-CP layer after 400 thermal cycles.

The thermal cycled Type 2 pad solder joints showed even more dramatic changes as shown in Figure 8. Not only has the ASN-CP layer on both the pad side and bar side increased in thickness (measuring ~1 μm thick), but a second intermetallic phase grew between it and the bulk solder. From Table 5, it can be seen that the elemental composition of the first layer reflects a higher Au concentration than that seen on non-thermal cycled ASN-CP layers. The Pb phase in the layer is also no longer detected. Again this in part is likely due to the distance from the bulk solder created by the growth of the second interfacial layer. EDS scans of the second layer showed that the normalized Au and Sn weight percentages correspond with the AuSn_4 composition (~70 wt% Sn; ~30 wt% Au) [11]. A comparison of the EDS results for the 3 interfacial layers observed in the thermal cycled solder joints to similar non-thermal cycled layers can be seen in Table 5. Significant changes are highlighted in red.

Detailed dimensional analysis of the thermal cycled solder joints indicated that the constructed solder joint thicknesses varied widely from the thickness used during the original cycles-to-failure (N_f) analysis. The analysis that predicted 406 cycles

to 25% failure was performed for a solder thickness of 38.1 μm . The actual thicknesses observed in the thermal cycled joints varied from 6 - 78 μm . Since the shear strain upon the solder joint is inversely proportional to the thickness, this range has a significant impact on the N_f analysis. The measured solder joint thicknesses, the updated failure rate analyses and whether cracks or failure for the joint were observed are listed in Table 6.

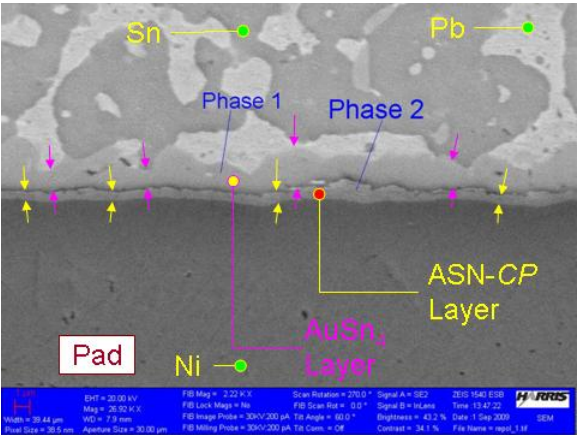


Figure 8: FE-SEM cross section image showing the Type 2 pad ASN-CP layer cross section after 400 thermal cycles.

Table 6: Measured thickness of thermal cycled solder joints with related failure observations and updated N_f analysis.

Bar	Side	Pad Type	Actual Thickness (μm)	Failed Y/N/C C = Cracked	%Failure for 400 cycles	# of Cycles for 25% Failure Rate
1	L	2	25	N	>100%	149
	R	2	70	N/A	0.07%	1790
2	L	1	21	N	>100%	100
	R	1	6	Y	>100%	5
3	L	1	19	C	>100%	76
	R	2	72	Y	0.06%	1869
4	L	2	67	N	0.12%	1564
	R	2	78	C	0.03%	2313

Using the updated N_f analysis, the failure observed in 2R and the cracking for joint 3L were expected. The lack of failure or cracking for joint 1L, and 3R's failure appear out of family; but both are the result of poor solder joint formation. 3R necks down across the thickness of the joint causing a stress concentration that likely failed in tension during the rapid temperature transitions. For 1L, the 1R solder joint opposite it did not form under the bar, allowing the bar to freely expand away from 1L and minimizing its cumulative damage. That leaves the 4R and 2L cases remaining as outliers. In 2L's case, the reason behind the apparent lack of cracking is indeterminate. Since 2R likely failed quickly

unloading 2L for all subsequent thermal cycles, 2L would have received less cumulative damage than the other joints. It is possible though that the Type 1 pad exhibiting the ASN-CP layer only did not degrade the solder joint strength. Based on its high calculated N_f (2313 for 25% failure), 4R should show the least amount of damage after the completed 400 thermal cycles. However, the large fracture evident in Figure 9 shows that this is not the case.

Detailed inspection of Figure 9 shows that the crack initiated at the interface between the bulk solder and the two interfacial layers which have formed on the bar. Recall that these are the thickened ASN-CP layer with the second interfacial layer of AuSn₄ intermetallic that formed during thermal cycling. The growth of the AuSn₄ intermetallic layer depleted the region directly adjacent to it of Sn, leaving a Pb-rich region which the crack propagated through. Thus the ASN-CP layer does potentially threaten the long term reliability of solder joints.

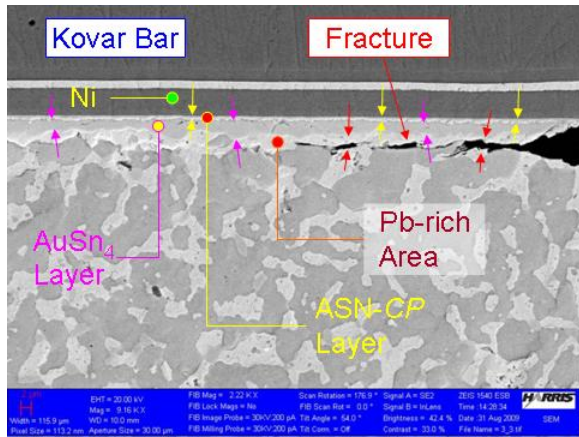


Figure 9: FE-SEM cross section image showing fracture adjacent to Type 2 pad ASN-CP layer secondary AuSn₄ intermetallic phase after 400 thermal cycles.

The weakening behavior of the formed *ASN-CP* layer and relating 2nd intermetallic layer on the thermal cycled solder joints is similar to that described in previous studies. Mei et al described the weakening of BGA solder joints which contained a small estimated weight percentage (0.1%) of Au for electroless Ni, immersion Au (ENIG) plated pads. Despite that small percentage, visible Au-Sn intermetallics were evident within the bulk of the solder ball interconnects which during thermal aging supposedly migrated back to the solder-pad interface creating a very thin Au-Sn₄ intermetallic layer (~1 μm thick) which showed poor adhesion in 4-point BGA bending tests [7]. The proposed mechanism behind the Au migration in this case was the Gibb's free energy reduction achieved by reacting the Au

with the Ni to form (Au, Ni)Sn₄ intermetallic phases [13]. Although the impact on the solder joint strength is similar, based on the presence of 2 separate Au containing layers and the minimal Ni content in the second layer growing over the ASN-CP layer, it appears that a different mechanism is driving the layer formation in this case. At a minimum there may be a different source for the Au that was incorporated into the ASN-CP layer and 2nd AuSn₄ intermetallic layer through thermal cycling.

By performing a diffusion distance prediction for the Au through the solder at 125°C for the duration of hot dwells (30 minutes * 400 cycles), it becomes clear that multiple Au sources are possible. Using the material properties described in [7], it is predicted that the Au would diffuse 1.47 mm and 0.62 mm within the Pb and Sn phases of the solder, respectively. Since the solder pads are 0.5 mm wide, the Au could easily travel across the thickness of the solder joint or reach the pad area from the solder/Au boundary at the edge of the pad (see Figure 5). The lack of detectable Au in the bulk solder and the appearance of the AuSn₄ intermetallic growth only adjacent to the ASN-CP layer, suggest that the Au source may also be the ASN-CP layer itself. However, detection of Au in the layer after thermal cycling in the Type 1 pads that were supposedly Au free prior to thermal cycling indicates that both sources are possible.

Understanding the kinetics behind the layer formation is important in ensuring that its effects can be fully compensated for in all designs. However, it may not be needed to develop a working double tin and wick process that can be used effectively in sensitive BGA, LCC and other limited-strain-relief components design applications. Accounting for the pad geometry to minimize the amount of Au present on the pads is likely the most critical addition to the current process parameters. J-STD-001D currently only requires Au removal on the pad receiving solder [5]. Thus the typical methodology is to use the same solder stencil that is used for component attach which only applies solder where final solder joints are made. This will leave the solder/Au interface in close proximity to the component solder joint and depending on the circuitry allow for the likely formation of the ASN-CP layer. As the results of this testing indicate, simply relying on double tinning of PCBs with thick Au in this fashion may not be sufficient to fully remove Au in highly stressed locations and prevent the formation of reliable solder joints. One possible implementation would be to create a tinning solder stencil which allows solder to be applied to adjacent circuitry in the area of solder interconnects where the design allows. This would ensure the proper balance between solder volume

added and the amount of Au to be dissolved on the surface and increase the distance to the Au/solder interface minimizing diffusion effects. The best use of this information is to use the ASN-CP layer as a process indicator when developing the Au removal process. In the critical locations, the process should strive to remove the Au both from the bulk solder and the interfacial layer.

V. Conclusions

Within this work it has been shown that double tin and wicking on pads plated with thick Au ($\sim 3.5 \mu\text{m}$) over Ni can result in the formation of an extremely thin ($\sim 200 \text{ nm}$) continuous layer containing Au, Sn, and Ni, and sometimes Cu and/or Pb, referred to as the ASN-CP layer, at the interface between Sn-Pb eutectic solder and a Ni-plated pad or component on both sides of the final solder joint. Changing the tinning conditions from room temperature, preheated to 120°C , or using infrared reflow heating did little to affect the layer formation. The ASN-CP layer formation was most dependent on the pad geometry with the layer formation occurring most often on traces with wider circuits exiting the pad areas. Thermal cycling of the solder joints containing the ASN-CP layer result in thickening of the layer and the growth of a secondary AuSn_4 intermetallic layer which did have an adverse effect on the long term reliability of solder joints.

VI. Acknowledgement

The authors wish to thank Harris Corporation for continued support of this work.

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