

A Design Rule for 3D TSV Technology to Avoid Radial Cracking in Silicon Interposer

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Abstract:

Three dimensional through-silicon via (3D TSV) technology emerges due to the requirement of high performance, low cost and small form factor in the three dimensional packaging technology. The typical TSV structure is a thin silicon wafer drilled with through hole, the inside wall of the hole is plated with dielectric SiO_2 and diffusion barrier such as Ta, and then the hole is filled by Cu or W as the conductor. During fabrication, testing and service, the packages with TSV structures usually undergo temperature excursion. When the operation temperature is higher than stress-free temperature, the expansion of metal via will induces tensile stresses in circumferential direction in silicon interposer due to the mismatch of coefficient of thermal expansion. The tensile stress could drive the microcracks within the SiO_2 and silicon to initiate and finally break the silicon interposer by radial cracking. In the current paper, a design rule is established based on fracture mechanics to avoid such failure, including the parameters such as via radius, flaw size, Young's modulus, coefficient of thermal expansion, and fracture toughness. The explicit expression in mathematical form makes such a rule easily implemented in 3D TSV design.

Key words: TSV, fracture, CTE mismatch, design rule

1 Introduction

Three dimensional through-silicon via (3D TSV) technology emerges due to the requirement of high performance, low cost and small form factor in the three dimensional packaging technology [1-3]. Without changing the size of a package, the multiple

functional modules such as processors, memories, logics are stacked and interconnected by TSV. The typical TSV structure is a thin silicon wafer drilled with through holes by either etching or laser drilling, the inside wall of the hole is deposited with dielectric SiO_2 and diffusion barrier such as Ta, TaN or TiN, and then the hole is filled by Cu or W as the conductor [4-13]. Due to the large mismatch in coefficient of thermal expansion (CTE) of different materials used in TSV structure, stresses generated near TSV could lead to many thermomechanical reliability issues [15-23]. One of those is that a tensile hoop stress in silicon can arise around via in processing, testing, and service of microelectronic packages, as long as there is a temperature excursion from the stress free temperature. The tensile hoop stress can drive the microcracks within the SiO_2 and/or silicon to initiate and finally break the silicon interposer by radial cracking [24-26]. This paper formulates an analytical method to analyze this phenomenon and establish a design rule to avert radial cracking.

2 Model and Formulation

Consider a typical 3D TSV structure. The inner via is Cu or W, the outer material is silicon, and in between are the thin dielectric and barrier layers. Since the thickness of dielectric and barrier layers is typically much smaller than the via diameter, and the CTE mismatch is mainly due to via and silicon, we simplify the model to be a two-layer cylindrical model as in Fig.1(a). The via radius is R , and the silicon interposer is assumed to be infinite. Symbols E , ν and α are the Young's modulus, Poisson's ratio and CTE, respectively. The subscripts 1 and 2 refer to via and silicon, respectively. For simplicity, all the material properties listed in Table I are assumed to be linear, elastic, isotropic, homogenous and independent of temperature change.

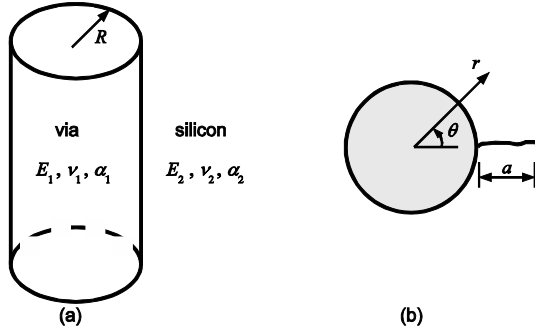


Figure 1. (a) The schematics of 3D TSV structure. (b) Axial symmetrical plain strain problem with an arbitrary crack emanating from the via.

Table 1: Materials properties.

	Modulus E (GPa)	Poisson's ratio ν	Fracture toughness K_{Ic} (MPa $\sqrt{m}$)	CTE α ($10^{-6}/K$)
Cu	130.6	0.34	-	17
W	411	0.28	-	4.5
Si	129.1	0.28	0.9	2.6
SiO ₂	70	0.17	0.7	0.5

Since the via height is typically larger than the via diameter, it is easier to consider a plain strain problem. The stress state based on such a model is approximately that in the middle plane across the TSV structure, at which the hoop stress is largest. Let (r, θ) be the in-plane polar coordinates sitting in the center of the circular via and the z direction pointing out the plane. For such an axial symmetric problem under plain strain condition, the stress field only depends on r . The details of governing equation, boundary conditions and solutions are given in Appendix. Here, the main concern is the hoop stress in silicon interposer.

The thermal mismatch strain ε_T is given by

$$\varepsilon_T = (\alpha_1 - \alpha_2)(T - T_0), \quad (1)$$

where T is the temperature in operation and T_0 is the stress-free temperature at which the via is filled by Cu or W and annealed. The hoop stress in silicon is

$$\sigma_{\theta\theta}^{(2)} = E^* \varepsilon_T \left(\frac{R}{r}\right)^2, \quad (2)$$

where

$$E^* = \frac{E_1 E_2 (1 + \nu_1)}{E_1 (1 + \nu_2) + E_2 (1 + \nu_1) (1 - 2\nu_1)}. \quad (3)$$

If the via and silicon have similar elastic properties, i.e., $E_1 = E_2 = E$ and $\nu_1 = \nu_2 = \nu$, then

$$E^* = \frac{E}{2(1-\nu)}. \quad (4)$$

Consider an arbitrary radial crack in silicon emanating from the via with size a , as in Fig. 1(b) [24-26]. The stress intensity factor at the advancing crack tip is [27]

$$K = 2E^* \varepsilon_T \sqrt{R} \cdot f\left(\frac{a}{R}\right), \quad (5)$$

where the dimensionless function $f\left(\frac{a}{R}\right)$ is

$$f\left(\frac{a}{R}\right) = \left(\frac{\pi}{8}\right)^{\frac{1}{2}} \left(\frac{a}{R}\right)^{\frac{1}{2}} \left(1 + \frac{a}{R}\right)^{-\frac{3}{2}}. \quad (6)$$

Based on linear elastic fracture mechanics, the critical condition to avoid the radial crack is to satisfy $K < K_{Ic}$, where K_{Ic} is the fracture toughness of silicon. Integrating Eqs.(1)-(6) into the above inequality, the design rule to avert radial cracking in TSV structure can be implemented as

$$X < X_c, \quad (7)$$

where

$$X = (T - T_0) \sqrt{R} \cdot f\left(\frac{a}{R}\right) \quad (8)$$

is the crack driving force, and

$$X_c = \frac{K_{Ic}}{2E^*(\alpha_1 - \alpha_2)} \quad (9)$$

is the fracture resistance of TSV structure. The X number only depends on via radius, processing and operation condition, while the X_c number purely depends on material properties of via and silicon. For example, for Cu-filled TSV structure, $X_c =$

$0.31 \text{ K}\sqrt{\text{m}}$, and for W-filled TSV structure, $X_c = 2.09 \text{ K}\sqrt{\text{m}}$.

As we know, it is always hard to control the flaws and hard to know the actual flaw size distribution, so is the value of $f(\frac{a}{R})$. But the function $f(\frac{a}{R})$ is of maximum value of 0.24 at $a/R = 0.5$. So in design, the worst case scenario can be implemented as:

$$X = 0.24(T - T_0)\sqrt{R} \quad (10)$$

3 Application and Results

Let us consider several examples where the TSV structure is designed into a microelectronic package.

Laser drilling is one popular method to form through hole in silicon due to its low cost, time efficiency and layout flexibility, but induced a damaged zone in silicon around the hole with large cracks [24]. The typical crack size could vary from several microns to tens of microns, comparable with the via size [25, 26]. So in the following, we will use Eq.(10) to estimate the X number.

Pick a typical value for via radius, e.g. $100 \mu\text{m}$. Consider that the TSV is filled with Cu by electroplating at room temperature. If such a structure is used for CPU or GPU processors, during normal operation of a high performance workstation, the temperature in silicon can be as high as 82°C if the junction temperature is set to be 85°C . In this situation, the X number is $0.14 \text{ K}\sqrt{\text{m}}$, smaller than the critical X_c number $0.31 \text{ K}\sqrt{\text{m}}$. We are relieved.

If this Cu-filled TSV structure undergoes high temperature process during assembly flow, e.g. reflow of C4 solder bumps or BGA balls, the operation peak temperature can be as high as 250°C . Now, the X number is $0.54 \text{ K}\sqrt{\text{m}}$, larger than the critical X_c . The radial cracking is expected now.

Another example: consider the electronics under the hood of automobiles. High temperature and high power electronics are required for normal operation of the vehicles. Pick a typical underhood temperature 165°C into Eq.(10), $X = 0.34 \text{ K}\sqrt{\text{m}} > X_c$ for Cu-filled TSV structure. The radial cracking is also a reliability concern.

The mitigation methods are obvious from Eq.(8) to (10):

(1). Minimizing the flaw size a is always beneficial. Not only smaller flaw size induces smaller X number, but also makes X number independent of via size. If $a \ll R$, then Eq.(8) can be simplified as:

$$X = 0.63(T - T_0)\sqrt{a} \quad (11)$$

Then in design, the via size is not a concern in the design as long as the radial cracking is concerned.

(2). If the flaw size a is hard to minimize, the risk can be mitigated by reducing the via size R .

(3). Minimizing the temperature excursion $T - T_0$ is an effective way to mitigate the radial cracking.

(4). Of course, increasing X_c is also a way. For example, W-filled TSV is of high $X_c = 2.09 \text{ K}\sqrt{\text{m}}$. Even if Cu is preferred as conductor, but different material selection paves a way to solve the issue if all other methods do not work under some circumstances.

Eq.(7) has to be followed for all manufacturing steps, assembly processes and use conditions.

4 Discussions

The CTE mismatch generates not only tensile hoop stress, but also axial stress in z direction. If the axial stress in silicon is high enough, it could fracture the silicon interposer by horizontal cracking.

The stress in silicon in z direction is zero when the TSV is an isolated one or the pitch is much larger than the via diameter. When the pitch is comparable to via diameter, $\sigma_{zz}^{(2)}$ increases with via density, but usually still smaller than $\sigma_{\theta\theta}^{(2)}$ as long as the via density is less than 60% [27]. Hence, when the radial cracking is suppressed, so is the horizontal cracking.

In some of TSV designs, a thick polymer dielectric is adopted. For such a case, the similar methodology can be used to solve the hoop stresses in silicon then obtain the failure criterion as Eq.(7). The algebra is messy but straight forward. The purpose of the simple analytical solution in this paper

is not giving an accurate calculation for more complex TSV structures, but it provides a clear design rule to follow. Compared to earlier studies on TSV, especially relying on finite element analysis heavily [15-23], the current analytical model provides accuracy and fidelity in addition to its simplicity.

The design rule proposed here to avoid radial cracking in silicon interposer is similar to that by Blech [28] to avoid electromigration in Al or Cu conductor lines in interconnects.

5 Conclusion

In conclusion, a design rule is developed to avoid radial and horizontal cracking in silicon interposer. The method to develop the design rule and the explicit form of the design rule can be widely used to ensure reliability of 3D through silicon via technology.

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7 Appendix

For an axis symmetrical problem under plain strain condition as in Figure 1(b), the displacement field only depends on r and only u_r exists. Finally the governing equation becomes

$$\frac{d}{dr} \left(\frac{1}{r} \frac{\partial(r u_r)}{\partial r} \right) = 0. \quad (\text{A.1})$$

The general solution to the homogeneous Eq.(A.1) is

$$u_r = Ar + Br^{-1}. \quad (\text{A.2})$$

The coefficients A 's and B 's are to be determined by the following boundary conditions:

1. u_r is finite when $r \rightarrow 0$ and $r \rightarrow \infty$.
2. At interface, i.e. $r = R$, the displacement and traction are continuous.

Finally, the displacement fields in both via and silicon are

$$u_r^{(1)} = \frac{E^* \varepsilon_T}{E_2/(1+\nu_2)} r, \quad (\text{A.3})$$

$$u_r^{(2)} = \frac{E^* \varepsilon_T}{E_2/(1+\nu_2)} \frac{R^2}{r}. \quad (\text{A.4})$$

And strains are

$$\varepsilon_{rr}^{(1)} = \varepsilon_{\theta\theta}^{(1)} = \frac{E^* \varepsilon_T}{E_2/(1+\nu_2)}, \quad (\text{A.5})$$

$$\varepsilon_{rr}^{(2)} = -\varepsilon_{\theta\theta}^{(2)} = -\frac{E^* \varepsilon_T}{E_2/(1+\nu_2)} \left(\frac{R}{r} \right)^2. \quad (\text{A.6})$$

And stresses are

$$\sigma_{rr}^{(1)} = \sigma_{\theta\theta}^{(1)} = -E^* \varepsilon_T, \quad (\text{A.7})$$

$$\sigma_{zz}^{(1)} = -(2\nu_1 E^* + E_1) \varepsilon_T, \quad (\text{A.8})$$

$$\sigma_{rr}^{(2)} = -\sigma_{\theta\theta}^{(2)} = -E^* \varepsilon_T \left(\frac{R}{r} \right)^2. \quad (\text{A.9})$$

where ε_T and E^* are as defined in Eqs.(1) and (3).

And all other components are zero.