

Investigation of SiC Power Module Requirements for Smart Grid Applications

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Abstract

Post-Silicon power devices, specifically SiC and GaN, provide attributes such as high switching speed, high voltage withstand and high temperature operation. These provide attractive performance characteristics. However, other attributes, such as high Young's modulus and difficult metallization present packaging challenges that can directly affect long-term packaging reliability. As with all electro-physical systems, the interdependencies of electrical, mechanical and thermal forces must be co-investigated during physical development and fabrication to assure suitable reliability. This study is a first look at critical issues that affect general high voltage (>10kV), high temperature (>200°C), power module packaging applicable to next generation approaches for Future Renewable Electric Energy Delivery and Management Systems. The initial assessments establish electrical and thermal stress boundaries and initial requirements on materials and material characteristics. This paper is a survey of issues for the early stages of the program focusing on very high electric field stresses and time-varying high current densities

I. INTRODUCTION

The physical embodiment of a power electronic circuit and system concurrently manages a multitude of energies; of specific focus are electric, magnetic, mechanical and thermal energies. It is not reasonable that development of a power electronic circuit be considered solely electrical. However, the primary driver is, and remains, electrical energy, even though other forms for sensing, actuation and isolation are included.

Electrical design drives density and efficiency, which drives the mechanical and thermal issues, respectively. These summarily drive reliability, specifically the chemical and mechanical effects, at interfaces. An early stage evaluation must investigate both spatial and time-varying effects in for potential physical circuit embodiments.

This paper focuses on immediate electrical issues of voltage and current to establish design guidelines for development of a Multi-Chip Power Module for Test Development (MCPM-TD) in support of the FREEDM Solid State Transformer (SST) development. The development of the guidelines sets a methodology and boundary for further developments generalized to a broader class of applications as the program progresses to post-silicon

devices.

The initial SST MCPM-TD is designed for 3,800V and <5A, using silicon IGBT devices to be used in both hard switching and resonant electrical topologies. The circuit topology must be considered to bound time-varying (dt) requirements of the packaging. The power silicon semiconductor devices are rated for 6,500V and 25A; well beyond the test module application requirements.

II. PACKAGING DEVELOPMENT

A. Research Framework for Packaging

A systematic framework exists for structuring technology development in electronic energy packaging [1]. The framework is set into a three-dimensional matrix that comprehensively identifies the technical challenges for investigation. The Electronic Energy Packaging Framework (EPPF) extends the generally accepted "levels-of-packaging" [2] used in microelectronics to include much higher power applications. The classic levels are

Level-0: In-die semiconductor integration

Level-1: Die in package (i.e. component packaging)

Level-2: Package on board (i.e. board-level packaging)

Level-3: Board in Rack (i.e. box-level packaging)

The packaging levels can be extended further for power and begins to develop a packaging philosophy toward “Board-level to Floor-level” packaging. Extended levels are:

Level-4: Rack in cabinet (i.e. systems-level packaging)

Level-5: Cabinet in room

Level-6: Room in Building

Level-7: Building in community

Why are “Levels” important? Each level has a requirement to interface to the lower level, i.e. each level can be considered a packaging system composed of sub-systems. The interfaces between each level are, as previously mentioned, the area most impacting reliability, and is considered the second dimension of the Electronics Energy Packaging Framework (EPPF). Elimination and reduction of levels increases reliability, almost always increases density and improves performance.

The third dimension of the EPPF used to systematically and comprehensively identify research requirements is the observations that, again as previously mentioned, multiple forms of energy flow through the packaging. Flowing through a level and across an interface to the next sublevel, are electrical, mechanical, thermal, etc. energies.

Each energy form has an optimum material for energy conduction and an associated materials-processing technology. As excursions to higher temperatures or higher voltages are needed, the EPPF can be used to comprehensively identify the technical challenges and guide research into new materials and processes to support advanced packaging.

An example of the applicability of this framework is to qualitatively assess voltage stress as may occur in a MCPM or in a Utility company switchyard. The natural challenge is managing high electric fields (dV/dx) between apparatus (components), interconnecting wires, bus bars, and cabling.

The same dv/dx problem exists in, e.g. a copper-on-ceramic (direct bonded copper, DBC) MCPM for silicon IGBTs, between components and interconnects. Techniques, such as application of silicone gels, are used to eliminate the effects of dirt, humidity and reduction of partial discharges.

High dV/dx applies to the switchyard, the MCPM and to other “levels,” e.g. board-level packaging. Hence, the author has coined the phrase “board-level to floor-level packaging” to exemplify the parallels that exist between all levels of packaging from Level-0 to Level-7. The EPPF is robust to provide detailed and comprehensive identification of technical challenges to guide developing research needs.

This framework was used in this work to identify requirements for the MCPM-TD. Though this paper

focuses only on electrical voltage and current issues in the module.

B. Operational Environment

One of the component drivers in the FREEDM System is the type of power semiconductor device, i.e. post-silicon device. Devices and the application set a thermal boundary in selection of packaging materials. Recent industrial advances in SiC semiconductor processing have developed junction and dielectric isolated devices. Under present consensus dielectric devices would be limited to 250°C. This coincides well with a division in organic v. inorganic packaging materials at 300°C. Module development for <250°C opens opportunities for research into highly reliable “high temperature” modules using organic-based packaging, which can also provide lower cost systems. For higher temperature operation, metalized ceramic-based packaging would be developed. However, with the continual evolution of nano-based materials, newer packaging approaches may come available.

Applications drive both the components and topologies. The focus is on two primary application classifications: inverters and Solid-State Power Controllers (SSPCs). The characteristics in the SSPC classification also include Solid-State Circuit Breakers (SSCBs) and solid-state Fault Interruption Devices (FIDs).

Packaging requirements for inverters are for high performance during steady state operation with occasional excursions for fault management. Requirements for SSPCs are inherently transient with operation at very high gradients occurring in time (dt) and spatially ($dtdx$) within the module. The SSPC may see a $10X$ current change or follow an aggressive I^2t protection current profile. The SSPC has low duty-cycle operational requirements, but very high operational reliability requirements. Fault management and coordination in a power system is a primary contributory area for solid-state power switching.

CI. Solid State Transformer in FREEDM System

The FREEDM project aims at establishing a novel generation of smart power grid infrastructure which includes secured communication, distributed grid intelligence, high-frequency and high-voltage power conversion, and distributed energy storage devices (Fig. 1). On the load side, the Distributed Renewable Energy Resources (DRERs) and Distributed Energy Storage Devices (DESDs) are connected to FREEDM system through 120V and 480V class Intelligent Energy Management (IEM) subsystems. Plus, a high power IEM subsystem is used in main grid connection. The IEM which consists of a Solid State Transformer (SST) and an intelligent controller has bi-directional energy flow capability and can isolate

fault current from the user side. And the faults in the 12kV system will be isolated by the Intelligent Fault Management (IFM) subsystems. The IEMs and IFMs are embedded with Distributed Grid Intelligence (DGI) software, and can communicate with each other through a Reliable and Secured Communication (RSC) network. The SiC semiconductor devices will be applied into FREEDM systems in order to meet the critical high voltage, high frequency requirements, and ultimately the 1MW demonstration system of this so-called “energy internet” will be established [3].

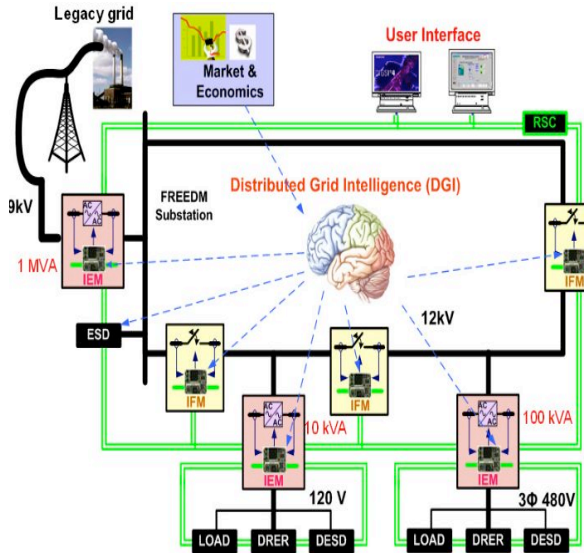


Figure 1. FREEDM System, the Internet of Energy (IEM: Intelligent Energy Management, IFM: Intelligent Fault Management, DRER: Distributed Renewable Energy Resource, DESD: Distributed Energy Storage Device)

Being a key component in the frame of FREEDM, the SST uses advanced wide-band gap semiconductor devices such as SiC IGBTs and a much higher frequency (10kHz) to attain a significant size and weight reduction. Comparing to conventional 60Hz electromagnetic transformers, 10kHz SSTs with the same capability can reduce the weight and size to its 1/3 [4]. Besides, the reduced requirement for copper and laminated steel makes SST even more competitive. The SST prototype here consists of a cascaded high voltage high frequency AC/DC rectifier that converts 7.2kVac to three 3.8kV DC buses; then this voltage is stepped down to 400V by a DC-DC converter; at last a voltage source inverter(VSI) is used to converted the voltage to 240/120V 60Hz AC (Fig. 2).

C2. Identification of MCPM-TD Electrical Issues

A drawing of the MCPM-TD, representing relative size and layout, including pin-out, is shown in Fig. 3.

From the framework, the MCPM-TD, as a finished module, appears as a packaged component and ready for board mounting. Here the electrical path and interface is evaluated for high dV/dx and current carrying capabilities (dI/dt) of the pins (interface). Several issues are addressed: (1) pin diameter to avoid corona in free air; (2) sharp geometric transitions, e.g. at the pin (cylinder) edge; (3) pin conduction area for high dI/dt ; and (4) creepage and clearance between pins. The later depends strongly on surface condition of the pathway between the pins, and pins to case. These issues can be resolved with judicious evaluation of the internal module layout, provided certain criteria remain the same. If a gel is

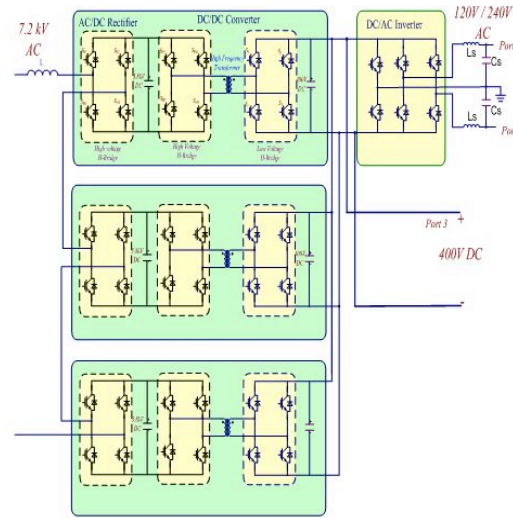


Figure 2. Schematic of SST

used internal to the module for voltage stress management, then the next higher level must re-evaluate the stress in air.

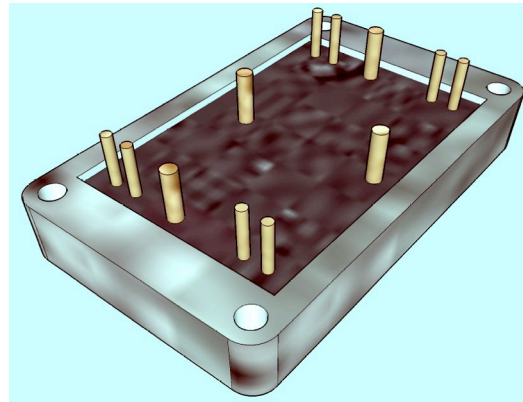


Figure 3. MCPM-TD pin layout and relative proportions

A drawing of the MCPM-TD circuit metallization pattern with dimensions is shown in Fig. 4. Again, the electrical evaluations are for voltage stress

gradients and current carrying capacity under fast electrical transitions. To better assess the stresses in the layout an FEA is performed and discussed in the following sections.

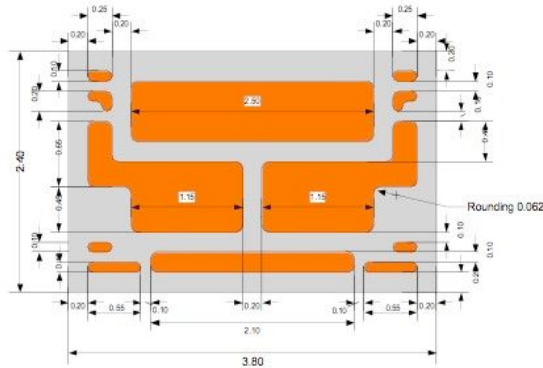


Figure 4. MCPM-TD metallization layout and dimensions

C3. Capacitance Effect in Package

The critical parts of any DC/DC converter are the switching power poles [5]. In this layout the switching power poles attach onto two large copper pads in the center (Fig. 4). Equivalent capacitances are formed laterally between two metallization edges at the surface, between copper surface traces, but coupled through a copper pad under the ceramic, and between the traces and case or ground, see Fig. 5. Capacitance can be calculated by:

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \quad (\text{Eq.1})$$

where ϵ_0 and ϵ_r are the electric constant and relative static permittivity; A is the overlapping surface area; d is the separation between the conducting sheets. Fringing effects can be included by adjusting the area with a geometric mean; but is assumed negligible here.

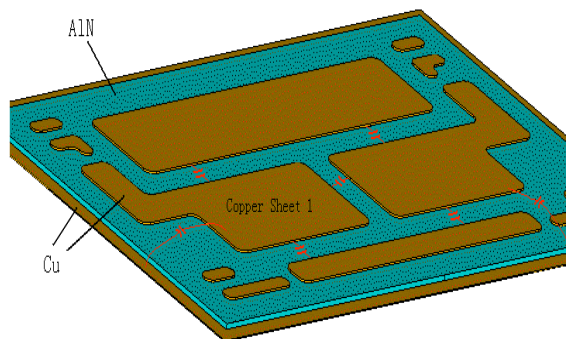


Figure 5. Capacitance Distribution on Board

The capacitance between two metallization edges at the surface is negligible due to the small overlapping areas and the relatively big separation, but the capacitance between the copper traces and the

copper pad is significant. For example, the area of copper sheet 1 (Fig. 5) is 656 mm^2 , and the thickness of the AlN substrate is 0.635 mm . According to Eq.1, the capacitance from trace to the bottom copper pad is 82.3 pF . The frequency for this H-bridge converter is 3 kHz or 0.33 ms . Under hard switching, the dt per cycle from 1% to 5% of the total switching period depending on the speed of the device. Thus, for example, repetitive 3.8 kV switching at 1% period yields a current through the AlN substrate of 94 mA during each switching occurrence. The stored energy in the substrate capacitance per switching cycle is 0.6 mJ with a power loss of 7.1 W for the total converter. At 12 kV the loss is 71 Watts . This energy loss will dissipate as heat, so a qualified heat sink or heat dissipation design is required. The substrate currents are shown in Table 1

Table 1. Substrate current in mA for varied switching times (dt)

Voltage (<i>dt</i>)	V _{bus} =3,800V	V _{bis} = 12kV
3.3μs	93.8	296
8.3μs	37.5	118
16.7μs	18.8	59.2

III. MCPM-TD MODELING AND RESULTS

A simple package layout shown in Fig.4 allows analysis of two critical features: high electric field gradients at sharp outside corners and high currents (i.e. current crowding) at interconnect corners. This provides a way to evaluate materials and topologies under high stress gradients.

A. Electric Field Evaluation of Pins

The surface electric field gradient increases as the pin diameter decreases. Though the voltages are relatively low in this Test Development, the higher voltages of the FREEDM program can reach $12kV$ and with overvoltage, lighting and transients, much higher voltage will need to be considered in the packaging layout. For two cylindrical conductors in close proximity, the critical disruptive voltage [6] is,

$$E_0 = g_0 \delta^{2/3} r m \log_e D / r \quad (\text{Eq. 2})$$

where g_0 is critical gradient in kV/cm ($g_0=21.1\text{ kV/cm}$ is a commonly accepted number in power systems for open air.)

r is radius of conductor in centimeters

D is the distance in centimeters between conductor
 m is surface factor (common value is 1 for solid

surface)

$$\delta \text{ is air density factor } \delta = 17.9b/459 + ^\circ F$$

where b=barometric pressure in inches of mercury

The present application of the MCPM-TD is energized to $3.8kV$. The worst case dimensions for

pin diameter is 2.5 mm and spacing between top-center and bottom-center pins is 38 mm , as shown in Fig. 2. From Eq. 2, $E_o = 9.1\text{ kV}$, providing a $> 2:1$ safety margin for the pins protruding into air. Extending the capability of the package to the full 6.5 kV rating of the power semiconductors will require different pin diameters and spacing with an adequate safety margin.

B. Electric Field Evaluation of Layout

Initial electric field analyses are performed by an FEA evaluating the static electric field potentials, and provide quantitative gradients for the layout shown in Fig. 4. The circuit operates at 3.8 kV , functions as a typical H-bridge and has two areas of concern: fields gradients interconnect-to-ground (case) and at field concentration points (edges and outer radii) under worst case operating conditions.

For the MCPM-TD, all major interconnects have 5.1 mm separations with corner curvature radii of 1.6 mm . The metallization is copper on AlN ceramic with no surface coating. A 2-D FEA is performed using ANSYS. Only the surface fields across the ceramic are considered. Gradients from interconnect edge through the ceramic to a backside ground plane are not considered. Typical AlN thicknesses are 0.6 mm with a breakdown value of about 29.1 kV/mm (739 V/mil) [7]. This gives an absolute value of 17.5 kV , well beyond the design requirements for this project.

The AlN surface is considered smooth, i.e. no surface roughness is considered during the initial evaluation. Surface roughness includes microscopic spires and peaks, which act as electric field concentrators. Conversely, microscopic craters act as voids that trap gas during application of a coating. Voids support *partial discharge* (PD) aging of coating materials. Hence, surface roughness and, in a similar way, surface particle contamination, enhance localized field gradients and reduce high voltage withstand capability of the MCPM. In the final assembly a surface roughness is specified and a silicone gel coating applied to make the module voltage withstand value predictable [8].

C. E-Field Gradient Results

The electric field distributions for the MCPM-TD (Fig. 4) are shown in the following figures for two modes of circuit operation and with variations of the curvature of the interconnect corner geometries.

When all IGBTs are turned off, the maximum electric field at the corners with original trace curvatures of 1.59 mm (0.0625 in) has a maximum field located in the top left at 1.40 kV/mm as shown in Fig. 6. After changes in the corner geometry radius to 5.08 mm (0.2 in) the maximum electric field decreases to 1.03 kV/mm as shown in Fig. 7. Not shown are any substrate edge fields. Care is needed during final assembly that the module frame is offset

further, and a high voltage, high temperature material, such as high temperature plastic or ceramic is used.

When two IGBTs are conducting, the maximum electric fields are as before, but with different positions, example shown in Fig. 8. Knowing the circuit operation is important to identify worst-case conduction patterns that guide design requirements. The maximum electric field is a critical factor in determining the reliability of MCPMs. For example, higher electric field can accelerate aging of silicone gel fillers.

D. Electrical Current Restrictions

Higher the frequency, lesser is the annular cross-section through which current in a trace can flow. This “skin effect” is usually considered to have an exponential distribution. However, this is only when the trace thickness, t , is “infinitely” thick. In power circuits the dimensions are often comparable and infinitely thick cannot be used.

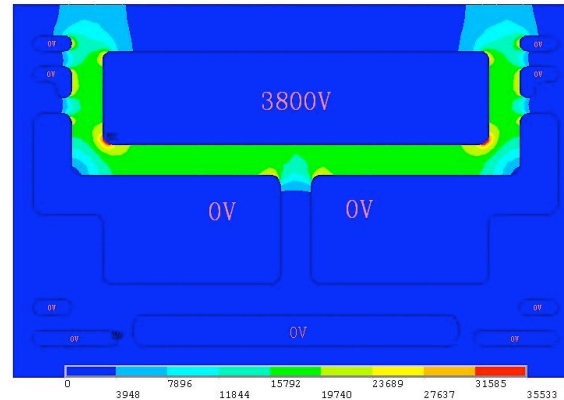


Figure 6. All switches are off with original curvature. Peak field is 1.40 kV/mm (at the dark red corner points)

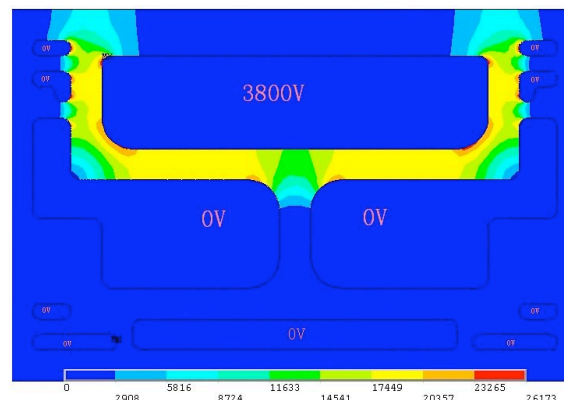


Figure 7. All switches are off and traces modified for less curvature. Peak field is 1.03 kV/mm

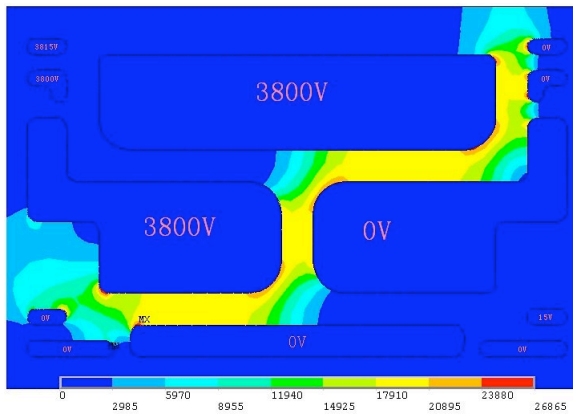


Figure 8. Diagonal switches of the H-bridge are conducting. Peak values are as before.

Figure 9 shows a standard aluminum conductor with dimensions $1\text{ mm} \times 0.5\text{ mm}$. Aluminum has a conductivity $\sigma = 3.77 \cdot 10^7\text{ S/m}$; copper the value of $59.6 \times 10^6\text{ S/m}$. When a current of 2.68 MHz flows in the cross-section, the current in the conductor experiences confinement with a skin depth, δ , of 0.05 mm of the outer surfaces.

The FEA uses COMSOL to solve the complex-valued Helmholtz equation for the amplitude of the magnitude vector potential A . Specifically, the power loss is discerned to show the limitations on packaging traces of fast switching transitions from either resonant circuit operation or the Fourier components in hard switching.

Focus is on thermal gradients resulting from the current distributions as shown in Fig. 10. Here the wide trace surface shows hot spots when the $t=2\delta$.

Similar is the effect when the conductor thickness is reduced further. The total skin effect is a monotonic change in impedance with frequency. However, of most concern is the resistance and resulting resistive heating pattern. Shown in Fig. 11 is the change of resistance as the thickness to skin depth ratio changes. From previous investigations, a minimum in the resistance occurs when the $t = \pi\delta$.

For high voltage circuits the steady state currents are relatively low and traces can be relatively thin for power modules. However under fault and surge operation as may occur in solid state power controllers (circuit breakers) or evolving solid state transformers, the requirement of module operation requires layout designs to include very high current densities with very high transition times. Hence, an understanding of the magnitude of current crowding from skin effect is required.

IV. SUMMARY

A framework is introduced to identify critical topics for packaging in FREEDM Systems. This

paper focuses on electrical issues caused by high voltage and current gradients in a MultiChip Power Module, and specifically for a MCPM for Test Development (MCPM-TD). A FEA maps the electric fields of the MCPM-TD layout and provides guidance to layout revision. Also, introduced is the limitation, particularly in power modules, of skin effect when the skin depth is comparable to the interconnect thickness. High current gradients in thin conductors can cause thermal gradients and long-term degradation.

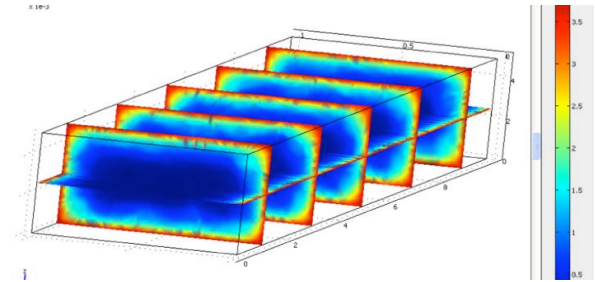


Figure 9. Current Density graph when $t = 10\delta$

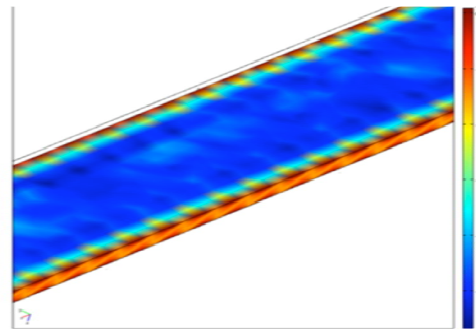


Figure 10. Surface Resistive Heating at thickness $t = 2\delta$

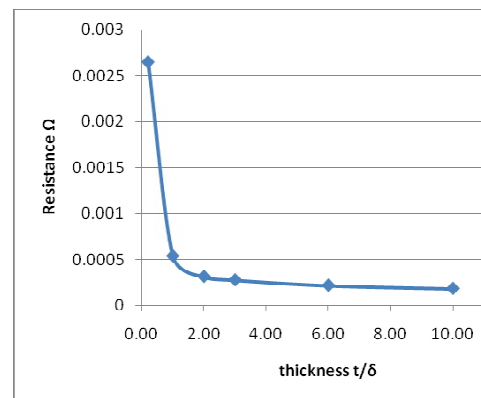


Figure 11. Resistance v. thickness per skin depth

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