

A Direct Fanning-out Packaging Technology using Cu Base Plate for Embedded Fine-pad-pitch LSI

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Abstract

As the wiring of LSI devices continues to shrink, the pitch of the bonding pads becomes smaller and smaller. This makes it more difficult to form connections using flip chip bumps and increases the cost of the interposer substrate. A direct fanning-out packaging technology, named as "SIRRIUS", gives a solution for this problem. The SIRRIUS package consists of a Cu base plate, a fine-pad-pitch embedded LSI chip, built-up resin layers, and multi-layer fanning-out wiring.

An experiment in which chips with 80- μ m-pitch, four rows of pads are embedded clarifies that using a low-viscosity resin and optimizing its thickness are important for achieving fine-pitch interconnects with high reliability. By measuring the displacement of the mounted chips and laser vias, and improving their position accuracy, the feasibility of fabricating the SIRRIUS package with a lump method is demonstrated. A 31-mm-square, 900-pin-count SIRRIUS package with three-layer wiring, 15 μ m wide, is successfully fabricated. Its total thickness is only 0.69 mm including the Cu plate. Evaluation of package-level and board-level reliability show no electrical failures or cracks after 600 and 1000 cycles, respectively.

Our "SIRRIUS" package has following features; 1) small package thickness, 2) low cost process due to directly connecting the Cu plating to fine-pitch LSI pads, and 3) high heat dissipation, low package warpage and high reliability, due to the rigid Cu plate. Therefore, the SIRRIUS package is an attractive approach to achieving thin and highly reliable fine-pad-pitch system LSI packages for replacing FCBGA packages.

Key words: LSI package, embedded active, Cu plate, and laser via

1. Introduction

A flip-chip ball grid array (FCBGA) package is now widely used for high-pin-count system LSIs, and many efforts have been made to continue to shrink the wiring pitch of both LSIs and interposer substrates. However, the shrink speed for LSIs is faster than that for the substrate, resulting in the increase in the interposer substrate cost. There is thus an urgent requirement for a package-level fine-pitch interconnect process to replace the conventional FCBGA process.

The use of embedded active components is a highly attractive approach because it results in thinner, higher density interconnects. There has thus been much research on embedded active technologies [1–5].

Our previous investigations [6,7] of embedded LSI packages with a Cu plate demonstrated that the package is much thinner than a

conventional FCBGA package, and it has low thermal resistance, comparable to that of an FCBGA package with a heat sink, and has an excellent warpage property due to the use of a Cu plate.

In the study reported here, we developed a direct fanning-out packaging process for fabricating embedded fine-pad-pitch LSI interconnects. This process, which we named as seamless interconnect for re-routing LSI using substrate technology (SIRRIUS), is a promising approach to solve the narrow pad-pitch connection problem. The "seamless" means that the chip and package-level wiring are directly connected by plated copper.

The concept of the package structure, its advantage in terms of fabrication cost, and the key process technologies for fabricating fine-pad-pitch connections are described. We also demonstrate the fabrication of a prototype package and its reliability.

2. Concept of SIRRIUS package

2.1 Structure and features

As illustrated in Fig. 1, our SIRRIUS package consists of a Cu base plate, a thinned LSI chip mounted on the plate, built-up resin layers, and multi-layer fanning-out wiring.

The SIRRIUS package has several attractive features. The package is much thinner than a conventional FCBGA package, due to the use of a thinned LSI chip and thin resin layers. The package has low thermal resistance due to the Cu plate attached to the back side of the chip. The package has small warpage and high reliability due to the rigidity of the Cu plate. The Cu direct connection allows a finer pitch layout for the pads of the embedded LSI and provides a lead-free package with lead-free BGA balls. Its fabrication cost should be lower than that of the conventional FCBGA package, because no specific materials for bonding, such as gold wire or solder balls, and for underfilling are necessary.

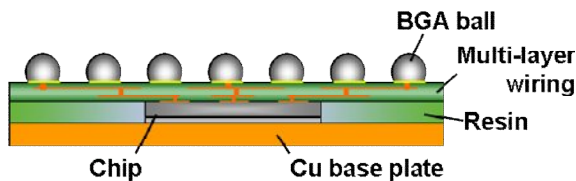


Fig. 1 Cross-sectional schematic view of SIRRIUS package

2.2 Fabrication process

As illustrated in Fig. 2, thinned LSI chips with adhesive film on the back side are mounted on a Cu base plate in the face-up position. In our experiments, we used 50- μm -thick chips and a 0.5-mm-thick Cu base plate. The base plate supports the thinned chips and works as built-in heat spreader after dicing.

The chips are embedded in a resin layer using a simple vacuum lamination process. As discussed later, selection of an appropriate resin is important for embedding the chips evenly.

Next, vias are formed to connect the interlayer wiring. The selection of the via formation process is also important. A metal post method was previously reported for the first via connection [6]. However, in our experiments, all vias are formed only using a laser process to reduce the total fabrication cost. A UV-YAG laser is adopted to form the fine-pitch vias.

After via formation, fanning-out wiring is fabricated on the resin layer using a semi-additive process. Multiple layers of fanning-out wiring are formed by repeating the resin lamination and Cu

plating processes as many times as needed. After solder-resist application, the fabricated packages are separated with the Cu plate, and BGA balls are attached.

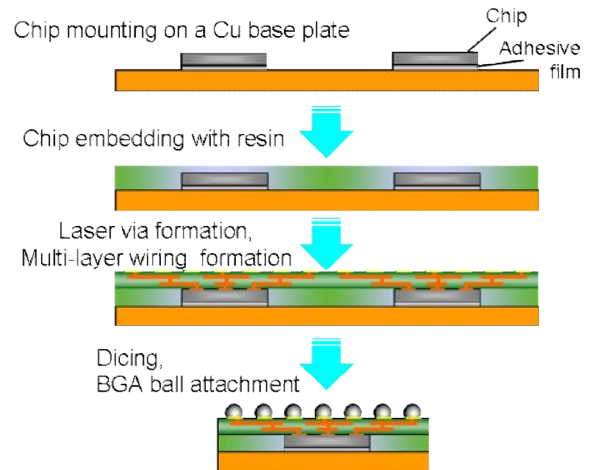


Fig. 2 Fabrication of direct fanning-out embedded chip package

2.3. Comparison with FCBGA package

The structures of a conventional FCBGA package and the SIRRIUS package are compared in Fig. 3. The SIRRIUS package is much thinner due to the thinned LSI chip and thin built-up resin layers [6].

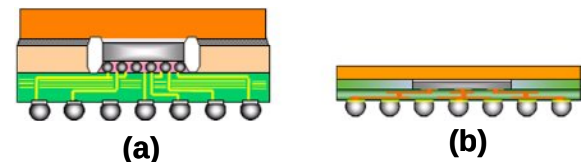


Fig. 3 (a) Conventional FCBGA package and (b) SIRRIUS package

The fabrication process flows for the FCBGA and SIRRIUS packages are compared in Fig. 4. Each process is divided into (a) mounting and connection steps and (b) wiring formation steps. The wiring formation step for the FCBGA package corresponds to the interposer fabrication process, and a 2-2-2 built-up substrate is selected as a test model.

For the mounting and connection process, the FCBGA package needs many steps, such as FC bump preparation, under-fill resin formation, lid and heat-sink attachments. On the other hand, the SIRRIUS package needs none of these steps, due to its direct connection structure. For the wiring formation process, the SIRRIUS package needs only three times of resin layer and wiring formation steps, because it has a finer interconnect pitch and a finer

wiring width than the interposer used for the FCBGA package [6,7]. As a result, the SIRRIUS package is much more cost effective, compared to the conventional FCBGA package.

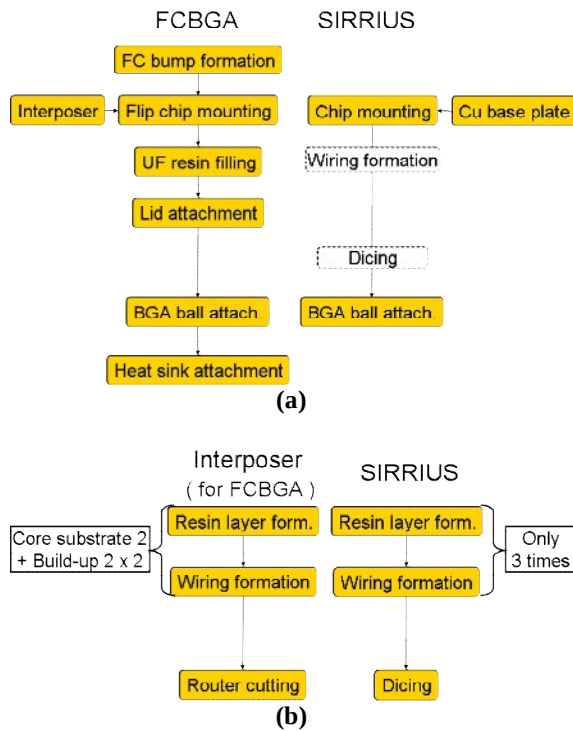


Fig. 4 (a) Mounting and connection steps and (b) wiring formation steps for FCBGA and SIRRIUS packages

3. Key process technologies for fine-pad-pitch LSI interconnects

3.1 Target structure and test chip

To investigate to fabricate interconnections for fine-pad-pith LSI, we use test chips with 8-mm-square, an 80- μm -pitch, four rows of pads, approximately 1200 pads in total. Adjacent two pads are connected by on-chip Cu wiring to form daisy chains after being embedded. The first vias which contact to chip pads are made by UV-YAG laser, as described before.

Figure 5 shows photographs of a chip and a magnified view of a corner. Although the pads are aligned in five rows, we used four rows in our experiments.

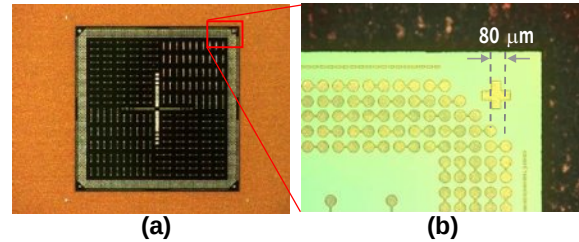


Fig. 5 Test chip used in the experiments: (a) mounted on Cu base plate, (b) magnified view of 80- μm -pitch-pads in chip corner

3.2 Resin selection and its thickness control

For achieving fine-pad-pitch interconnection and high-reliability, selection of an appropriate resin and optimization of its thickness are quite important. Generally, using a resin with high mechanical strength improves package reliability. However, resins with high mechanical strength usually have higher melt viscosity, making it more difficult to embed the LSI chips evenly.

Figure 6 shows a micrograph image of a chip embedded in high melt viscosity resin. There is an air void at the edge of the chip. Also, the resin surface near the chip edge is wavy because of the higher melt viscosity of the resin.

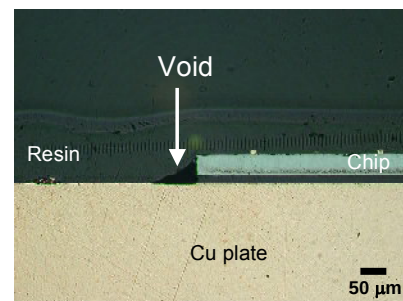


Fig. 6 Chip embedded in high melt viscosity resin

Figure 7 shows SEM photographs of the center and two edges of a chip embedded in epoxy resin with low melt viscosity. The resin lamination process is performed only one time. There are no air voids at the chip edges, despite the 50- μm step height. The surface of the resin is virtually flat even with an embedded chip. This result shows that it is unnecessary to make a cavity or a hole beforehand.

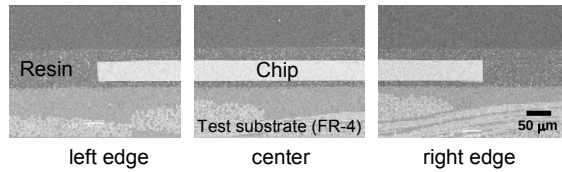


Fig. 7 Chip embedded in low melt viscosity resin

Optimizing the resin thickness is also important for achieving fine-pad-pitch interconnects with high reliability. Figure 8 shows the distribution of the resin thickness on the Cu plate. Before the vacuum lamination conditions are optimized, the resin near the package edges is thicker than that near the package center. Afterwards, the thickness of the resin is virtually uniform.

As a result of the appropriate resin selection and its thickness control, the good via connection is obtained after Cu plating, as shown in Fig. 9.

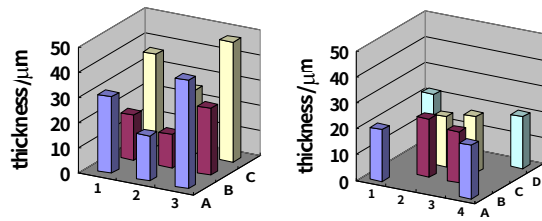


Fig. 8 Resin thickness distribution on Cu base plate: (a) before vacuum lamination conditions are optimized, (b) afterwards

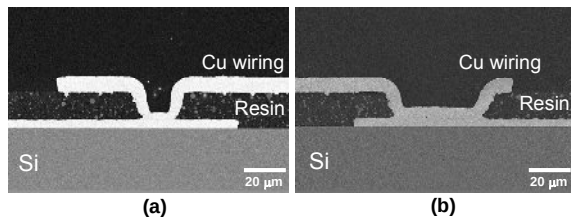


Fig. 9 Cross-sectional views of via connections after selecting appropriate resin and optimizing resin thickness: (a) 20-μm and (b) 50-μm-diameter vias

3.3 Wiring Design for 80-μm-pad-pitch Interconnects

As described before, the chips used in our experiments have 80-μm-pitch, four-row pads. Figure 10 shows the fanning-out wiring design. A monolayer drawing is preferable for fewer wiring layers; however, it is difficult to form wiring width narrower than 8 μm, and to form laser vias in diameter smaller

than 20 μm. We thus design a two-layer fanning-out layout for the four rows of pads. As shown in Fig. 11(b), a single wire has to pass between two 80-μm-pitch pads. This layout still requires the use of small vias, and the UV-YAG laser is necessary to form vias about 30 μm in diameter.

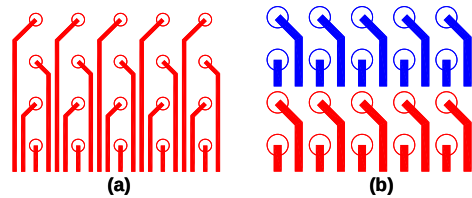


Fig. 10 Schematic of wiring design for four-row, 80-μm-pitch-pad interconnects:

(a) mono-layer drawing, (b) two-layer drawing (blue wiring is on the second layer)

3.4 Position measurement of mounted chip and laser vias

Accurate chip mounting and laser-via formation are also necessary for achieving fine-pad-pitch connections. To evaluate the accuracy, the displacement of the mounted chip from the designed position is measured. Figure 11 shows the displacement of the mounted chips. The error in the chip position is found to be smaller than 10 μm.

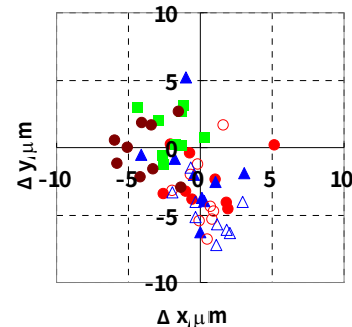


Fig. 11 Displacement of mounted chips (different marks correspond to different base plates)

Measuring the displacements of the laser vias is much more difficult, owing to their huge number. To measure the positions of all the vias on the Cu base plate, we need to select an appropriate vision measuring machine and use it under suitable measuring conditions.

Figure 12 shows the images on the vision measuring machine for laser vias on a whole chip and

single via. The diameter of the via is approximately 30 μm . Under suitable visioning conditions, the vias stand out as solid black circles. This enables them to be detected and their positions to be measured automatically.

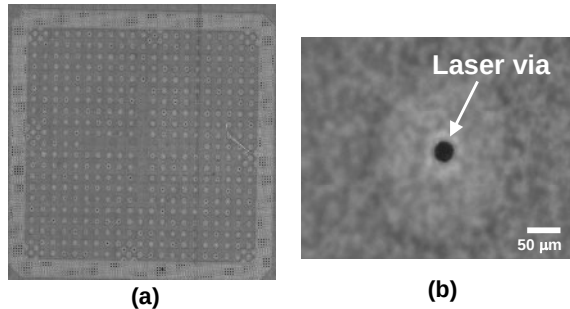


Fig. 12 (a) Laser vias for a whole chip (8 mm sq.) and (b) a single via by vision measuring machine

Thanks to the automatic measurement, the ~200,000 laser vias on the Cu base plate are measured in about two and half hours. The recognition ratio is 99.8%, so almost all the via positions on the Cu base plates can be measured with the vision measuring machine.

Figure 13 shows the displacement distribution of the laser vias. For one chip, the distribution is almost Gaussian (a). However, the distribution for all vias for several packages on the Cu base plate is not Gaussian (b). The reason for this difference becomes clear when their displacements are distinguished by chip (c). As shown in Fig. 13(c), the displacement distribution for all laser vias is the aggregated distributions for all chips.

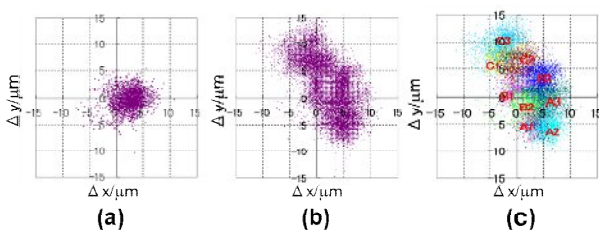


Fig. 13 Laser via displacement distribution for (a) one chip, (b) all chips on Cu base plate, (c) all chips (chips distinguished by color)

We also estimate the UV-YAG laser irradiation influence on 90-nm CMOS transistors. The drain current - gate voltage curves of the transistors are unchanged by the laser irradiation, whether or not the pads are covered with Cu of 5 to

30 μm in thickness. Therefore, the laser via process does not damage the embedded LSI.

3.5 Divided fabrication method and lump fabrication method

We compare the measured displacement data with the accuracy needed for 80- μm -pad-pitch interconnects. The representative LSI pad diameter, laser via diameter, and wiring land diameter are 60, 30/20 as top/bottom, and 40 μm , respectively. As shown in Fig. 14, 20- μm displacement for the laser vias and 10- μm displacement for the upper layer wiring are critical for achieving reliable interconnects.

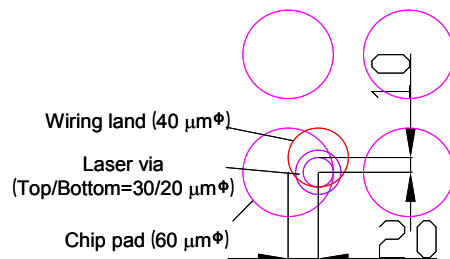


Fig. 14 Relationships between LSI pad, laser via, and wiring land diameters for 80- μm -pad-pitch interconnects

Representative displacements of the chip mounting, laser via, and wiring land are 8, 18, and 5 μm , respectively. These displacements are smaller than the critical values shown in Fig.14.

Displacement of the laser via from the chip pad depends not only on the nominal laser via displacement but also on the chip mounting displacement. Therefore, two types of fabrication methods are compared. One is a divided method, which uses the individual alignment marker of each chip. The other is a lump method, which uses the Cu plate alignment marker for every chip. The lump method is more cost effective, because the fabrication process is simpler.

The displacement of a laser via is larger than that of chip mounting and the wiring formation. Therefore, if we can reduce the laser-via displacement, we can fabricate SIRRIUS packages using the lump method. We thus try to improve the accuracy of the laser via positioning. As shown in Fig. 15, we successfully reduce the displacement to the value smaller than 10 μm . Use of the lump fabrication method is thus feasible.

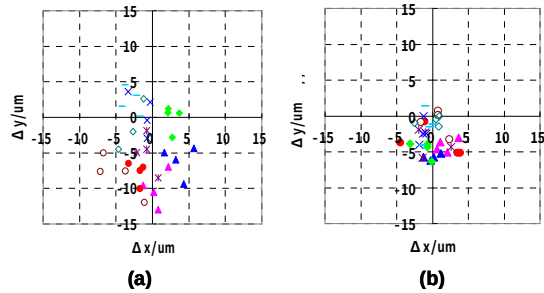


Fig. 15 Laser via displacement (a) before and (b) after improvement in laser via positioning

4. Prototype SIRRIUS package and reliability

4.1 Fabrication

Using the technology processes described above, we fabricated a prototype SIRRIUS package.

Figures 16 and 17 show package photographs after the first wiring layer fabrication and second wiring layer fabrication, respectively. As shown in Fig. 16, 80- μm -pitch, four-row pad connections are clearly observed. In the second wiring layer, the pad pitch is widened to 100 μm , and fine 100- μm -pitch connections are fabricated.

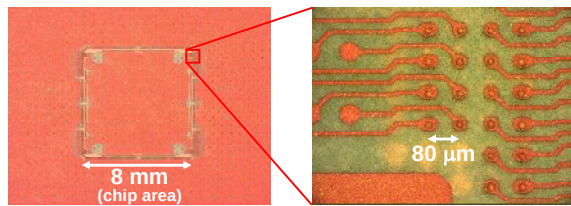


Fig. 16 Prototype SIRRIUS package after the first wiring layer fabricated

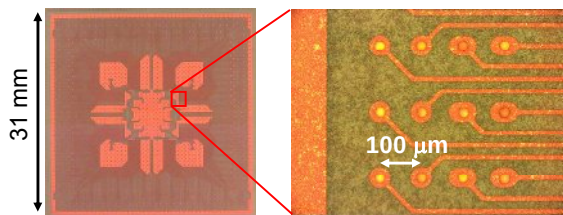


Fig. 17 Prototype SIRRIUS package after the second wiring layer fabricated

Photographs of the fabricated prototype SIRRIUS package are shown in Fig. 18. Its specifications are listed in Table 1.

The top-side view shows only the 0.5-mm-thick Cu plate, which acts as a heat spreader [6]. The BGA-side view shows the 900 BGA balls. Since Pb-free BGA balls are used, the package is

completely lead free.

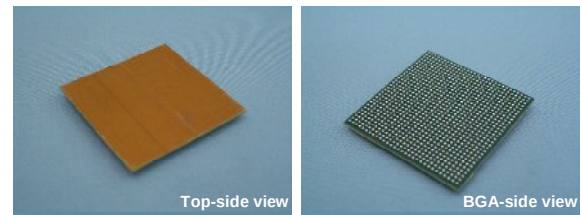


Fig. 18 Top-side and BGA-side views of fabricated prototype SIRRIUS package

Table 1 Specifications of fabricated prototype SIRRIUS package

Chip	Size (mm)	8 x 8
	Thickness (μm)	50
	Pad count	1200
	Pad arrangement (signal)	80 μm , 4 row
Package	Size (mm)	31 x 31
	Thickness (mm)	0.71
	BGA pad count	900
	BGA pad pitch (mm)	1.0 (area array)

Cross-sectional views of the SIRRIUS package are shown in Fig. 19. A 50- μm -thick LSI chip is embedded in the first built-up resin layer and connected to the first metallization layer by direct Cu plating. Despite the use of a 0.5-mm-thick Cu plate, the total package thickness is only 0.69 mm, including three metallization layers and solder resist.

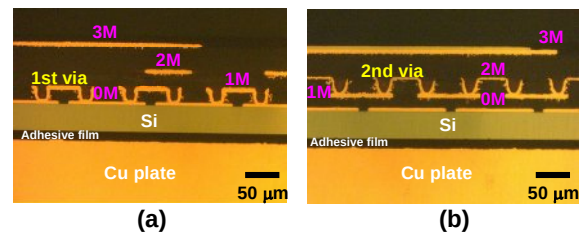


Fig. 19 Cross-sectional views of fabricated prototype SIRRIUS package: (a) cross-section showing the first via, (b) cross-section showing the second via

4.2 Reliability

The reliability of the prototype SIRRIUS package was evaluated at the package level using thermal cycle testing. The test conditions and results are summarized in Table 2. The package samples were subjected to a pre-treatment process with

conditions corresponding to JEDEC (Joint Electron Device Engineering Council) level 3. The samples showed no electrical failures or resin cracks after 600 cycles.

Table 2 Package-level thermal cycle test conditions and the result.

Pre-treatment
1. Pre-bake: 125°C for 10 hours
2. Moisture absorption: 30°C, 70% RH for 7 days
3. Reflow: max. 260°C, 3 times
Test conditions
-55°C, 10 min; 125°C, 10 min 600 cycles
Result
No electrical failures or resin cracks

We also evaluated the reliability at the board level. The test conditions and results are summarized in Table 3. The samples showed no electrical failures or cracks after 1000 cycles.

Figure 20 shows a cross-section of the SIRRIUS package sample after 1000 cycles. No cracks inside the package or BGA balls are observed. The heights of BGA balls in the center and the edges of the package are almost the same. These results of the reliability tests indicate that the SIRRIUS package has good long-term reliability.

Table 3 Board-level thermal cycle test conditions and results

Test conditions
-40°C, 10 min and 125°C, 10 min 1000 cycles
Result
No electrical failures or BGA ball cracks

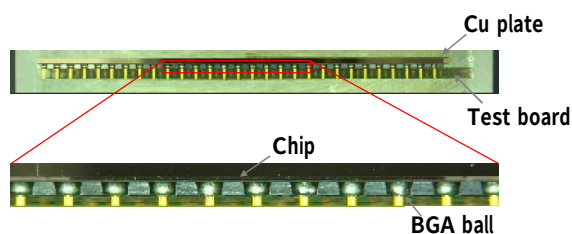


Fig. 20 Cross-section of the board after 1000 cycles of thermal treatment

Conclusion

We have successfully developed a direct fanning-out packaging technology, named as “SIRRIUS”, for embedding fine-pad-pitch LSI chips. The SIRRIUS package consists of a Cu base plate, an embedded LSI chip, built-up resin layers, and multi-layer fanning-out wiring with laser-vias.

For embedding the chip with 80- μm -pitch and four-row pad layout, using a low-viscosity resin and optimizing its thickness are important. By estimating the displacement properties of the mounted chips and laser vias and improving their position accuracy, we demonstrated that the lump method can be used to fabricate the SIRRIUS package. A 31-mm-square, 900-pin-count SIRRIUS package with three-layer wiring, 15 μm wide, was fabricated. Its total thickness is only 0.69 mm including the Cu plate. Evaluation of package-level and board-level reliability showed no electrical failures or cracks after 600 and 1000 cycles, respectively. The SIRRIUS package is thus an attractive approach to fabricating thin and highly reliable fine-pad-pitch system LSI packages for replacing FCBGA packages.

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