

Active Demonstration of a Passively Self-Aligned, Multi-Chip Package using Proximity Communication in a Switching Fabric

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Abstract

Recently, we introduced a novel chip packaging platform based on the passive self- alignment of chips into 2D arrays, which extends the physical area of fully integrated CMOS VLSI silicon chip beyond the area of the single chip reticle [1]. We report the first active demonstration of this packaging concept, in which functional chips are configured in a face-to-face geometry with sufficient alignment accuracy to enable Proximity Communication (PxC): chip-to-chip capacitively coupled communication between overlapping metal pads [2]. The key advance reported here is a low-cost packaging application of self-aligning precision microballs and etched pits in CMOS for successful high fidelity PxC signaling. Creating these pyramidal wafer pits required co-integrating silicon micromachining into a 180 nm CMOS technology. Our demonstration vehicle is an active switching fabric composing a four chip linear vector array [3]. Atop these four face-up "island" chips sit face-down "bridge" chips, such that data can be coupled between four islands via overlapping bridges. Inverse pyramidal pits on both bridge and island chips are photolithographically defined relative to the capacitive micropads. In our demonstration 300 micron diameter microballs precisely lock the chips in global alignment to within a micron and PxC signaling is achieved across array without error. This assembly has relaxed manufacturing tolerances: up to half the microball diameter in placement inaccuracy still leads to precise self-alignment to within a couple of microns.

Key words: proximity communication, wafer scale packaging, 0.18 μm CMOS, silicon micromachining.

1. Introduction and motivation.

Computer system performance has steadily benefited from Moore's scaling law. Over the past years the CMOS VLSI circuitry has seen its dimensions shrinking well into the nanometer scale. The mounting technological barriers are proving it ever more challenging to continue this trend. The overall system can still benefit from further performance improvement with innovative integration and signaling techniques to overcome scaling limitations and off-chip bandwidth bottlenecks. Novel interconnect technology, Proximity Communication (PxC), has been reported [1] and has been shown to enhance the system functionality in a multi-chip configuration. PxC is based on a capacitive coupling in order to directly transmit data from one chip to another. An array of metal pads, of both receiver and

transmitter type, are fabricated in the top metal layers of the semiconductor chips and as these chips are placed in the direct proximity of one another the inter-chip communication is established. PxC sets new standards in the chip interconnect technology. For example, the chip I/O bandwidth density is improved by two orders of magnitude in comparison with conventional chip packaging technologies such as ball grid arrays. In absolute numbers, PxC offers a dramatic increase in chip I/O bandwidth per each square millimeter of the chip overlap, up to 10 Tbit/s. Additionally, PxC concept can also facilitate the replacement of the failed chips in the package given that the capacitive nature of the contacts does not require permanent connections. This feature could improve the package assembly yields for multi-chip modules

where the ability to separate nonfunctional and functional (good) die (KGD) is a key. PxC relies on the capacitive coupling between the metal pads in the top CMOS stack up layering of the overlapping “communicating” chips. The their linear size to 20-30 μm (400-900 μm^2 area of each pad) while maintaining high channel density and ensuring the I/O bandwidth. The microscopic pad size puts stringent alignment constraints on alignment which has to be sufficient to fully eliminate the pad to pad or channel to channel cross-talk and establish an error free PxC connection. The package assembly has to be accurate within microns in terms of chip to chip relative positioning with minimized or virtually non existing vertical separation. Also rotational degrees of freedom

The outlined PxC packaging requirements would currently present a practical challenge for a conventional chip and package assembly tooling. The high volume manufacturing assembly line is equipped with pick and place machines capable of aligning chips within $\pm 12.5 \mu\text{m}$ tolerance. Undoubtedly there are flip chip tool solutions specified to align and place chips to fraction of a micron but those are utilized in the prototype rather than manufacturing environment. Clearly in order to assemble PxC chips into a MCM package within the described tight alignment tolerances a breakthrough technology is required.

This paper describes a PxC package consisting of four active chips arranged in the linear vector array. The alignment accuracy is guaranteed by a novel packaging approach based on the silicon micromachined features integrated with CMOS electronics. These features are anisotropically etched pits and house high precision micro-balls to allow simultaneous locking in x-, y-, z- chip to chip mutual positioning as well as their rotational orientation. The wafer level fabrication process is discussed and its integration is demonstrated in the standard 0.18 μm CMOS technology. This enabled chip assembly is based on a low cost, injection molded plastic tray with an integrated heat sink, and wire bonded to a circuit board compatible with an advanced telecom computing architecture (ATCA) chassis. The wire bonds carry power, ground, and switch I/O to the four face-up island chips that are evenly spaced in the plastic tray. We report on our multichip package, the fabrication of the alignment mechanism, our global positioning metrology measurements, and the first validation of PxC signaling in a package

capacitive pads need to be sufficiently small in order to effectively maximize the use of this overlap. Conceivably the pads could be scaled down to micrometers although for practical reasons it would prove sufficient to set and their corresponding positional errors must be especially accounted for when several PxC chip interfaces are created. For example, if PxC designs are based on the 24x24 μm^2 square capacitive pads it would allow for 1/3 pad size or 8 μm of lateral misalignment as well as vertical chip separation. Any further refinement in x-, y- and z- positioning would further lower the power consumption and improve the communication performance.

2. Chip to chip alignment enabled by pit and micro-ball.

The alignment mechanism reported in this paper is based on the etch pit and micro-ball implementation. In its root is a square top pyramidal etch pit micromachined in silicon. It is well understood that the square or circular opening in mask layer on top of (100) silicon will evolve into an inverse pyramid shaped pit when exposed to hydroxide etching chemistry. The pit is sidewalled with (111) silicon planes and its edge openings are parallel to $\langle 110 \rangle$ direction. The (111) sidewalls form 54.7 degree angle with the top (100) surface (Fig. 1a).

The etch pit owes its shape to a distinct disparity in etch rates between different silicon planes, particularly low etch rate of (111) plane relative to high etch rate of (100) plane as well as other higher order silicon planes. The r_{111}/r_{100} etch rate ratio mostly depends on the choice of wet etchant, its temperature and concentration and silicon doping. The ratio could vary from 1:20 to 1:400 but a particular process and choice of materials it is a well calibrated repeatable parameter which allows to accurately program the micromachined silicon pit opening with wide process window. The photolithography defines the etch pit positions as well its dimensions. Due to the high anisotropy the etch stop or exact timing are not necessary which makes the process very robust.

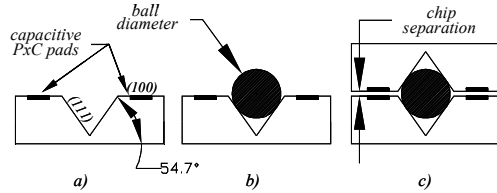


Figure 1. A schematic cross-section of the etch pit and ball configuration for chip to chip alignment.

If two silicon chips need to be brought into alignment a pair of etch pits of identical size and separation would be micromachined in each in their designated overlapping areas. The first chip pits are then populated with micro-balls of appropriate size (Fig. 1b) and the second chip pits are then “dropped” on top of them. The second chip would need to be initially aligned to only about half the diameter before being “dropped” as the micro-balls then would engage into its pits and autosteer the chip into the designed location providing the capacitive pad overlap and the calculated chip separation (Fig. 1c). The aforementioned high volume pick and place equipment can well accommodate the task. For example, in case of a 300 μm diameter ball each pit need to be initially aligned within approximately 150 μm in x- and y- letting the micromachined pits position the chips down well into micrometers. This passive alignment technology could be scaled up to several chips, arranged in linear or areal fashion resulting in operational PxC MCM. As noted, since there no permanent PxC connections the PxC MCM may have true reworkable or even reconfigurable capability.

The ball and pit alignment technology was recently demonstrated with optical proximity and was integrated with compliant interconnects. The details and principle of these applications could be found [2] and [3]. To date capacitive PxC has only been demonstrated on an optical bench using mechanical nano-precision stages along with on-chip electronic feedback, to mitigate all six potential degrees of chip misalignment and to position chips precisely for high fidelity PxC signaling. It was shown in the capacitive 1.8 Gbps PxC signaling between two chips the I/O signal density

improved by 25x and energies per bit lowered by 10x over conventional serialized links [4].

3. Back-end of the line etch pit processing.

Integration of alignment pits into silicon that contains CMOS circuits presents challenges that relate to both the active CMOS circuitry and to the Si-micromachining process steps. Importantly, the pit integration must not cause circuit failure and secondly the dielectric stack up must not interfere with accurate pitting to facilitate the alignment tolerance needed for PxC packaging. The on-chip integration of CMOS electronics and silicon micro-machined structures is an exploding field with many examples demonstrated by both the commercial foundries and academic institutions. The applications have been targeted in the ambient sensing, temperature and pressure monitoring, accelerometry and wafer scale packaging to name a few. The designer of these micromachined structures have to ensure the post-CMOS fabrication is fully compatible with CMOS circuitry keeping the process within the allowed thermal budget and utilizing appropriate chemicals and tooling. It also has to be well understood whether and how the original CMOS design rules are not violated.

Our demonstrated PxC self-aligned prototype is a multi-chip package consisting of four logic chips (the island chips) that are tied together through PxC links provided with two bridge chips. Altogether, these four island chips form a buffered crossbar switch. The chips are fabricated in the standard 0.18 μm 6 metal logic process, both bridge and island situated on the same reticle. Each chip contains four designated etch pit sites such that there to be two alignment etch pits per each chip edge designed for the overlap with its mating chip.

Chip dimensions are shown at scale in Fig. 2, the etch pits are designed to be 1 mm away from the bridge chip corners. The designated etch pit area on the bridge and island chips is 700x700 μm^2 . This area contains no active circuitry but is still compliant with the CMOS design rules particularly metal density rules corresponding to each stack up layer. The metal fill is a rectangular array of squares stacked exactly on top of each other from the metal 1 up to metal 6. When completed the etch pit opening will be over 170 μm away from the active circuitry in any direction which, in our

experience, is a sufficient keep-out distance to maintain the CMOS integrity and yield.

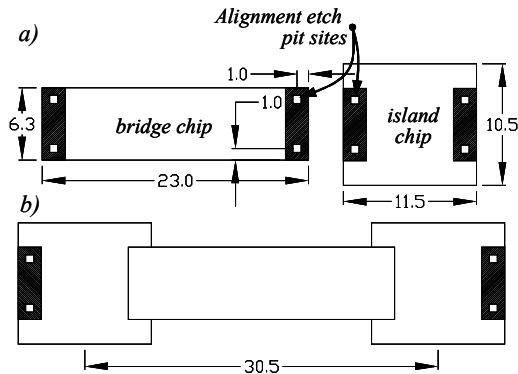


Figure 2. Island and bridge PxC chips with their respective dimensions in mm and etch pit locations (a); (b) demonstrates their bridge/island layout with aligned etch pits and overlapped PxC blocks.

The alignment etch pit fabrication is a two stage fabrication process. First stage aims for selective CMOS stack up removal in the pit dedicated area. A result is a complete removal of interlayer dielectrics, metal fill and polysilicon down to a silicon substrate. In the second stage the exposed silicon substrate is shaped into the etch pit with anisotropic wet etch.

The key requirement for a precisely defined etch pit is a pristine flat silicon surface. We addressed this key issue in the first fabrication stage and optimized the process for it. The CMOS wafer is first patterned with 8 μm thick SPR-220 photoresist with a $500 \times 500 \mu\text{m}^2$ opening that is intended for the CMOS deprocessing (Fig. 3a). The stack up is removed in a sequential manner removing one CMOS layer at a time. Each CMOS layer is attacked with dry etch process first for corresponding ILD removal (Fig. 3b) which is then followed by a wet etch of aluminum (Fig. 3c). The metal layers are designed to be isolated from each other without the tungsten interconnects in between. Each layer is mostly composed of oxide like dielectrics and is specified to have a known thickness. The implemented etch conditions are as indicated in the Table 1.

Each layer removal is appropriately timed corresponding to its thickness and composition. The dry etch rate averages about 70 nm/min.

Table 1. CMOS dry etch deprocessing conditions.

Flow CF ₄ , sccm	20
Flow O ₂ , sccm	1
Pressure, mT	50
Power, W	200
Bias, V	500
Temperature, °C	20

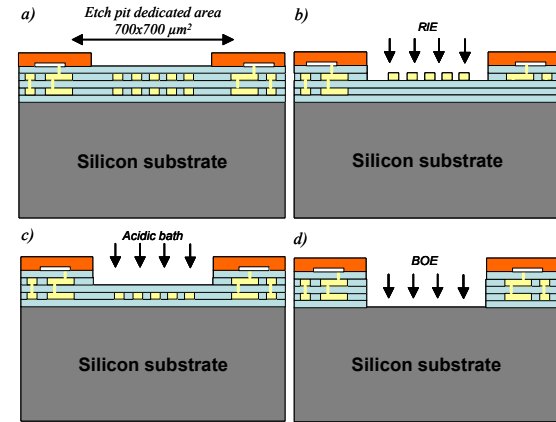


Figure 3. Schematic process flow (shows two metal layers only, the real stack up consists of six metal layers) for the selective area CMOS deprocessing.

Aluminum metal fill tiling is removed with its wet etchant (phosphoric, nitric and acetic acids based E-6 mixture from Fujifilm Electronic Materials). The masking photoresist is stripped off, reapplied and repatterned with proximity aligner three times during these cycles due its erosion and loss of thickness.

After removing all of the six metal layers with its ILDs the wafer is briefly exposed to buffered oxide etch (BOE). BOE removes the remaining dielectrics (IMD and field oxide) layer adjacent to the silicon substrate. Due process variability from wafer to wafer and also non-uniformity of the dry etch rates across the wafer the resulting dielectrics layer under Metal 1 prior to BOE exposure carries certain roughness up to several hundred nanometers. BOE removes this roughened layer and exposes the silicon substrate surface (Fig. 4). The BOE step is as well critical to ensure the alignment etch pits' designated shape, their dimensional accuracy and uniformity across the wafer. Without it the residual roughness in the dielectrics would be imposed onto the silicon interface. This would compromise the integrity of the coated masking silicon nitride layer which is used in order to

define the etch pit opening. The etch pit quality and yield will not allow for the accurate PxC chip to chip alignment if this layer is poorly adhered to silicon or carries voids.

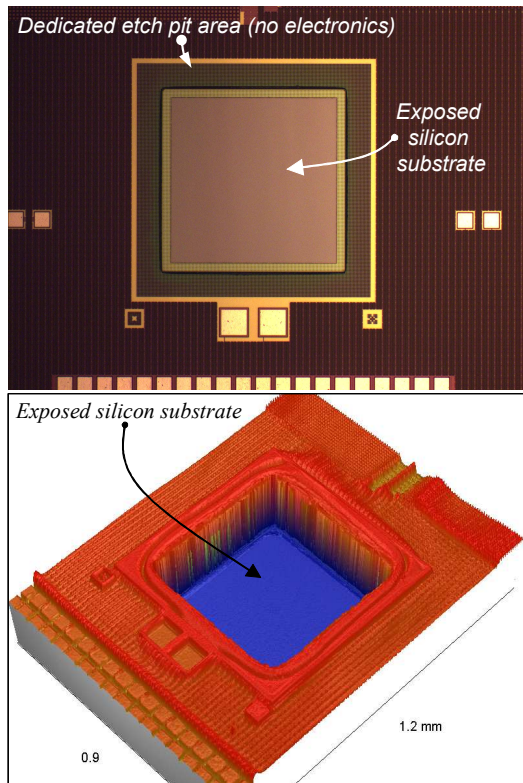


Figure 4. Top image is a top view of the dedicated etch pit area with entirely removed CMOS stack up. Shown is the exposed pristine silicon substrate surface ready for silicon nitride coating and pattern. Bottom image is obtained with an interferometric microscope and is 3D illustrating the same etch pit area. Shown in false color are height variations from the original CMOS stack-up down to the exposed silicon substrate. Silicon is 10.5 μm below top CMOS surface.

A second stage in the alignment pit fabrication is its anisotropic wet etch formation. Post processing of CMOS wafers, in particular anisotropic etching of silicon has been a challenge for a long time. The difficulties stems from mainly incompatibility of anisotropic etchants and mask materials. The hydroxide etchants of choice are potassium hydroxide (KOH) and tetramethyl ammonium hydroxide (TMAH). Both are inexpensive chemicals and provide high etch rates. For a given temperature KOH etches silicon faster and has higher anisotropy ratio, r_{111}/r_{100} . For example, 35%

KOH solution at 75°C etches (100) silicon at 1.1 $\mu\text{m}/\text{min}$. For 170 μm of etched depth it undercuts the mask by 5 μm in horizontal direction. The corresponding anisotropy ratio is 1:40. In comparison 5% TMAH solution at 75°C will etch at 0.7 $\mu\text{m}/\text{min}$ undercutting 10 μm . Without the etch stop the pit formation need to be timed to reach an anticipated depth. As was pictured in Fig. 1 our alignment mechanism is based on the micro-ball residing on the etch pit's (111) sidewalls. The etch rate and the extent of the undercut are repeatable parameters such that with temperature stabilized both the etched features or pits are obtained with high accuracy dimensionally. We have demonstrated reproducible calibrated wafer scale pitting process with both KOH and TMAH etchants. As opposed to KOH the TMAH contains no metal ions and is already widely used in the CMOS foundries in the form of the photoresist developers so its CMOS compatibility is readily established.

Silicon nitride is a widely used candidate for a hard mask material in silicon bulk anisotropic micromachining. It is well suitable for both KOH and TMAH provided it is of high quality with low pinhole density and well adhered to silicon. High quality silicon nitride is deposited with low pressure CVD. This process takes place at temperatures exceeding 700°C which is outside of the thermal budget acceptable for any type of post processing of completed CMOS circuitry. Plasma enhanced CVD of silicon nitride can be carried out at or below 350°C which is CMOS compatible for practical deposition durations. Unfortunately the PECVD silicon nitride is of lower quality relative to LPCVD. Our CMOS chips, both bridge and island, are already foundry passivated with silicon nitride. There are arrays of open aluminum micropads on the chips' surface that need to be adequately masked against the hydroxide chemistry. Their fill factor is very high so the PECVD silicon nitride cannot provide sufficient pinhole free coverage and effective masking against KOH or TMAH. We have also experimented with alternative protective coatings, such as silicon carbide and amorphous carbon. The applicability of these materials in hydroxide chemistry was not found satisfactory due to inadequate adhesion to aluminum pads. There are newly developed organic polymer etch protective coatings. We have evaluated photopatternable ProTEK[®] PSB resist from Brewer Science, Inc [5]. It is a spinnable negative acting resist that forms 5 μm

thick film. The resist provides a conformal surface coverage, shows no pinholes or cracks and protects the ICs for the duration required to form the etch pit (2.5hrs in 30% KOH or 4hrs in 5% TMAH). While adequately protecting the CMOS top surface and aluminum micropads the ProTEK[®] resist is not suitable for defining the alignment etch pits due to large mask undercuts. It was observed that its undercut is not a reproducible parameter which varies from etch pit to etch pit or across the wafer, approximately from 20 to 40 μm for a mentioned duration of the etch pit process.

The PxC alignment pits need to be defined with a micron accuracy so we developed a two layer mask composed of silicon nitride and ProTEK[®] resist. A conformal 0.5 μm SiN_x hard mask is PECVD deposited at 350°C across the 200mm wafer and patterned with resist for dry etching in a selectively opened window in CMOS. The resist is patterned with 0.25 μm lithography to define square 328x328 μm^2 outlines for the anisotropic etch of the pits and also open windows in all of the aluminum micropads. The nitride is dry etched down to silicon substrate in the pit area and down to aluminum on the pads. ProTEK[®] resist is then spin coated and patterned. ProTEK[®] pattern is an array of a larger 338x338 μm^2 square windows centered on top of the nitride openings. The sufficient lithographic accuracy in both the dimensional resolution as well as the registration for the ProTEK[®] pattern can be relaxed to a ± 2 μm such that the proximity aligner can be utilized. The dual mask is complete and ready for the anisotropic etching. The PECVD silicon nitride defines the etch pit with submicron accuracy while the ProTEK[®] resist masks the wafer against KOH everywhere outside of the pit locations. The backside of the wafer is a polished surface coated with PECVD silicon nitride.

The pit anisotropic wet etch is a wafer scale batch process carried out in a bath with either KOH (35%, 75°C) or TMAH (5%, 75°C) for a duration required to etch the pits down to 170 μm (or depth larger by 10% than the radius of the intended micro-ball). The ProTEK[®] resist is then ashed in oxygen plasma completing the alignment pit fabrication process (Fig. 5).

The pits' depths do not need to reach their inverse pyramid apex to properly work. Since the microball is going to be residing on the

pit's sidewalls the pit has to be deep enough and the resulting pit opening, initial mask size plus the undercut, will set the microballs position in z- and, eventually the chip to chip separation. The process window in wet etching is therefore quite wide. For example, a ± 10 minute timing error during the 150 minute wet etch in KOH would result in ± 11 μm pit depth variation while only effecting the pit opening by ± 0.3 μm resulting in highly accurate pit formation despite having no etch stop. Of course, the undercut still contributes to the pit opening and hence must be accounted for in sizing the microball and determining the chip gap in the packages.

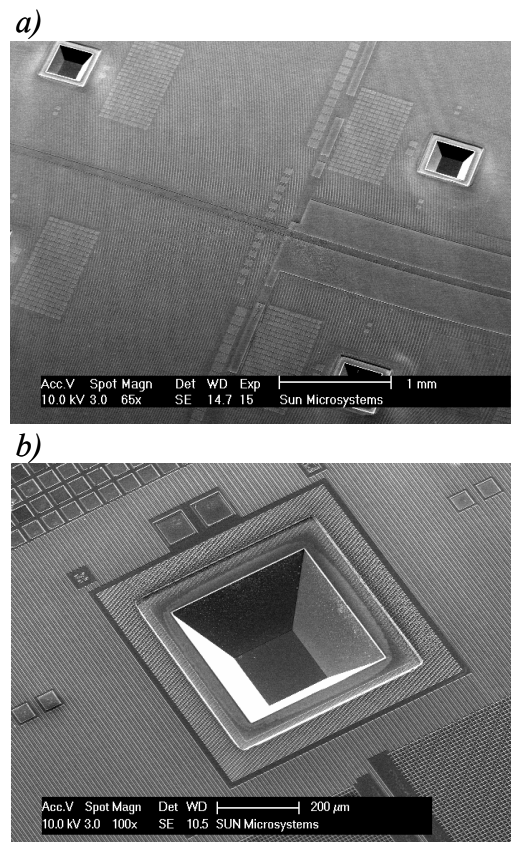


Figure 5. SEM micrographs of the wafer fragment (a) showing several fabricated etch pits in 0.18 μm CMOS and the individual pit (b).

The SEM in Fig. 5b shows the CMOS window extends down to base silicon. The neighboring circuitry remains pristine and the pyramidal faces exhibit (111) facets with rms roughness of several nm. The ultimate facet smoothness is primarily dictated by the chemistry of the anisotropic etch provided that

both the native oxide and process contamination have been exoriated prior to etching. The alignment of the pyramidal pits relative to the PxC capacitive pads is entirely determined by the resolution and accuracy of the photolithographic tooling. The resulting pit size uniformity across a 200mm wafer is within 1 μm of standard deviation. We have not observed any IC deterioration caused by the described CMOS post-processing.

4. Package assembly.

Each demonstrated PxC package contains four island chips and two bridge chips. The bridge chips in the package were microsoldered to the island chips and overhang as face down chips to the neighboring island chips. The two bridge chips in Fig. 6 derived their power and ground from their respective island chips via microbump attachment to form a hybrid chip. Micro-bump is a low ohmic contact dense interconnect arranged on the fine pitch of 54 μm . The detailed description of this interconnect could be found in [5]. The low cost sapphire microballs are assembled in the etch pits of the first chip, creating a relative reference system controlling location, rotation, and height of the mating chip. The size of these microballs is appropriately chosen to minimize the chip separation. Their ball diameter is in the range of 290-300 μm and depends on the choice of the anisotropic wet etchant and its corresponding undercut. The diameter and eccentricity of these microballs is tightly controlled down to a fraction of a micron.

When the mating chip is brought into approximate half the ball diameter alignment during mating into locating sites in the housing, the ball located in the etch pit of the first chip will locate itself in the etch pit of the mating chip. This provides the primary position reference. A second establishes rotational reference – with some allowance for true position of the ball. The remaining two balls on the mating chip can then find etch pits in a third chip (and so on), and provide the final spacing reference between the three (or more) chips. A true position analysis based on the capabilities of the accuracy of the silicon etch process and the planarity of the silicon wafers and the underlying substrate can be done to determine the optimal size and location of the etch pits.

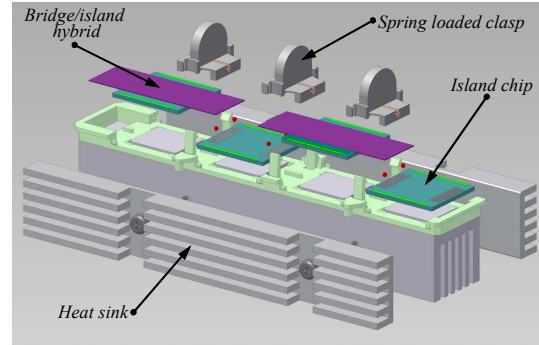


Figure 6. Exploded view of the PxC package with four island and two bridge chips. The chips are passively aligned with ball and pit mechanism and locked with spring loaded clasps on the heat sink.

Note that the precise alignment between chips is performed entirely as a passive alignment step. The multi-chip assembly may then be wire-bonded to a printed circuit board or second level package, after the chips have been precisely aligned. A heat sink, attached from below can provide a path for heat removal and also mechanical reinforcement to the package. The picture of the assembly wire bonded to the board is shown in Fig. 7.

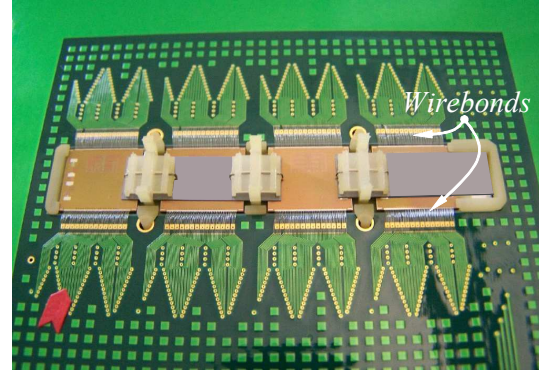


Figure 7. Completed PxC package mounted into the PCB board. Wirebonds to all four islands supply power and I/O connections.

We have introduced a new alignment mechanism that precisely positions chips by a self organizing process that further passively assembles to tolerance. This alignment mechanism allows one to take advantage of the relatively coarse chip placement accuracies of the packaging industry. This example was the first package that implemented the new ball and pit alignment mechanism in active chips and was accomplished with wire bonding to the island chips.

5. Package metrology and test.

The assembled packages were verified on the accuracy of lateral alignment with high precision microscope system. The system is equipped with linear stages capable of resolving $0.1\text{ }\mu\text{m}$ over the package footprint. Corresponding four corner points on each island chip have been mapped out and their coordinates have been compared against the GDS original data as we assembled and reassembled several packages to also demonstrate the mechanism's ability to be reworked. Resulting chip to chip displacement error is $2.2\text{ }\mu\text{m} \pm 0.5\text{ }\mu\text{m}$. Some of the major key factors contributing to the error are photolithographic tolerances, ball diameter deviations and the flip chip bonding misalignments with the latter influencing the overall chip displacement the most.

At the core of this prototype is a multi-chip package consisting of four logic chips (the island chips) that are tied together through Proximity Communication links. Together, the four island chips form a buffered crossbar switch. Each Proximity Communication link consist of 72 transmit and 72 receive channels each capable of running at 1 Gbit/s.

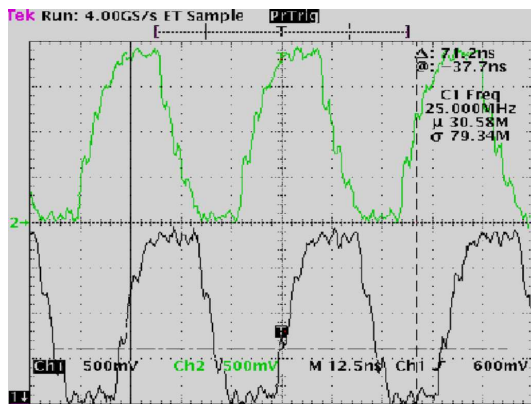


Figure 8. Demonstrated data stream through one of the PxC hops of the four chip linear package.

All 72 PxC channels of the switch run at 1 Gb/s but are exclusively dedicated to the internal operation of the fabric and were not available for signal quality analysis. To evaluate signal integrity we deployed a few service channels that run at lower data rates below 100 MHz rate. We measured data strings across the PxC pads between a bridge/island interface and showed the PxC received data streams in Fig.8. Actually we show two different service channels

operation at the same interface. The Fig. 8 data confirms that PxC is working across multiple channels at one of the PxC interfaces.

6. Summary.

We have demonstrated for the first time the multi chip package with established PxC between the chips. The necessary micron scale chip to chip positioning as well chip separation was ensured by etch pit and ball self alignment. The CMOS compatible robust wafer scale fabrication is described leading to highly accurate pitting process in the $0.18\text{ }\mu\text{m}$ node

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