

Thermal Characteristics for LSI Embedding Build-up PWBs

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Abstract

Electronics manufactures work over with developing the performance, multiplying the function and downsizing of electronics modules with the high-density jisso technology. The authors carry out developing LSI embedding build-up PWBs with simultaneous laminate process as a forced solution. On the other hand, the high-density jisso technology brings heat issues. This paper reports the thermal characteristic for LSI embedding build-up PWBs on thermal simulation; 1) estimating thermal property of current LSI embedding build-up PWBs, 2) study of thermal conductivity on material on improving the thermal performance, 3) heat spreading along metal layers in build-up PWBs, 4) effect of embedded heat spreader. The authors succeed to improve thermal performance by 28% in comparison to conventional PWB structure.

Key words: LSI embedding, thermal characteristic, thermal conductivity, heat spreading, simulation

I. Introduction

It is commonplace for daily essentials to be installed electronic modules in these days. Major demands for the electronic modules are developing the performances, multiplying the functions and saving the weight. Therefore, many electronic companies work on developing highly integration of Si chip with high performance and/or multifunction. On the other hand, semiconductor makers provide small packaging technologies for LSI, such as CSP (Chip Scale Package or Chip Size Package), FC (Flip Chip) and WLP (Wafer Level Package). Additionally, it is also the solution for the

market demand to assemble LSIs and passive components in one package with high density, such as MCP (Multi-Chip Package), SiP (System in Package), POP (Package on Package), 3-D stacking and so on.

The other solution for market request is high density mounting on PWB (Printed Wiring Board) with 3-D jisso technologies and the device embedding technologies. The feature of these technologies is materializing highly dense jisso with commonly used, i.e. easily procurable and quality assured, components.

The passive parts embedding technologies for PWB is already introduced to sub-module of camera

module for cellular phones especially to improve technical function with maintaining a specified form factors as the B²it™ (Buried Bump Interconnection Technology) PWB^[1]. Moreover, the embedding technologies expands with embedding active device so-called e-B²it (Embedded-Buried Bump Interconnection Technology) PWB, such as small pin count bare Si chip and assembled in WLP, and then put in commercial production.

The authors study active device embedding technologies to enhance the scale of embedding LSI in these days^[2]. The investigation for high ratio signal transmission is also worked over^{[3], [4]}.

Besides, it brings serious heat issue for the dense jisso or mounting technologies to concentrate heat sources, such as LSIs, in narrow area or small volume. Additionally, the heat sources are covered up with heat resistive material for e-B²it PWBs technology, so that it brings the severe heating to rise temperature more than operative temperature of LSIs. Consequently, it is necessary to improve heat spreading to manage the working temperature of embedded LSI.

In this paper, the authors estimate the working temperature of embedded LSI, and the temperature distribution and the heat flow in a given e-B²it PWB on CFD (Computed Fluid Dynamics) analysis. Then, the capability of power consumption, which the authors define as the power consumption to rise the temperature of LSI by 40K, is derived. Furthermore, the improving on coolability of the embedded LSI and the e-B²it PWB is reported with following issues,

- A) thermal conductivity of the material,
- B) enhancing of heat spreading with metal layers,
- C) embedding not particular kind of heat spreader in e-B²it PWB

II. Basics of Analysis Model

The thermal characteristic is simulated on CFD Analysis with ANSYS ICEPAK 12.0 under the still air condition. Figure 1 shows schematic view of fundamental analysis model.

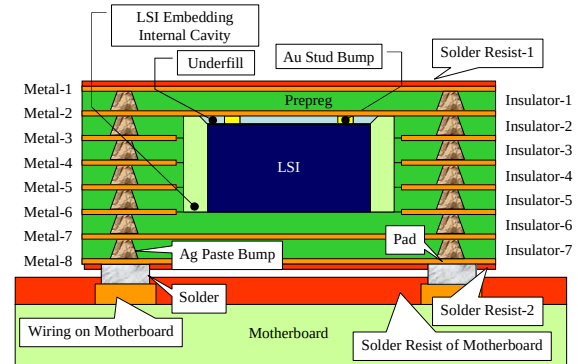


Figure 1

Schematic view of simulation model

T_j	Junction Temperature of Embedded LSI
T_t	Temperature at Top of e-B ² it PWB
T_b	Temperature at Top of Motherboard
T_a	Ambient Temperature
ΔT_j	Difference between T_j and T_a
ΔT_t	Difference between T_t and T_a
ΔT_b	Difference between T_b and T_a
R_{ja}	Thermal Resistance between Junction and Ambient
R_{jt}	Thermal Resistance between Junction and Top of e-B ² it PWB
R_{ta}	Thermal Resistance between Top of e-B ² it PWB and Ambient
R_{jb}	Thermal Resistance between Junction and Motherboard

Table 1

Definition of thermal junction

The thermal evaluation TEG, JTEG Phase 5 of Hitachi High-Technologies, is embedded in the e-B²it PWB. The e-B²it PWB consists of 8 metal layers and 7 insulation layers. The metal layers are formed out of Cu foil and the insulation layers are built up with the composite of thermo-setting epoxy resin and glass fiber, so called epoxy prepreg. The metal layers are connected electrically and/or thermally with Ag paste bumps.

The thermal conductivity of Cu is 401W/mK. Prepreg is adopted the thermal conductivity supplied by prepreg manufacturers. The thermal conductivity of Ag paste bump is given about

10W/mK^[5]. In authors' current study, the thermal conductivity of Ag paste bump is applicable for current design rules.

The routing design of e-B²it PWB is imported in ANSYS ICEPAK model through Gerber format data. The dominant wiring layers of the simulation model are metal-2, 7 and 8. The TEG is mounted on metal-2 with Au stud bumps on silicon chip and underfill between silicon chip and metal-2. The connection pads for motherboard are assigned in metal-8. Details of the e-B²it PWB and TEG are shown in figure 2 and table 2.

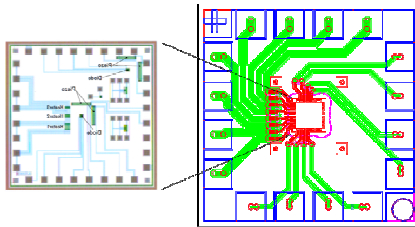


Figure 2

Top view of TEG and e-B²it PWB

e-B ² it PWB	Dimension	20mm x 20mm x 0.7mm	
	Number of Layers	Metal	8
		Insulator	7
	Number of Pads	16	
TEG	Dimension	3mm x 3mm x 0.3mm	
	Number of Pads	32	

Table 2

Detail of TEG and e-B²it PWB

The environment of analysis is compliant with JESD51 series with regarding the e-B²it PWB as an area array surface mount package device. The e-B²it PWB is mounted on the motherboard with solder paste through peripheral pads, where the shape, dimension and wiring of the test board are followed JESD51-9. The test board is held on the fixture and then set into the enclosure in accordance with JESD51-2. The temperature out of the enclosure is given 25degreesC. The Details of the test board, the fixture and the enclosure are shown in figure 3 and table 3.

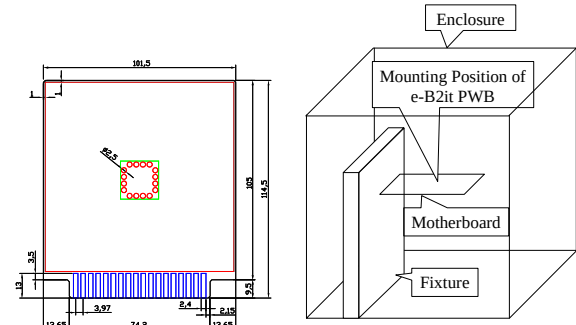


Figure 3

Schematic view of motherboard and environment

Motherboard	Dimension	101.5mm x 114.5mm x 1.6mm	
	Metal Thickness	70um	
Enclosure	Inside Dimension	304.8mm x 304.8mm x 304.8mm	
	Wall	Material	Acrylic Board
		Thickness	3.2mm
Ambient Temperature		25C	

Table 3

Specification of motherboard and environment

III. Result of Analysis and Discussion

Figure 4 shows the dependence of temperature on power consumption with the model shown in figure 1. Figure 5 shows the temperature profile at the power consumption of 1W.

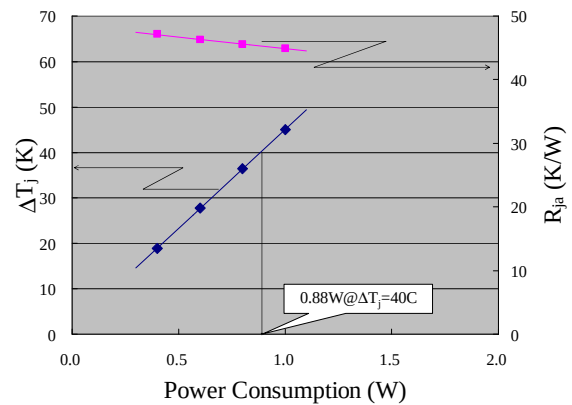


Figure 4

Power consumption dependence of temperature

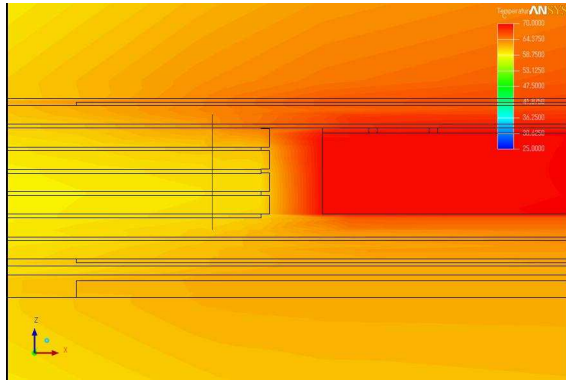
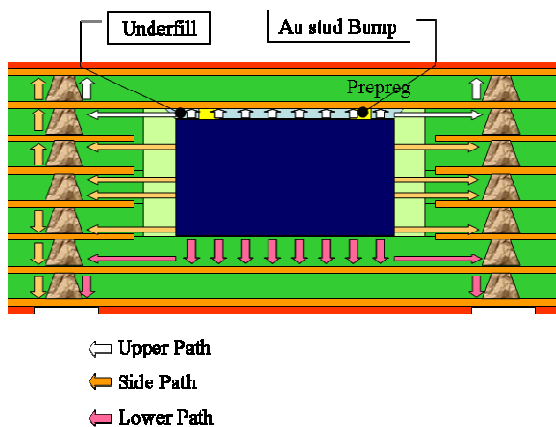


Figure 5

Temperature profile at power consumption=1W

Figure 4 shows that the thermal resistance R_{ja} is 46.2K/W at 1W of the power consumption. The capability of power consumption, which the authors determine the power consumption to rise LSI junction temperature by 40K, is derived 0.88W. The capability is less than expected. In CCD camera modules application, the consumers request to embed LSI, DSP for example, with the power consumption more than 1W. Consequently, the authors consider that it is necessary to improve the power consumption capability more than 20%.

The authors consider dominant thermal paths in the current e-B²it PWB structure as shown in figure 1 to improve thermal performance. There exist 3 dominant thermal paths in e-B²it PWB as shown in figure 6.

Figure 6 Thermal paths in e-B²it PWB

1) Upper Path

The heat conducts from LSI to metal-2 through Au stud bumps and the underfill. The heat broadens horizontally along metal-2. The heat also diffuses on metal-1 through Ag paste bumps and prepreg partially. The heat diffuses on the surface of solder resist-1, and then is removed the natural convection and the thermal radiation.

2) Lower Path

The heat conducts from LSI to prepreg on the bottom of LSI, and then spreads horizontally along metal-7. The heat diffuses to metal-8 through the Ag paste bumps dominantly and prepreg partially. The heat conducts to the motherboard through the solder connection. The heat diffuses on the surface of the motherboard, and then is removed with the natural convection and the thermal radiation.

3) Side Path

Heat flows from LSI through the filling resin around LSI to metal-3, metal-4, metal-5 and metal-6. During diffusing along the metal layers, hotness goes up to the top and/or down to the bottom of e-B²it, then is irradiated with the natural convection and the thermal radiation on the top and transfers to the motherboard.

Figure 7 indicates that there are 2 dominant thermal paths, namely 'Upper Path' and 'Lower Path', in the model shown in figure 6. As shown in figure 7, 53% of generated thermal energy goes out through 'Upper Path'. Additionally, 44% of the thermal energy leaves through 'Lower Path'. On the other hand, the thermal flux along the 'Side Path' is 3% of total energy only. 'Side Path' scarcely contributes on cooling of embedding LSI in this model. The ratio of the heat flow along each path is constant if the power consumption increases.

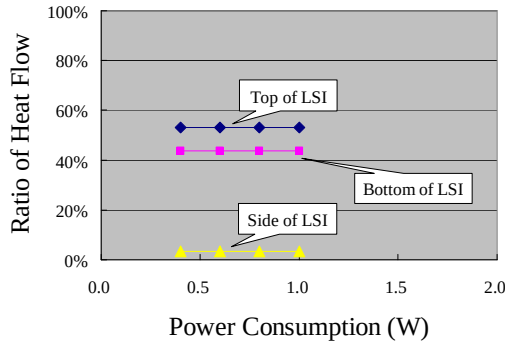


Figure 7

Heat flow ratios on each side of LSI

With consideration for the improving the thermal performance of e-B²it PWB, it is expected very difficult to enhance 'Upper Path' any more. The path owns only 1 exit of heat on the top of e-B²it PWB. The coolability is controlled with the efficiency of heat exchange dominantly on the top, but not the conduction inside. It is denoted with ΔT_t close to ΔT_j and small R_{jt} comparing with R_{ja} as viewed in figure 8. It is almost impossible to develop the efficiency any more, although something like heat sink is attached on the top.

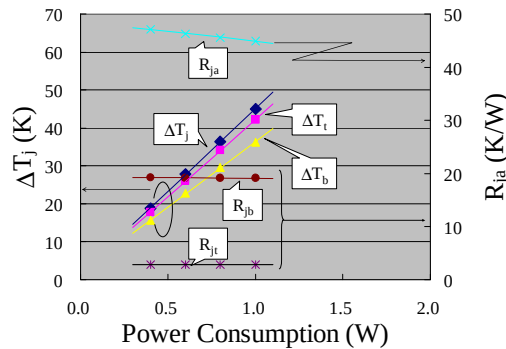


Figure 8

Junction temperature, top temperature, thermal resistance R_{ja} , R_{jt} and R_{jb}

On the other hand, there is large difference between ΔT_j and ΔT_b ; thereby, R_{jb} is large enough to admit improvement. Consequently, the authors focus to improve 'Lower Path' to increase the capability of power consumption.

It is considerable that the improvement affects the

flow along 'Side Path'. The heat along 'Side Path' flows to the bottom through Ag paste bumps, and then conducts to the motherboard. The admittance of improving thermal conductivity along 'Lower Path' also affects the one of 'Side Path'. Therefore, the authors also work over with 'Side Path'.

At the first, the authors consider the enhancing of thermal performance without alternation of material properties. Thus, it is focused to enhance the conductivity from the LSI to metal-3, 4, 5 and 6 with the narrowing of gap between the LSI and the inside edge of the metal layers as shown in figure 1 and 6. It is expected to enhance 'Side Path'.

Figure 9 shows temperature dependence on the gap and figure 10 shows temperature profile where the gap is 250 μ m and 50 μ m.

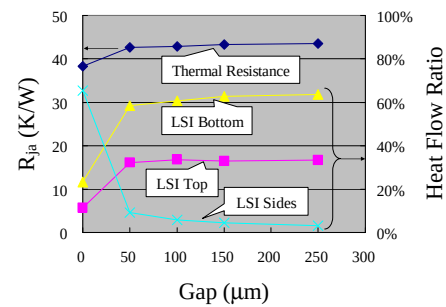


Figure 9

Dependence of thermal resistance on gap width

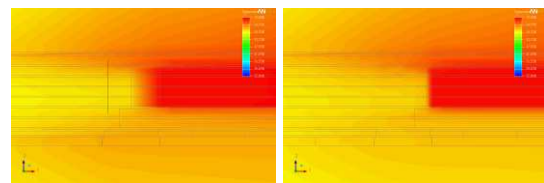
(a) Gap=250 μ m(b) Gap=50 μ m

Figure 10 Temperature profile

It is clear that thermal resistance does not decrease significantly at the gap more than 50 μ m as shown in figure 9. Heat flow ratios on the top, bottom and sides are almost constant in this range. Figure 10 indicates the difference of temperature between LSI and the edge of metal-3, 4, 5 and 6 is large even

where the gap is 50 μm , although the heat looks spreading into metal-3, 4, 5 and 6. Consequently, it is necessary for improving 'Side Path' to reduce the gap less than 50 μm .

It is generally impossible to process the gap 50 μm or less in the commercial production. Consequently, it is resulted that the material around LSI is too thermally resistive to work out the thermal performance with the thinning of the gap. The authors consider that it is necessary to increase thermal conductivity of materials.

The LSI embedded in e-B²it PWB is covered with the prepreg on the bottom, the filling resin of LSI embedding internal cavity on the side and the underfill on the top. These materials are composed of low thermal conductive epoxy resin; the thermal conductivities are less than 1W/mK generally, which are 2 or 3 digits less than the one of metals. It is clear that these thermally resistive materials obstruct the thermal propagation along the thermal paths mentioned above.

The authors evaluate the individual effect of these materials first. Figure 11 shows the results of simulation. The individual increasing of conductivity to 2.0W/mK on the prepreg, the filling resin and the underfill reduces thermal resistance R_{ja} from 46.2K/W with the model shown in figure 1 to 42.7K/W, 43.5K/W and 44.6K/W, i.e. decreasing by 8%, 6% and 2%, respectively. Thus, it is found that the prepreg and the filling resin are key materials to improve the thermal performance in model shown in figure 1. Developing of prepreg enhances thermal conductivity all over in e-B²it PWB, particularly at the contact to LSI bottom, which enhances the heat flow along 'Lower Path'. Increasing the thermal conductivity of the filling resin intensifies the flow from the side of LSI to metal-3, 4, 5 and 6, so that the flow along 'Side Path' increases.

The analysis results that R_{ja} reduces to 39.2K/W, that is, reduction of 13% from the model shown in figure 1, when the thermal conductivities of both prepreg and filling resin are 2.0W/mK.

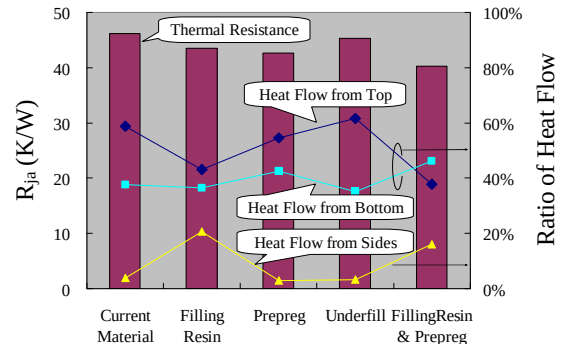


Figure 11

Relation of thermal resistance and thermal conductivity of material around LSI

The underfill does not cause progress obviously. There exists wide heat transmission path on the top of LSI with Au stud bumps in conventional e-B²it PWB structure as shown in figure 1 and figure 6. Consequently, the enlargement on the thermal conductivity with the underfill is not effective method for substantial improvement on thermal performance.

The next stage, the authors work over the thermal broadening of 'Side Path' with thickening of metal-3, 4, 5 and 6 as shown in figure 12. In this discussion, thermal conductivity of the filling resin and the prepreg are assumed 2.0W/mK respectively.

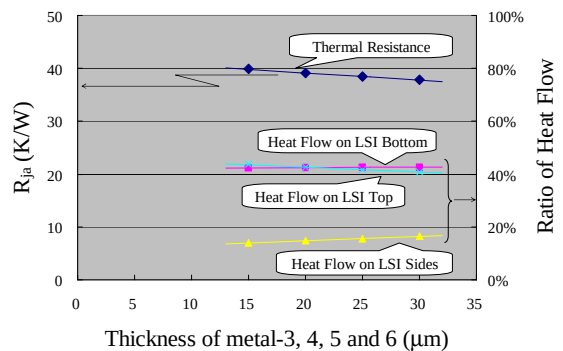


Figure 12

Thermal resistance with thickness of metal-3 to 6

Thermal Resistance R_{ja} reduces to 37.8K/W, reduction by 18%, at 30 μ m of metal thickness as shown in figure 12. The heat flow along 'Side Path' increases with the thickening of the metal layers, and so on 'Lower Path'. Figure 13 shows that the gradient of temperature in e-B²it PWB, conjugated Cu metal thickness in the internal layers of e-B²it PWB from 15 μ m to 30 μ m. Thickening of metal layers brings the broadening of thermal energy in e-B²it PWB, thereby contributes the enlargement effective heat radiation area on the e-B²it PWB and then enhance thermal dissipation performance on heat conduction to the motherboard.

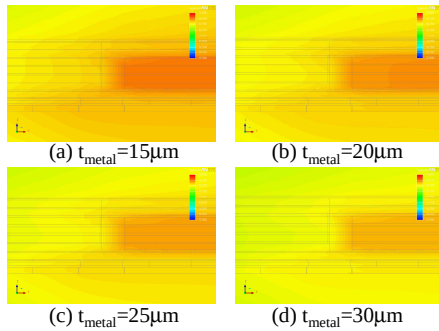


Figure 13

Temperature profile in e-B²it PWB with thickness of metal-3 to 6

It is general that thicker metal layer owns disadvantage in fabrication of metal circuit. The fineness of metal line is inverse proportional to the thickness because of subtractive etching process. Therefore, thick metal layer goes against the trend of the miniaturation in general. However, thick metal layer is adaptable for metal-3 to metal-6 in e-B²it PWB. These layers are not dominant wiring layer; the signal routing is primarily carried on with metal-1, 2 and 7. Thus, it is possible for metal-3 to metal-6 to specialize for thermal conduction without degrading the design rules.

Finally, the authors also discuss the further improvement of the thermal diffusion from the LSI to metal-3, 4, 5 and 6. It is discussed to embed a

heat spreader in e-B²it PWB with foresaid thermal conductivity of the materials, that is, the thermal conductivity of the filling resin and prepreg are assumed 2.0W/mK.

Figure 14 shows the schematic of the altered e-B²it PWB with embedded heat spreader. The heat spreader is attached on the backside of the LSI through the heat conductive thermo-setting epoxy film, and then mounted on insulator-5. The thickness of the heat spreader is assumed the same as the inner metal layers. The depth of the heat spreader in e-B²it PWB is similar to metal-6 where the distance between the inside edge of metal-6 and the spreader is 50 μ m. Consequently, the heat flows from LSI to metal-6 through the heat spreader.

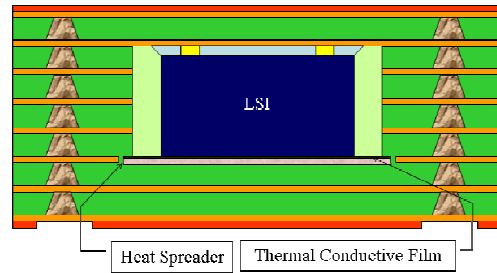


Figure 14

Heat spreader embedded in e-B²it PWB

Figure 15 and 16 show the result of the simulation. Figure 15 shows that the thermal resistance decreases to 37.0K/W, i.e. by 20% and 34.3K/W, by 26%, where the thickness of metal-3 to metal-6 is 15 μ m and 30 μ m, respectively. The capability of power consumption increases to 1.05W and 1.13W, by 19% and 28%, as shown in figure 16 where the thickness of metal is 15 μ m and 30 μ m respectively. The capability exceeds more than 1W, which the authors consider as the goal.

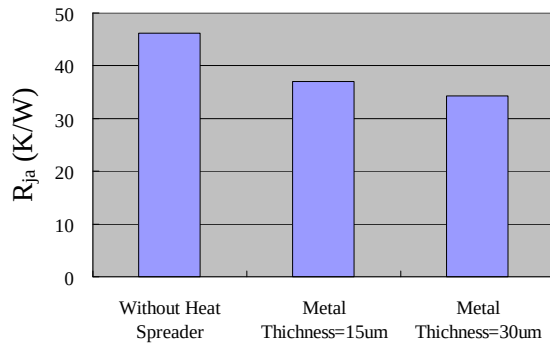


Figure 15

Thermal performance with embedded heat spreader

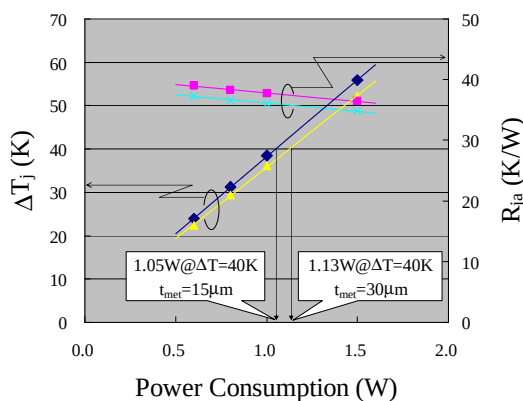


Figure 16

Capability of power consumption in thermal performance enhanced e-B²it PWB

IV. Conclusion

The authors investigate enhancing thermal conduction path in e-B²it PWB on CFD analysis. It is resulted as follows,

- The capability of power consumption improves from 0.88W to 1.13W, by 28% totally with embedding heat spreader in e-B²it PWB, thickening of metal layers and enhancing the thermal conductivity of the prepreg and the filling resin of LSI embedding internal cavity. The thermal resistance decreases by 26%. That is, the authors accomplish the target to exceed the capability more than 1W.
- Thermal resistance reduces by 18% with the

thickening of internal metal layers and enhancing the thermal conductivity of the prepreg and the filling resin.

- The adapting of thermally improved the prepreg and the filling resin reduces the thermal resistance by 13%.

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