

# Critical Issues of 3D High-Performance IC Integrations

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## ABSTRACT

Moore's law has been the most powerful driver for the development of the microelectronic industry. This law emphasizes on lithography scaling and integration (in 2D) of all functions on a single chip, perhaps through system-on-chip (SoC). On the other hand, the integration of all these functions can be achieved through system-in-package (SiP) or, ultimately, 3D IC integration. There are many critical issues of 3D IC integration, especially for 3D high-performance IC integrations. In this study, some of the critical issues of 3D high-performance IC integrations will be discussed and some potential solutions or research problems will be proposed.

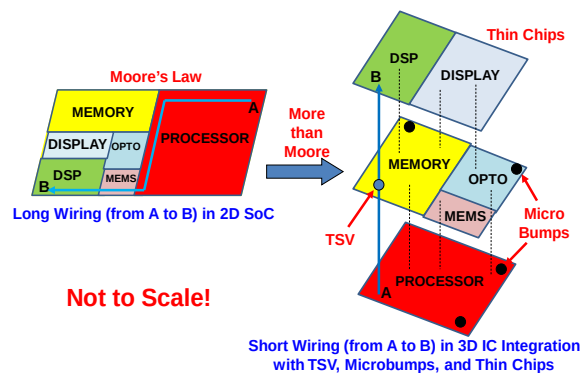
**Key Words:** 3D IC integration, TSV with RDL, solder microbumps, MEOL, thin wafer handling, and thermal management

## Introduction

The invention of the bipolar junction transistor and the junction field-effect transistor by Bardeen, Brattain, and Shockley in 1956 foreshadowed the development of generations of computer and smart phones yet to come. The invention of the silicon integrated circuit (IC) by Jack Kilby of Texas Instruments in 1958 and 6 months later by Robert Noyce of Fairchild Semiconductor excited the development of generations of integrations. The proposal (for minimum cost) of doubling the number of transistors on an IC every 24 months by Gordon Moore in 1965 (also called Moore's law) has been the most powerful driver for the development of the microelectronic industry in the past 44 years. This law emphasizes on lithography scaling and integration (in 2D) of all functions on a single chip, through system-on-chip (SoC).

On the other hand, integration of all these functions can be achieved through system-in-package (SiP) or, ultimately, 3D IC integration, which is one of the "More-than-Moore". Based on the silicon platform technology, anything that involves the integration of electronics, photonics, mechanics, chemistry, heat, magnetic, biology, etc., for functionality and system performance when interacting with people and the environment, is known as "More-than-Moore".

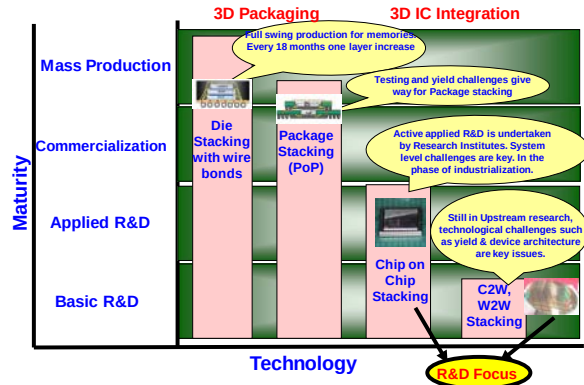
3D IC Integration is the key technology for electronic products which must meet the following requirements:



**Fig. 1 Moore's law (2D SoC) vs. More-than-Moore (3D IC Integration)**

- (1) Form Factor – Smaller is Better, e.g., PDAs, cameras, Mobiles (COMS image sensors)
- (2) Performance – Faster is Better, e.g., shorten local and global interconnect lengths.
- (3) Cost – Cheaper is Better, e.g., system improvements without the high-cost of scaling.
- (4) Reliability – Low-risk is Better, e.g., it still works after drops.

The Holy Grail of 3D IC integration (e.g., heterogeneous integration) is shown in Figure 1, where all the chips, e.g., microdisplay, MEMS, memory, microprocessor, optoelectronic, multiple outputs dc-dc converter, digital signal processor, microbattery, and analog-to-digital (A/D) mixed signal are combined and stacking in three dimensions. It can be seen that, in



**Fig. 2 3D packaging technologies**

general the electrical performance of 3D IC integration is better than that of 2D SoC. However there are many critical issues in questing for the Holy Grail. Some of the critical issues will be discussed and some potential solutions or research problems will be proposed in this study.

### 3D Packaging

Figure 2 shows 4 groups of 3D packaging technologies, namely: (1) chip stacking with wirebonds; (2) package-on-package (PoP); (3) chip-to-chip (C2C) bonding; and (4) chip-to-wafer (C2W) and wafer-to-wafer (W2W) bonding. It can be seen that (1) and (2) are mature technologies and in mass production, and they are called 3D packaging. (3) and (4) are considerably new technologies and are called 3D IC integration. In (4) because of the difference in chip size and yield, C2W bonding is usually used more often than W2W bonding.

### FEOL, BEOL, and MEOL

FEOL (Front End of Line) is usually performed in wafer fabs (to pattern the active devices, e.g., transistors, resistors, etc.) and the process is from a bare wafer to passivation, which covers everything except the bonding pads for the next level of interconnect. BEOL (Back End of Line) is usually performed in packaging assembly and test houses and it involves everything after passivation, e.g., UBM (under bump metallurgy), wirebonding, metallization, wafer bumping, backgrinding, and dicing. MEOL (Mid-End of Line) is usually performed by integrating the FEOL and BEOL technologies into a 3D IC integration technology which involves, e.g., TSV, microbumps, thin-wafer handling, metallization, UBM, wafer bumping, backgrinding, and dicing.

### Critical Issues of 3D IC Integration

Just as with many other new technologies, 3D IC integration still faces many critical issues. In the development of 3D IC integration, the following must be noted and understood: [1-24]

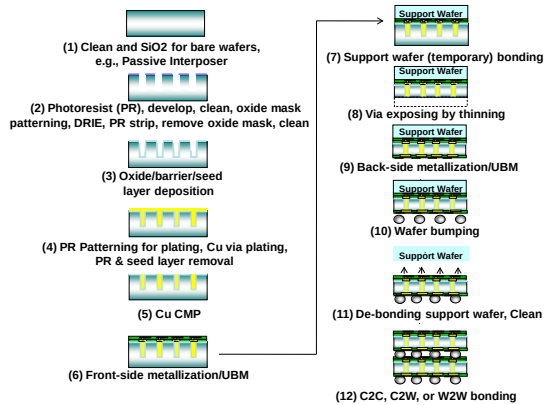
- (1) Design guidelines and software are not available.
- (2) Test methods and equipment are lacking.
- (3) Known good dies (KGDs) are required.
- (4) Through-silicon vias (TSV) with redistribution layers (RDL) usually are required.
- (5) Microbumps usually are required.
- (6) Wafer thinning and thin-wafer handling during processing are necessary.
- (7) High equipment accuracy is necessary for alignments.
- (8) Fast chips must be mixed with slow chips.
- (9) Large chips must be mixed with small chips.
- (10) 3D IC stacking inspection methodology is needed.
- (11) 3D IC stacking expertise is lacking.
- (12) 3D IC stacking infrastructure is lacking.
- (13) 3D IC stacking standards are lacking.
- (14) Thermal issues: the heat flux generated by stacked multifunctional chips in miniature packages is extremely high.
- (15) Thermal issues: 3D circuits increase total power generated per unit surface area.
- (16) Thermal issues: chips in the 3D stack may be overheated if proper and adequate cooling is not provided.
- (17) Thermal issues: the space between the 3D stack may be too small for cooling channels (i.e., no gap for fluid flow).
- (18) Thermal issues: thin chips may create extreme conditions for on-chip hot spots.

In this study, the focuses are on TSV with RDL, thin wafer handling, low-cost solder micro bumps, and thermal management.

### TSV with RDL

The most important key enabling technology for 3D IC integration is TSV with RDL. It provides advanced vertical interconnects and system-in-package (SiP) solutions such as C2C, C2W, and W2W stacking; wafer-level packaging and redistribution; interposer packaging; and the shortest electrical path (vertical electrical feedthrough) between two sides of a silicon "chip or interposer." Just as with many other new technologies, TSVs still face many critical issues. In the development of TSVs, the following must be noted and understood. [1-24]

- (1) TSV cost is higher than that of wire bonding, at least for now.
- (2) The only TSV volume product is CMOS image sensors.
- (3) Memories have just been talked about.
- (4) High-speed logic and processor will come even later.
- (5) TSV design softwares are lacking.

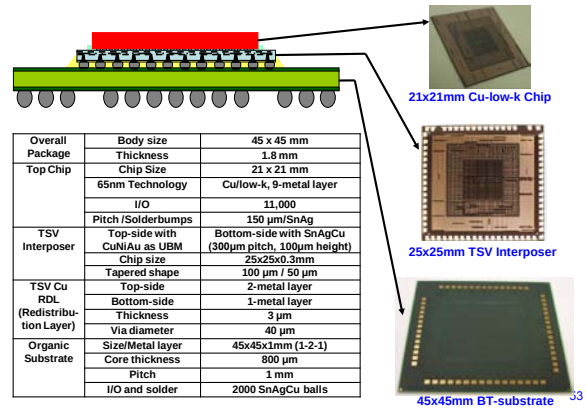


**Fig. 3 The most likely manufacturing process of TSV with RDL for 3D IC integration**

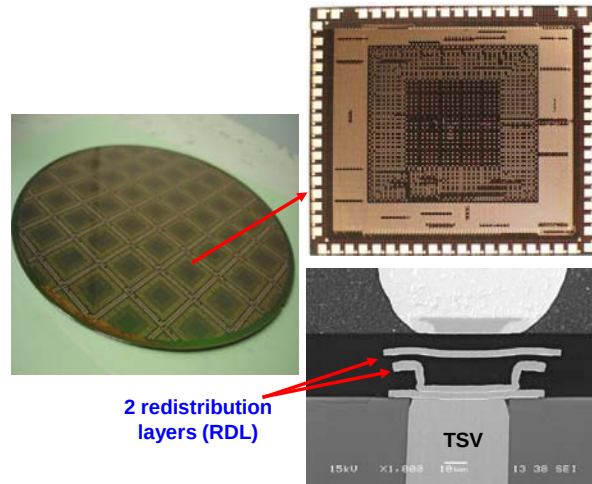
- (6) TSV design guidelines are not commonly available.
- (7) Copper filling helps on thermal problems but increases TCE (thermal coefficient of expansion).
- (8) Void-free copper filling usually takes a long time (low throughputs).
- (9) TSV wafer yields are high (>99.8%) owing to the large number of vias.
- (10) TSV wafer warpage is a problem owing to due to the TCE mismatch between the silicon and copper.
- (11) Thin TSV wafer handling is necessary during all the processes.
- (12) TSV with high aspect ratios are difficult to manufacture at high yield.
- (13) Test methodology and softwares for TSV are lacking.
- (14) High-volume production tools are lacking and/or expensive.
- (15) TSV inspection methodology and softwares are lacking.
- (16) TSV expertises, infrastructure, and standards are lacking.

There are many ways to make the TSV with RDL for 3D IC integration and the most likely one (or the one will be used the most) is shown in Figure 3. It can be seen that there are 5 key steps to make the TSV, namely (1) via formation, (2) SiO<sub>2</sub> deposition, (3) barrier and seed layers deposition, (4) Cu plating, and (5) CMP (chemical and mechanical polishing) of Cu plating residues. It should be noted that for bare wafers, a SiO<sub>2</sub> layer is needed before the photoresist, e.g., passive interposers. For active memory chips and active interposers (e.g., ASIC and processor) because of their passivation layer, only cleaning is needed. The front-side metallization/UBM can be made next on the blind TSV wafer which is ~700μm thick.

In most of the 3D IC integration applications, the thickness of the passive/active interposers is ranging



**Fig. 4 A high-performance chip supported by a TSV interposer soldered on a BT-substrate and then solder balled on a PCB**



**Fig. 5 TSV with RDL wafer made by the process shown in Figure 3**

from 100μm to 200μm and the stacking chips (e.g., memory) is ranging from 25μm to 50μm. Thus, a support wafer is needed for the remaining processes.

As soon as the support wafer is temporary bonded to the blind TSV wafer, it can be thinned down to expose the TSV. Then it is followed by the back-side metallization/UBM and wafer bumping. After that, the support wafer is de-bonded from the TSV with RDL wafer. Finally, the TSV with RDL wafer is ready for either W2W bonding or diced into individual chips for C2C or C2W bonding.

Today, all the steps on the left-hand side of Figure 3 are under controlled (even there are rooms for improvements) by the industry. However, all the steps on the right-hand side of Figure 3 require more R & D efforts because of the (tiny) thickness of the TSV with RDL wafer which is required by 3D IC integration applications.

Figure 4 shows a high performance chip which (cannot be supported by the BT-substrate) is supported

by a passive TSV interposer with two redistribution layers on top and one at the bottom [13]. A very simple BT-substrate is used to fan-out all the I/Os, powers and grounds to the PCB. Figure 5 shows the TSV with RDL wafer and the chip with its cross section clearly showing the two RDLs on the top-side of the interposer [13].

The TSV size should be as small as possible ( $\leq 30\mu\text{m}$ ). Because (1) less thermal expansion mismatch between the Si and Cu, (2) less Cu plating, (3) higher throughput, and (4) more space for routing, 5 to  $10\mu\text{m}$  vias are not uncommon.

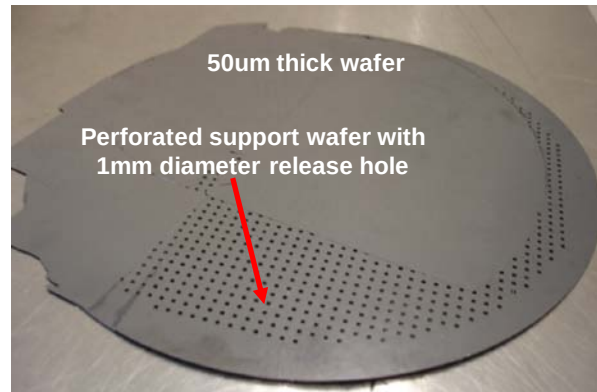
### Thin Wafer Handling

In order to have low-profile products with 3D IC integration technology, the thickness of the chips/wafers is usually very thin. Making the wafer thin is not a big problem. Most of the back-grinding machines (e.g., Disco) can do the job and grind the wafers to as thin as  $5\mu\text{m}$ . However, handling thin wafers through all the semiconductor fabrication and packaging assembly processes is difficult. Usually, the thin-device wafer is temporarily bonded on a support wafer. Then it goes through all the semiconductor fabrication processes, such as metallization, passivation, UBM, and the packaging processes, such as backgrinding and solder bumping. After all these are done, removing the thin wafer from the support wafer poses another big challenge. This study discusses a few methods for handling thin wafers.

The new 3M wafer support system [25] which enables conventional back-grinding equipment to be used to produce wafers with a final thickness as low as  $20\mu\text{m}$ . The key to the 3M system is its ability to provide a rigid, uniform support surface to minimize stress on the wafer as the silicon is removed, resulting in less cracking and chipping. The system includes both the equipment and consumables [3M UV-Curable Liquid Adhesive LC-2201, glass support plate (typically recycled, can be reused many times), and 3M light-to-heat Conversion Solution] necessary for mounting, demounting, and removing adhesive from the wafer.

In the 3M system, a glass plate is used to support the wafer through the back-grinding process. An ultraviolet (UV)-curable liquid adhesive is used as the bonding agent between the device wafer and the glass plate (support wafer). After the backgrinding process the thinned device wafer is transferred onto a dicing tape, and the support glass is removed by laser debonding of the adhesive-glass interface using a light-to-heat conversion (LTHC) layer. The adhesive then can be removed from the wafer, leaving behind fewer residues than seen with typical backgrinding tapes. This system also works for other semiconductor and packaging processes as long as the thermal-expansion mismatch between the device wafer and the glass plate is within the allowable tolerance.

EVG and Brewer Science have developed a solution that enables temporary bonding of a device



**Fig. 6 A simple support wafer method for thin wafer handling**

wafer to a right carrier substrate (support wafer) and allows not only thinning but also a full range of subsequent processes, including high-temperature deposition, etching, lithography, dielectric application and curing, plating, and chemical cleaning, [26]. **Temporary Bonding** The front side of the device wafer and the support wafer are coated with the WaferBOND, an HT Brewer Science adhesive material, by using a coating chamber that includes spin and spray coat capability. Both wafers then are transferred to a bond chamber, where they are carefully centered and vacuum bonded at elevated temperatures. Once the device wafer is temporarily bonded to the support wafer, it is ready for backside processing, including back-grinding, etching, metallization, TSV formation, etc.

**Debonding** During the debonding process, the thin wafer is debonded first via a thermally activated slide lift-off approach from the support wafer, cleaned in a single-wafer cleaning chamber to remove the remaining adhesive residues, and then transferred to the appropriate output format, such as a film-frame carrier, a dedicated wafer cassette, or a coin-stack packing canister. The support wafer is also cleaned and then can be reused immediately for another debonding process.

A simple support-wafer method for thin wafer ( $50\mu\text{m}$ ) handling is shown in Figure 6 [27]. One of the key problems encountered in the support-wafer method is wafer debonding. The  $50\mu\text{m}$ -thick device wafer is easily broken during the wafer debonding process. This key problem is resolved by optimizing the wafer debonding process to minimize residual stress. The first step is to reduce the pitch of the release hole on the perforated support wafer from 3.5 to 2 mm. The second step is to increase the number of perforations on the edge of the support wafer. These two optimized debonding methods allow more chemical solution to uniformly penetrate into the bonding adhesive and eventually debonded the wafers successfully.

For example, the thin ( $50\mu\text{m}$ ) device wafer is attached to a support wafer and is handled and put in the

PECVD chamber for SiO<sub>2</sub> deposition. No wafer cracking is observed during wafer handling and after silicon oxide deposition. Thus thin-wafer handling using the support-wafer method is highly recommended. Some engineering and process development are required, though.

### Low-cost Lead-Free Solder Microbumps

As mentioned earlier, the thickness of chips for 3D IC integration application is very thin and thus the conventional flip chip solder bumps ( $\sim 100\mu\text{m}$ ) cannot be used for connecting the thin chips. Instead, very tiny bumps in the range of 20 to 30  $\mu\text{m}$  are needed. Figure 7 [22] shows the cross sections of the bonding of two Si chips (the bottom one is with TSVs). It can be seen that the lead-free solder is pure Sn, the pitch is 15  $\mu\text{m}$ , and the circular pad is only 8  $\mu\text{m}$ .

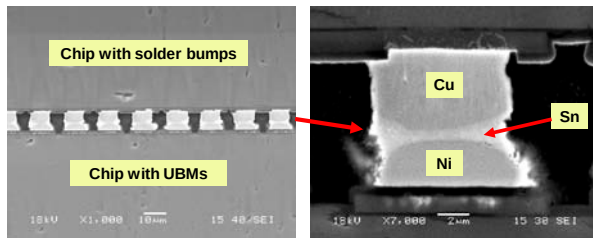


Fig. 7 SEM images of the assembly cross section of an Si chip and Si carrier with TSV

Underfill is usually needed between two chips with one with Cu-plated TSV because of the thermal expansion mismatch [7, 21]. (The equivalent CTE of a copper-filled TSV silicon chip could be as high as  $10 \times 10^{-6}/^\circ\text{C}$ .) Due to the very tiny gap between the chips, smaller filler sizes underfills (Max  $\leq 3\mu\text{m}$  and Ave  $\leq 0.5\mu\text{m}$ ) are required.

### Thermal Management of 3D IC Integration

As mentioned earlier that thermal management of 3D IC integration system is very important. Two examples are shown in this study. For other results, please see [20]. Figure 8 shows the temperature maps on a chip for various chip thicknesses. It can be seen that the heat on the chip surface is well dissipated for typical chip thicknesses of 100 to 200  $\mu\text{m}$  subjected to a generated power of 0.2W. For the 200  $\mu\text{m}$ -thick chip, the temperature distribution is almost uniform and equal to 35  $^\circ\text{C}$ . However, the hot-spot temperature on the chip increases to 69  $^\circ\text{C}$  (0.2W power) if the chip thickness is reduced to 10  $\mu\text{m}$ , and the hot-spot area is clearly shown.

Figure 9 shows the effect of two heat sources at a distance apart (gap) on the thermal performance of two stacked copper-filled TSV chips. There are two distinct heat sources (each with 0.1W and on 0.2x0.2mm area) on each chip (5x5x0.05mm). It can be seen from the left-hand side and upper curve of the figure that (1) the larger the gap ( $b/a \leq 0.7$ ) between the two heat sources, the better is the thermal resistance, and (2) when the gap

between the two heat sources is larger than 0.7 (i.e., the heat sources are too close to the edge of the chip), the thermal performance is weaker. This is due to suppressible spreading effects near the edges of the chips.

In addition to the case of overlapping heat sources discussed in the preceding paragraph, the orientation effect (staggered heat sources) of two stacked chips, each with two heat sources at a certain distance apart, on the thermal performance of a 3D SiP is presented in the right-hand side and lower curve of Figure 9. It can be seen that (1) similar to case of overlapping heat sources, the larger the gap ( $b/a \leq 0.7$ ) between those two pairs of staggered heat sources, the lower are the maximum junction temperature and thermal resistance, (2) when the gap between the two pairs of staggered heat sources is larger than 0.7 (i.e., the heat sources are too close to the edge of the chip), the thermal performance is weaker, and (3) the maximum thermal resistance of the 3D SiP with two TSV chips subjected to two pairs of staggered heat sources are lower than those with two pairs of overlapping heat sources. This is so because the staggered heat sources avoid the superimposition of heat sources and thus lead to better thermal performance. This result is very useful for the design and layout 3D SiP because it permits relocation of the heat sources and/or rotation of the chip.

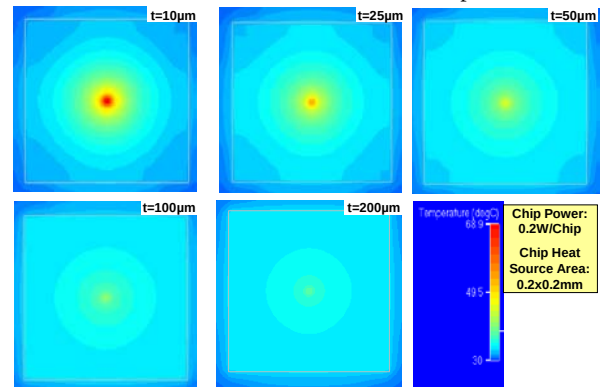


Fig. 8 Temperature maps on the chip for various chip thickness (hot spots)

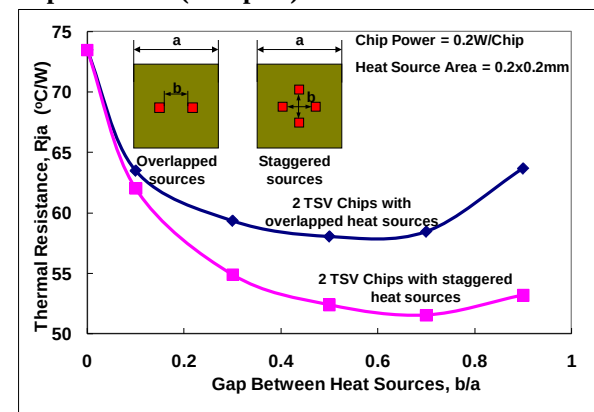


Fig. 9 Thermal resistance of a 3D integration of two Cu-filled TSV chips subjected to two distinct overlapped heat sources and staggered heat sources

## Summary and Recommendations

Some critical issues (challenges and opportunities) of 3D IC integration have been discussed and some potential solutions or research problems have also been proposed in this study. Some important results and recommendations are summarized in the following.

- (1) 3D IC integration is the key technology for electronic products which must meet the requirements of form-factor, performance, cost, and reliability.
- (2) 3D IC integration (MEOL) technology integrates the FEOL and BEOL and thus has to be performed in the fab.
- (3) TSV with RDL, thin wafer handling, microbump, and thermal management are the most important key enabling technologies for 3D IC integration.
- (4) TSV size should be as small as possible ( $\leq 30\mu\text{m}$ ). 5 to  $10\mu\text{m}$  are not uncommon.
- (5) The thickness of the passive/active interposers (e.g., ASIC and processor) is ranging from 100 to  $200\mu\text{m}$  and of the stacking chips (e.g., memory) is ranging from 25 to  $50\mu\text{m}$ .
- (6) The size of low-cost micro bumps connecting the thin chips should be ranging from 20 to  $30\mu\text{m}$ .
- (7) The most likely manufacturing process of TSV with RDL for most 3D IC integrations is shown in Figure 3.
- (8) A support wafer is necessary for thin wafer handling.
- (9) More works need to be done on low-cost thin wafer handling.
- (10) More works need to be done on the methods to strengthening the thin wafers.
- (11) More works need to be done on low-cost lead-free micro bumps.
- (12) More works need to be done on thermal management of 3D IC integration systems.
- (13) TSV with RDL opened the door for many new and useful applications, e.g., stacking up the chips and letting them talk to each other through the vias at the shortest distance possible, which we won't even dare to think of a few years ago. It is an exciting time for 3D IC integration!

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## References

- 1 Andry, P. S., Tsang, C. K., Webb, B. C., Sprogis, E. J., Wright, S. L., Bang, B., and Manzer, D. G. "Fabrication and characterization of robust

through-silicon vias for silicon-carrier applications." *IBM Journal of Research and Development* 52:571–581, 2008.

- 2 Knickerbocker, J. U., Andry, P.S., Dang, B., Horton, R. R., Patel, C. S., Polastre, R. J., Sakuma, K., Sprogis, E. S., Tsang, C. K., Webb, B. C., and Wright, S. L. "3-D silicon integration." *IEEE Proceedings of Electronic Components and Technology Conference*, Orlando, FL, May 2008, pp. 538–543.
- 3 Kumagai, K., Yoneda, Y., Izumino, H., Shimojo, H., Sunohara, M., and Kurihara, T. "A silicon interposer BGA package with Cu-filled TSV and multilayer Cu-plating interconnection." *IEEE Proceedings of Electronic Components and Technology Conference*, Orlando, FL, May 2008, pp. 571–576.
- 4 Sunohara, M., Tokunaga, T., Kurihara, T., and Higashi, M., "Silicon interposer with TSVs (through-silicon vias) and fine multilayer wiring." *IEEE Proceedings of Electronic Components and Conference*, Orlando, FL, May 2008, pp. 847–852.
- 5 Lee, H. S., Choi, Y.-S., Song, E., Choi, K., Cho, T., and Kang, S. "Power delivery network design for 3D SIP integrated over silicon interposer platform." *IEEE Proceedings of Electronic Technology Components and Technology Conference*, Reno, NV, May 2007, pp. 1193–1198.
- 6 Matsuo, M., Hayasaka, N., and Okumura, K. "Silicon interposer technology for high-density package." *IEEE Proceedings of Electronic Components and Technology Conference*, Las Vegas, NV, May 2000, pp. 1455–1459.
- 7 Selvanayagam, C., Lau, J. H., Zhang, X., Seah, S., Vaidyanathan, K., and Chai, T. "Nonlinear thermal stress/strain analysis of copper filled TSV (through silicon via) and their flip-chip microbumps." *IEEE Proceedings of Electronic Components and Technology Conference*, Orlando, FL, May 2008, pp. 1073–1081.
- 8 Wong, E., Minz, J., and Lim, S. K. "Effective thermal via and decoupling capacitor insertion for 3D system-on-package." *IEEE Proceedings of Electronic Components and Technology Conference*, San Diego, CA, May 2006, pp. 1795–1801.
- 9 Khan, N., Rao, V., Lim, S., Ho, S., Lee, V., Zhang, X., Yang, R., Liao, E., Ranganathan, N., Chai, T., Kripesh, V., and Lau, J. H. "Development of 3D silicon module with TSV for system in packaging." *IEEE Proceedings of Electronic Components and Technology Conference*, Orlando, FL, May 27–30, 2008, pp. 550–555.

- 10 Ho, S., Yoon, S., Zhou, Q., Pasad, K., Kripesh, V., and Lau, J. H. "High rf performance TSV for silicon carrier for high frequency application." *IEEE Proceedings of Electronic Components and Technology Conference*, Orlando, FL, May 27–30, 2008, pp. 1956–1952.
- 11 Premachandran, C., Rangnathan, N., Mohanraj, S., Chong Ser Choong, and Iyer, M. K. "A vertical wafer level packaging using through hole filled via interconnect by lift off polymer method for MEMS and 3D stacking applications." *Proceedings of the Fifty-first Electronic Components and Technology Conference*, Lake Buena Vista, FL, 2005, pp. 1094–1098.
- 12 Chen, K. S., Ayon, A. A., Zhang, X., and Spearing, S. M. "Effect of process parameters on the surface morphology and mechanical performance of silicon surfaces after deep reactive ion etching (DRIE)." *J. Microelectromech. Syst.* 11:264–275, 2002.
- 13 Zhang, X., Chai, T., Lau, J. H., C. Selvanayagam, K. Biswas, S. Liu, D. Pinjala, G. Tang, Y. Ong, S. Vempati, E. Wai, H. Li, B. Liao, N. Ranganathan, V. Kripesh, J. Sun, J. Doricko, and C. Vath. "Development of through silicon via (TSV) interposer technology for large die (21 × 21 mm) fine-pitch Cu/low-k FCBGA package." *IEEE Proceedings of Electronic Components and Technology Conference*, San Diego, CA, May 2009, pp. 305–312.
- 14 Hu, G., Kalyanam, H., Krishnamoorthy, S., and Polka, L. "Package technology to address the memory bandwidth challenge for tera-scale computing." *INTEL Technol. J.* 11:197–206, 2007.
- 15 Knickerbocker, J. U., Andry, P. S., Buchwalter, L. P., Deutsch, A., Horton, R. R., Jenkins, K. A., Kwark, Y. H., McVicker, G., Patel, C. S., Polastre, R. J., Schuster, C., Sharma, A., Sri-Jayantha, S. M., Surovic, C. W., Tsang, C. K., Webb, B. C., Wright, S. L., McKnight, S. R., Sprogis, E. J., and Dang, B. "Development of next-generation system-on-package (SOP) technology based on silicon carriers with fine-pitch interconnection." *IBM J. Res. Dev.* 49:725–754, 2005.
- 16 Tomita, Y., Morifuji, T., Ando, T., Tago, M., Kajiwar, R., Nemoto, Y., Fujii, T., Kitayama, Y., and Takahashi, K. "Advanced packaging technologies on 3D stacked LSI utilizing the micro interconnections and the layered microthin encapsulation." *Proceedings of the Fifty-first Electronic Components and Technology Conference*, Orlando, FL, 2001, pp. 353–360.
- 17 Choi, W. K., Premachandran, C., Ong, C., Ling, X., Liao, E., Khairiyanto, A., Chne, K., Thaw, P., and Lau, J. H. "Development of novel intermetallic joints using thin film indium based solder by low temperature bonding technology for 3D IC stacking." *IEEE Proceedings of Electronic Components and Technology Conference*, San Diego, CA, May 2009, pp. 333–338.
- 18 Takahashi, K., Umemoto, M., Tanaka, N., Tanida, K., Nemoto, Y., Tomita, Y., Tago, M., and Bonkohara, M. "Ultra-high-density interconnection technology of three-dimensional packaging." *Microelectronics Reliability* 43:1267–1279, 2003.
- 19 Lau, J. H., Lim, Y., Lim, T., Tang, G., Khong, C., Zhang, X., Ramana, P., Zhang, J., Tani, C., Chandrappan, J., Chai, J., Li, J., Tangdionga, G., and Kwong, D. "Design and analysis of 3D stacked optoelectronics on optical printed circuit boards." *Proceedings of SPIE, Photonics Packaging, Integration, and Interconnects VIII*, San Jose, CA, January 19–24, 2008, Vol. 6899, pp. 07.1–07.20.
- 20 Lau, J. H., and Tang, G. "Thermal management of 3D IC integration with TSV (through silicon via)." *IEEE Proceedings of Electronic Components and Technology Conference*, San Diego, CA, May 2009, pp. 635–640.
- 21 Yu, A., Kumar, A., Ho, S., Wai, H., Lau, J. H., Khong, C., Lim, S., Zhang, X., Yu, D., Su, N., Chew, M., Ching, J., Tan, T., Kripesh, V., Lee, C., Huang, J., Chiang, J., Chen, S., Chiu, C., Chan, C., Chang, C., Huang, C., and Hsiao, C., "Development of fine pitch solder microbumps for 3D chip stacking." *IEEE Proceedings of Electronic Packaging and Technology Conference*, Singapore, December 2008, pp. 387–392.
- 22 Yu, A., Lau, J. H., Ho, S., Kumar, A., Wai, Y., Yu, D., Jong, M., Kripesh, V., Pinjala, D., Kwong, D., "Study of 15-μm-pitch solder microbumps for 3D IC integration." *IEEE Proceedings of Electronic Components and Technology Conference*, San Diego, CA, May 2009, pp. 6–10.
- 23 Yu, A., Lau, J. H., Ho, S., Kumar, A., Yin, H., Ching, J., Kripesh, V., Pinjala, D., Chen, S., Chan, C., Chao, C., Chiu, C., Huang, M., and Chen, C., "Three dimensional interconnects with high aspect ratio TSVs and fine pitch solder microbumps." *IEEE Proceedings of Electronic Components and Technology Conference*, San Diego, CA, May 2009, pp. 350–354.
- 24 Yu, A., Khan, N., Archit, G., Pinjalal, D., Toh, K., Kripesh, V., Yoon, S., and Lau, J. H. "Development of silicon carriers with embedded thermal solutions for high power 3-D package." *IEEE Transactions on Components and Packaging Technology*, Vol. 32, No. 3, September 2009, pp. 566–571.
- 25 [www.3m.com/electronicmaterial](http://www.3m.com/electronicmaterial).

- 26 Pargfrieder, S., Kettner, P., Privett, M., and Ting, J. "Temporary bonding and debonding enabling TSV formation and 3D integration for ultra-thin wafers." *Proceedings of the 10th IEEE Electronics Packaging Technology Conference*, Singapore, December 2008, pp. 1301–1305.
- 27 Zhang, X., Kumar, A., Zhang, Q., Ong, Y., Ho, D., Khong, C., Kripesh, V., Lau, J., H., Kwong, D., Sundaram, V., and Tummula, R. "Application of piezoresistive stress sensors in ultra thin device handling and characterization." *Proceedings of Eurosensors Conference*, Dresden, Germany, September 7–10, 2008, pp. 1022–1026.