

Wafer Level Batch Fabrication of Silicon Microchannel Heat Sink and Electrical Through-Silicon Vias for 3D ICs

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Abstract

Cooling and power delivery are among the key challenges in three dimensional (3D) integration of high-performance ICs. We investigate various CMOS compatible approaches to integrate microchannel heat sinks and through-silicon vias (TSVs) to enable fluidic and electrical interconnections in a 3D stack of ICs. Microchannels are etched and capped using low temperature processes such as adhesive bonding or silicon-to-silicon (Si-Si) direct bonding techniques. After thinning the capping layer, TSVs are etched in the fins of the parallel microfluidic cooling channels. Using the mesh process discussed in the paper, the pinch off time for TSVs is reduced. Subsequently, high aspect ratio (10:1) TSVs are filled with copper using bottom up electroplating process. Solder bumps and polymer pipes can be used for electrical interconnections as well as fluid inlet/outlet ports to the substrate. Potential trade-offs that have to be considered while integrating electrical and fluidic interconnects in a wafer are also described in the paper.

Key words: Microchannel heat sink, through-silicon via, 3D integration

I. INTRODUCTION

Historically, advances in the field of packaging and system integration have not progressed at the same rate as ICs [1]. To keep up with ever increasing system integration demands, it is imperative that developments in silicon ancillary technologies be accelerated. To this end, 3D integration ushers a new era of technology convergence between on-chip interconnects and packaging [2]. 3D stacking enables reduced latency and increased bandwidths due to shorter interconnects and lower parasitics and offers lower energy per bit, increased device density, and heterogeneous integration [3]. Although 3D ICs are available commercially, they are mainly limited to stacking of memory and other low power ICs. With growing interest in 3D integration, it is important to understand the key issues involved in stacking chips - high performance as well as memory applications. In order to scale high performance processors and memory in the vertical dimension, certain challenges must be overcome.

The first challenge is the fabrication of reliable and low cost TSVs. This is important as it allows signaling and power delivery in a 3D stack of chips. The second challenge is heat removal. As a first order approximation, an n -tier 3D chip would generate n times the power density as compared to 2D chip having identical characteristics. It is known that the performance and power dissipation of ICs are influenced by

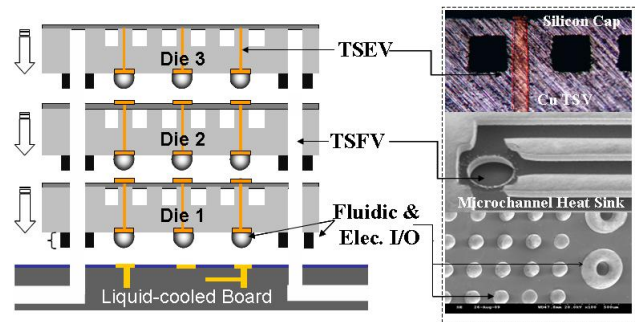


Fig. 1. Schematic of proposed chip-scale microchannel heat sink for 3D integrated circuits

temperature and the surrounding thermal environment. The cooling issue is already plaguing 2D IC systems, and this problem is exacerbated in 3D systems where heat flux from chips in the stack has to travel through a longer conductive path (i.e. larger thermal resistance) in order to be dissipated through the heat sink. Using a microchannel heat sink as an integrated part of silicon has been identified as a potential solution to cool power densities of up to $790\text{W}/\text{cm}^2$ with a maximum chip temperature rise of 71°C [4]. We investigate microchannel heat sink integration into each stratum of a 3D stack to enable cooling of $>100\text{W}/\text{cm}^2$ of each high power

density chip.

Figure 1 shows a proposed microfluidic network cooling scheme that can be used for cooling high-performance 3D chip stacks. Each silicon die of the 3D stack contains the following features: 1) an integrated microchannel heat sink [5], 2) through-silicon electrical (copper) vias (TSEV) and through-silicon fluidic vias (TSFV) [5], the latter used for fluidic routing in the 3D stack, and 3) solder bumps (electrical I/Os) and microscale polymer pipes (fluidic I/Os) on the side of the chip opposite to the microchannel heat sink [5]. The focus of this paper is on methodologies of integrating microchannel heat sinks and electrical TSVs in a 3D system.

The paper is organized as follows: Section II of this paper discusses the different topologies for integrating microchannels and TSVs. Section III discusses the batch level fabrication of microchannels and TSVs. Section IV discusses the potential trade-offs in microchannel cooling and signaling and power delivery in a 3D stack, and in Section V concluding remarks are presented.

II. TECHNOLOGIES FOR INTEGRATING MICROCHANNELS AND TSVs

A. Homogeneous Approach

In this approach, after Front End of the Line (FEOL) and Back End of the Line (BEOL) processing, microchannel heat sinks are etched on the back side of the wafers which are subsequently capped using a CMOS compatible bonding method such as a sacrificial polymer process [6] or Si-Si direct bonding process discussed in the paper. Once the microchannels are enclosed and sealed, TSVs are etched in the fins of the microchannels, and an appropriate sidewall isolation such as SiO_2 or Si_3N_4 is deposited. Finally, the TSVs are filled with a conductive material such as copper (with suitable barrier) or tungsten. This approach is conducive provided the processes following BEOL processing are CMOS compatible. This technique is thermally superior because of the high proximity of the microchannels to the active circuitry and absence of any thermal interface material in the conductive path between the microchannel heat sink and the heat source. Figure 2a demonstrates the concept of the homogeneous approach. A potential drawback of this technique arises from process integration issues, such as materials and temperature compatibility.

B. Heterogeneous Approach

In this approach, microchannels and TSVs are fabricated on a wafer that can be bonded in a number of ways to another wafer containing active circuitry and TSVs. In the first method (Figure 2b), the two wafers are mechanically and electrically bonded using an appropriate CMOS compatible technique [7,8]. This approach is relatively more flexible than the homogeneous approach. The processes involved in fabricating microchannels and high aspect ratio TSVs need not be compatible with CMOS. However the bonding process must be CMOS compatible to protect the underlying circuitry on the “capping” wafer. Precise alignment during bonding is

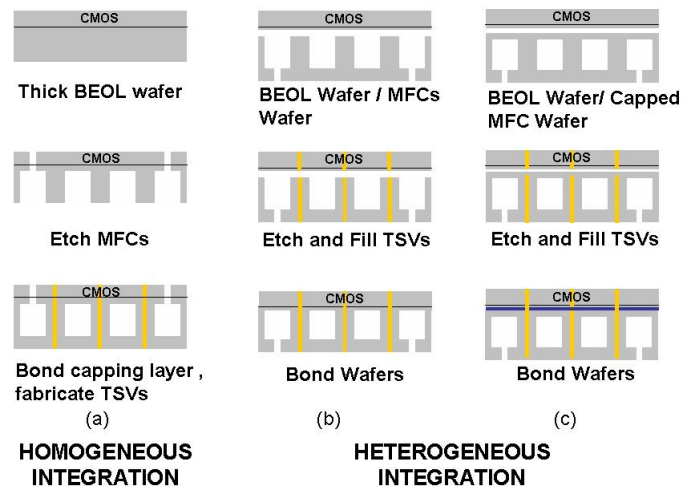


Fig. 2. Different schemes of integrating microchannels and TSVs.

required as both the bonding wafers have features on them. The electrical bonding of TSVs needs to be precise, as high density TSVs will be required to fulfill the power delivery and signaling requirements of a 3D stack.

In the second approach (Figure 2c), wafers are fabricated with microchannels and capped using bonding techniques compatible with TSV fabrication. Once capped, electrical TSVs are fabricated in the wafer which is then attached to a wafer with active circuitry using a hybrid bonding process demonstrated by [7,8]. The main advantage of this process is that these two wafers can be fabricated independently of each other (even in separate foundries), thereby eliminating the added complexity of making compatible microchannel heat sinks and TSVs in the same processing stage. However, the addition of the bonding interface and extra silicon thickness due to the already pre-capped microchannels may increase the total junction-to-ambient thermal resistance.

The heterogeneous approach of microchannel and TSV integration also enables the possibility of having a “Heterogeneous TSV” approach. To understand the need for this technology, let us consider the homogeneous integration scheme. For a given aspect ratio, the diameter of TSVs fabricated in the capped microchannel wafers would be large as compared to those fabricated if it were thinned CMOS wafers. These large diameter TSVs occupy valuable silicon real-estate which would have been used for CMOS circuitry. Since the channel wafers and CMOS wafers are fabricated independently in the heterogeneous scheme, the diameter as well as material for TSVs in both wafers can be different. The CMOS wafer can have smaller diameter TSVs fabricated using, say, tungsten and thereby have additional room for circuitry. Another advantage of this approach is reduced thermo-mechanical stress originating from CTE mismatch in the CMOS wafers due to smaller diameter TSVs [9]. Shown in Figure 3 is a graphical representation of this concept. The impact of this approach on electrical performance is currently being investigated via modeling.

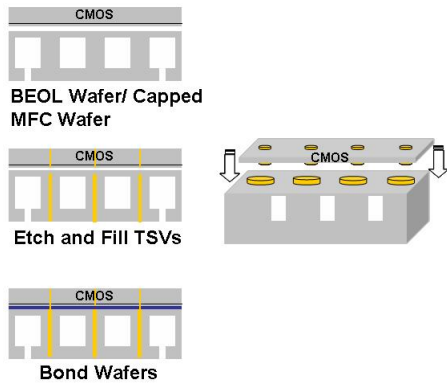


Fig. 3. Heterogeneous TSV technology.

III. EXPERIMENTAL DEMONSTRATION

We present a heterogeneous approach to integrate microchannels and TSVs in a wafer where microchannels and TSVs are fabricated independently and then bonded using the techniques discussed in the prior section (Figure 2c). The schematic in Figure 4 shows the fabrication process for integrating microfluidic cooling channels and electrical TSVs for a 3D IC stack. The process begins by depositing a $2\mu\text{m}$ thick layer of silicon dioxide on the front side of a $400\mu\text{m}$ thick wafer, which functions as an etch-stop layer when etching TSVs and TSEVs. We begin by etching fluidic TSVs and microfluidic channels using bosch process in an inductively coupled plasma (ICP) as shown in Figure 4b.

A. Wafer Bonding

There are several ways to bond a capping wafer to the microchannels. An adhesive bonding technique and a direct Si-Si bonding method were explored. Bonding using the adhesive method requires an intermediate layer such as SU-8. This technique enables bonding of silicon at low temperatures and is less dependent on substrate material, roughness and planarity of the bonding surfaces [10]. Bond quality evaluation and leakage tests have been performed in the literature [11], and the bond strength is sufficient for microfluidic applications. Results of the adhesive bonding are shown in Figure 5. The main advantage of bonding microchannels using the adhesive method is the inherent tolerance in terms of wafer thickness variation, particle contamination, etc. as compared to direct silicon bonding. The drawback of this process is that it necessitates the use of low temperature post bonding processes (e.g. sidewall isolation for TSVs) due to the presence of SU-8. Low temperature sidewall isolation techniques have been demonstrated using PECVD [12] and this maybe be promising for this application.

Low temperature plasma-activated Si-Si direct bonding approach was also implemented for capping microchannels. The surface preparation methods developed for low temperature processes are based on surface chemical activation resulting in different types of bonds at room temperature which amounts to lower annealing temperature and time [13]. The wafers are

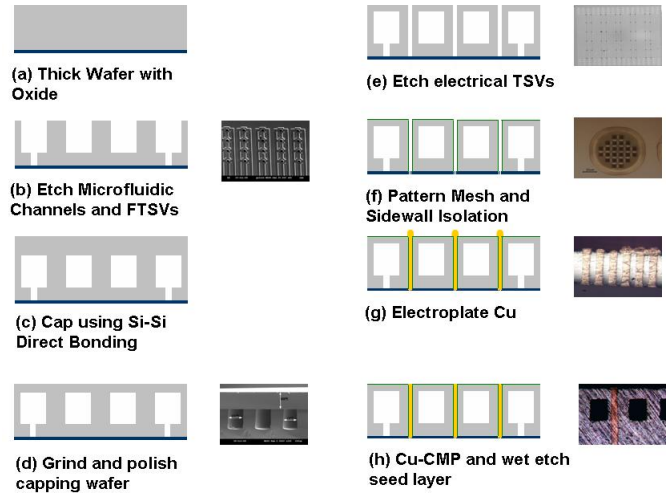


Fig. 4. Schematic of wafer-level integration of microchannels, through-silicon fluidic vias, and electrical through-silicon vias to enable 3D system integration using liquid cooling.

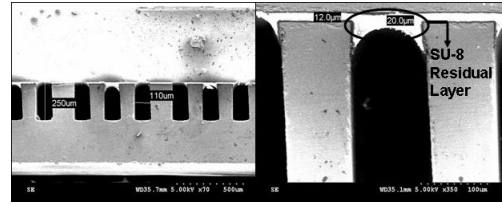


Fig. 5. Adhesive bonding using SU-8 layer.

bonded at room temperature. This is followed by a thermal annealing step at 400°C which provides the energy needed to transform the weak reversible bonds into strong permanent bonds. The bonded wafers were tested by destructive tests such as crack testing and dicing. When the wafers were diced, the bonded interface was observed in an SEM, as shown in Figure 6. The bonded and annealed samples were thinned down by back grinding and polishing the capping wafer to a thickness of $100\mu\text{m}$ to maintain the mechanical integrity of the microchannel heat sink. The need for thinning the capping layer arises from the fact that TSVs are to be integrated after the bonding process. Aspect ratio (AR) is a major limiting factor in TSV fabrication, as via etching and sidewall isolation techniques are AR dependent. Let us assume, for a given TSV diameter, we are aspect ratio limited to, say, 30:1 [14]. In order to maximize the cooling potential of microchannel heat sinks, the thickness of the wafer should be at least $200\mu\text{m}$ - $300\mu\text{m}$ [15] in addition to the thickness of the capping wafer. Without thinning and for a fixed TSV diameter, the total thickness would require fabrication of very high aspect ratio ($>30:1$) TSVs, and this puts a constraint on the maximum thickness of the capped microchannels. Shown in Figure 7 is a graph of TSV diameter versus wafer thickness for different aspect ratio values.

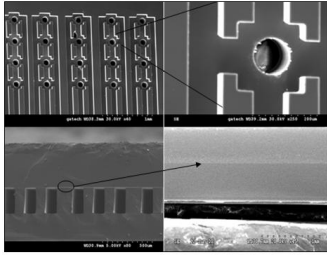


Fig. 6. Microchannel heat sink fabrication using low temperature plasma activated Si-Si bonding.

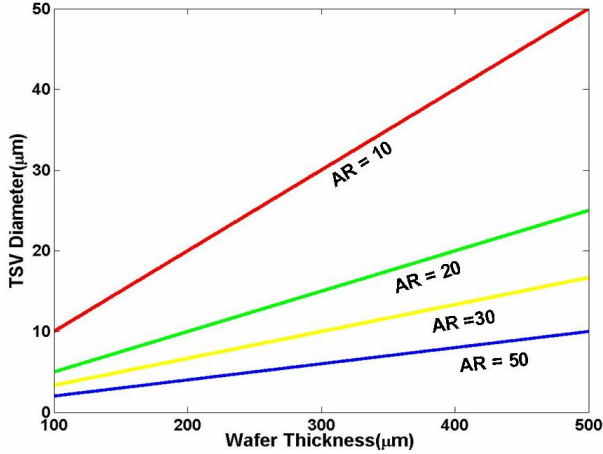


Fig. 7. TSV diameter as a function of wafer thickness and aspect ratio

B. TSV Fabrication

Once the wafers are bonded and thinned, TSVs are etched in the fins of the microchannels using the Bosch process until the vias reach the oxide (Figure 4e). TSV diameters ranging from $25\mu\text{m}$ - $80\mu\text{m}$ have been fabricated. However, for this first prototype, a diameter of $50\mu\text{m}$ was selected. A mesh is patterned on the silicon dioxide membrane, as shown in Figure 8a. The mesh pattern is aligned with the vias visible through the oxide, and the exposed oxide is etched using RIE (Figure 8b). After the mesh formation, a sidewall isolation of SiO_2 ($1\mu\text{m}$) is grown using thermal oxidation (Figure 4f). Low temperature processes such as PECVD oxide can also be used for sidewall insulation. Following via sidewall isolation, a seed layer of copper ($2000\text{ \AA}$) is deposited on top of this dielectric mesh followed by bottom-up electroplating process. There are two steps involved in the bottom-up electroplating process. In the first step, copper is electroplated on the mesh side until the mesh opening pinches-off. In the pinch-off process, copper tends to be plated at the corners of the mesh openings as shown in Figure 8c. This results in faster pinch-off time as compared to using the conventional electroplating processes on vias without mesh patterns [8]. The pinched-off mesh openings are shown in Figure 8d. Once the vias are pinched-off, the second step is through via electroplating to fill the vias using top side electroplating where the sealed copper mesh serves as the seed layer (Figure 4g). After plating

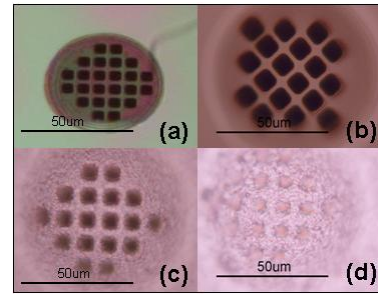


Fig. 8. Mesh fabrication for faster pinch off times (a) Mesh patterning (b) Etching of mesh (c) Seed layer deposition (d) Pinch off.

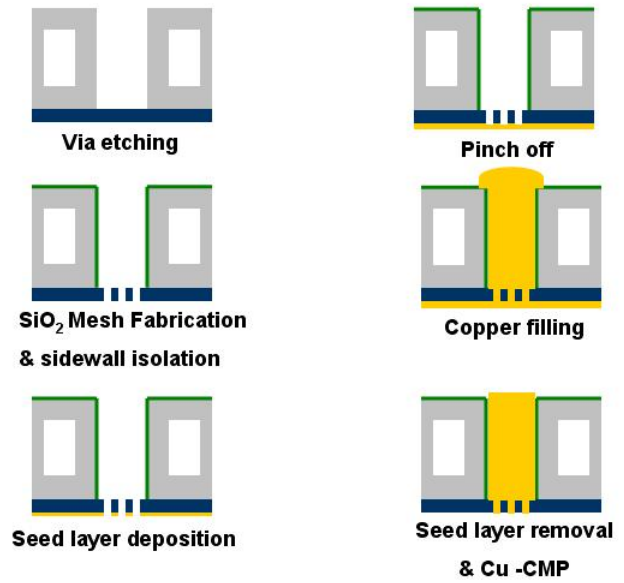


Fig. 9. Schematic of TSV fabrication in microchannels using mesh process

copper in the vias, the over-plated copper on the front side is removed by conventional chemical mechanical polishing (CMP) processing, while the copper seed layer on the back side of the wafer is removed by wet etching (Figure 4h). An expanded schematic demonstrating the process flow of TSV fabrication is as shown in Figure 9. Although it is not shown in the figure, the oxide mesh is etched after seed layer removal.

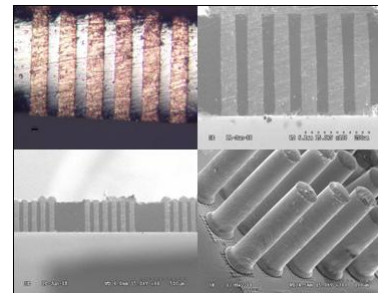


Fig. 10. Results of bottom-up electroplating of TSVs.

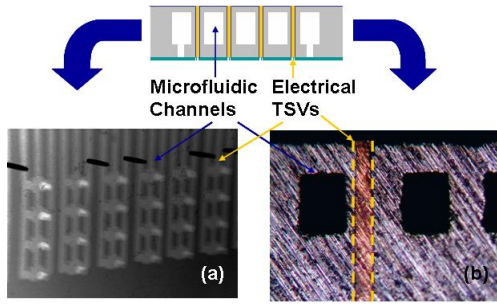


Fig. 11. (a) X-Ray Image of Microchannels and TSVs integrated on a single Chip. (b) Cross-sectional optical image of integrated microchannel heat sink and electrical through-silicon vias.

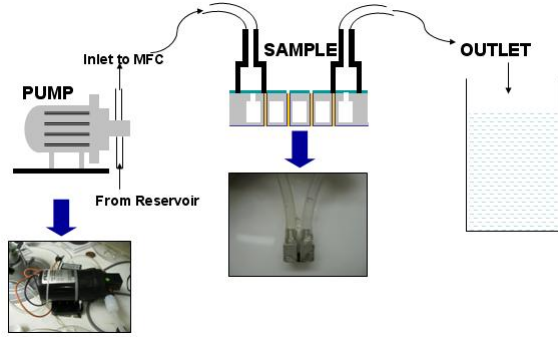


Fig. 12. Experimental setup for reliability and pressure drop measurements

C. Experimental Results

Shown in Figure 11 are X-ray and optical images of integrated microchannels and TSVs. The fabricated chip size is 10mm X 10mm and 51 microchannels are fabricated in a given chip. The depth of the microchannels is about 170 μm and width is 100 μm . Electrical through vias with a diameter of 50 μm and a height of 400 μm have been integrated with the microchannels. No voids or seams were observed when the TSVs were inspected in the SEM, X-Ray microscope and optical microscope. Fluidic reliability tests have also been performed on these samples with integrated microchannel heat sink and TSVs by passing DI water through the microchannels using the setup shown in Figure 12. Flow rates ranging from 20ml/min to 200ml/min have been tested with no mechanical failure.

IV. TRADE-OFFS IN ELECTRICAL AND FLUIDIC INTERCONNECTS

In this section we describe the modeling results of microchannel heat sink performance and TSV density. The set of equations and assumptions can be found in [1]. Figure 13 illustrates microchannel heat sink thermal resistance and pressure drop as a function of TSV diameter, number of TSV columns per wall, and microchannel thickness. As the number of TSV columns per wall increases, the thermal resistance and pressure drop increase. This occurs because as the number of TSV columns increases, the wall width increases, which leads to a smaller number of total microchannels (for fixed

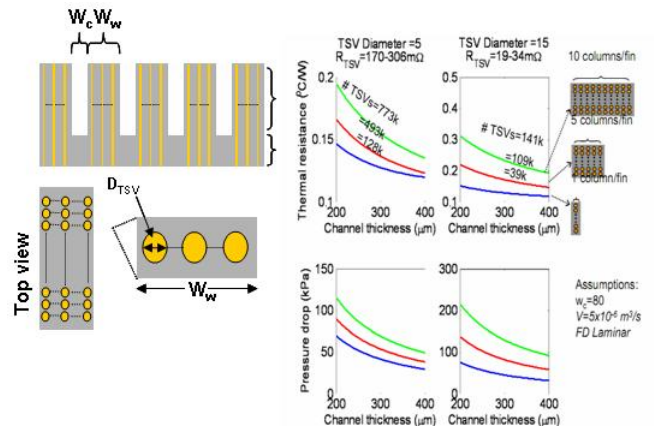


Fig. 13. Thermal Resistance and pressure drop in a microchannel heat sink as a function of TSV diameter, number of TSV columns per wall and channel thickness.

channel width and chip size). This has the consequence of decreasing the overall surface area in contact with the fluid which increases thermal resistance. As the diameter of the TSV increases, both thermal resistance and pressure drop increase for the same arguments presented above. Moreover, similar trends are observed as channel thickness decreases. In all cases, the value of junction-to-ambient thermal resistance is lower than current state of the art air-cooled heat sinks [16], and they meet the ITRS projections of approximately 0.2°C/W which will be needed to cool future high performance ICs.

The heterogeneous approach described above is also modeled using the same assumptions described. In this case, we assume a TSV diameter of 5 μm and the bonding interface between the CMOS chip and channel wafer is assumed to be SiO_2 . The modeling is based on the assumption that thermal conductivity of the bonding interface is a weighted average of the thermal conductivities of SiO_2 and Cu and that the TSVs are distributed evenly. The number of TSV columns per channel fin is varied from 5 to 20 along with the bonding interface thickness (1 μm to 10 μm) in order to quantify the effect of bonding. Figure 14 illustrates the result of this first order modeling.

V. CONCLUSION

Power delivery and heat removal are among key challenges for 3D integration of high performance logic and memory. 3D chip stacking combined with through-silicon vias and microchannel heat sinks can provide a high density of chip-to-chip interconnects for power delivery and signaling and can be an efficient cooling solution to meet the thermal management requirements of high performance IC stacks. In this work, we outline various configurations to integrate microchannel heat sinks and through silicon vias in a high performance 3D chip stack, fabrication issues, and preliminary experimental results.

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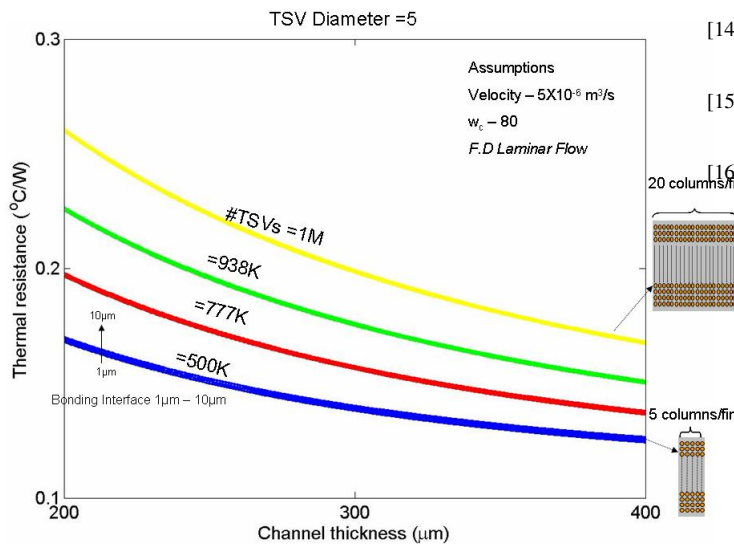


Fig. 14. Thermal resistance of microchannel heat sink as a function of number of TSV columns per channel wall, channel thickness and thickness of bonding interface.

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