

Dispensable 3D Electrical Interconnects -A near TSV back end packaging solution-

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Abstract

As packaging densities increase, lead by the requirements of smaller footprints, higher storage capacity, and multi-functional 3D die structures, traditional wire-bonding techniques become inadequate and thru silicon via (TSV) is not a cost-effective solution for packaging houses. This paper discusses the benefits of dispensing the electrical interconnects instead of using traditional wire bond or high cost TSV processes. Dispensing electrical interconnects allow form factors for stacked packages to reach near TSV dimensions. Offsets to expose die pads are typically <150 μ m and in some cases totally vertical structures can be achieved.

Material selection will vary according to pitch and electrical requirements. Methods for applying the different materials will be discussed as well as material selection criteria. The progression from large pitch applications of >300 μ m down to fine pitch applications of <100 μ m will be shown. Data will be presented stating the benefits for each material set and how the use of any of these dispensable electrically conductive fluids can be implemented into typical back end packaging houses using equipment that in most cases is already installed.

The non-contact nature of the dispensable electrical interconnect process allows for thinner die to be stacked without fear of cracking the stacked die. Furthermore, the entire die stacking process can be executed in a single step minimizing overall material handling and repetitive die stack processes that induce die crack and expensive yield losses.

Introduction

There are many different methods of creating 3D electrical interconnects whether it be on the die level or package level. Dispensable 3D electrical interconnects offer a single method that can be applied at both the die level and package level to create system in package (SiP) and system in silicon (SiS) solutions. (Fig 1) These solutions compete directly with wire bonding on cost, reliability and

throughput due to the batch nature of the process in which all assembly steps are executed once. This lowers overall cycle time and yields incremental cost savings as more die are added to the die stack. In comparison TSV is a process that requires a complex co-design of the assembly interconnects with device design before the wafers can be sent for assembly necessitating expensive cost models for commodities such as memory and other die stacks with low density interconnects (<100). Dispensable electrical interconnects allow form factors that are considerably smaller than wire bond which are almost completely vertical and reach near TSV dimensions in the XYZ plane. The machines, materials and processes explained herewith demonstrate the ease of adoption of this technology into back-end packaging houses with minimal disruption to current process flows.

Within the document any references to "reliability testing" include all the following tests: 1- Sample size of 77 units, 2- 1000 hours of high temperature storage (HTS), 3- 1000 temperature cycles (TC) from -55°C to 125°C, 4- 96 hours of biased hast (bHAST), 5- Dry bake at 125°C, 6- Moisture Soak 85°C/85% RH, 7- Peak reflow at 260°C. Any mention of passing reliability signifies that there were no failures recorded after these tests.

Vertical Interconnect Materials

Material selection for vertical interconnect pillars (VIP) is flexible and can be driven by cost of ownership (COO) and pitch requirements. Successful implementation has occurred with electrically conductive silver epoxy pastes, Copper-Tin-Bismuth (CuSnBi) pastes and silver nanoinks.

The silver epoxy VIPs in this study were formed using multi-component pastes from Lord Corporation. These pastes exhibited excellent shear strength and met all ROHS compliant requirements for semiconductor assembly. They were jetted with the Asymtek DispenseJet® and then cured in a batch oven at 150°C for 60 minutes. After assembly, the stacked die with silver (Ag) VIPs were compression molded using industry standard molding compound.

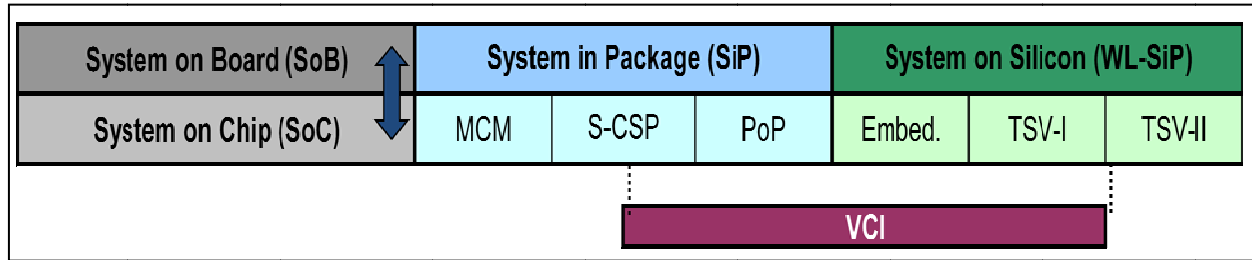


Fig 1: Vertical Circuits Vertical Interconnect Pillar (VIP) bridging back-end and front-end 3D applications.

The CuSnBi VIPs in this study were formed using multi-component pastes from Ormet Circuits Inc. The CuSnBi VIPs were jetted with the same Asymtek DispenseJet® and cured in a flowing nitrogen (N₂) batch oven ramped up to 205°C for 30 minutes. These parts were also then compression molded.

The nanoparticle inks in this study were Silver nanoinks. These inks were dispensed by aerosol technique with an Optomec Aerosol Jet® System.

Within the epoxy-silver system, the cure served to crosslink the epoxy to form a thermally stable VIP. The cross-linking reaction itself compresses the pillar interconnecting the silver flakes. In addition, the epoxy acted as an adhesion promoter between the die and substrate pad surfaces and the silver VIP. Resistivity of the VIP itself was of the order of 0.9×10^{-4} ohm-cm. Material passed reliability testing. When driven to end of life, the wear-out mechanism was due to fatigue and delamination of the epoxy-silver from the underlying die pad or substrate. IN an analogous manner, scaling down of this type of material to achieve fine pitch dispense was set by two factors: 1) the Ag/epoxy shrinkage and 2) the interfacial area between VIP and pad. The Ag/epoxy composition had to insure enough Ag to form overlapping and contacting metal particles with enough epoxy to bind the Ag together and to the underlying pad. With decreasing interfacial area, an optimization of metal contact area and adhesion area was necessary while fulfilling thermal cycling requirements. Based passing reliability data, 280 μ m pitch between electrical interconnect lines and higher with a VIP/die pad opening of 190x85 μ m (8550 μ m²) were required to qualify a product.

The CuSnBi VIPs cure by means of a transient liquid phase sintering process which enables low temperature sintering. After sintering, these VIPs are thermally stable up to 268°. Through the reaction of Sn with Cu, the sintering process forms a strong Cu₅Sn₆ Intermetallic joint between Cu particles. In addition, the presence of Sn in the vicinity of the die

or substrate pad formed an Intermetallic bond of the VIP to the pad. (Fig 2). Qualification of the material for 200 μ m pitch between electrical interconnect lines and higher revealed that this material passes reliability tests with pad openings of 55x55 μ m (3025 μ m²). Smaller pad openings have not been evaluated with this material.

Cu systems are sensitive to the presence of oxygen (O₂). Oxygen will form a Cu oxide barrier to the formation of the Cu₅Sn₆ inter-metallic material. In addition, CuO₂ forms a resistive layer, increasing the resistivity of the VIP. Using proprietary processes, the CuSnBi VIP can be sintered with resistivity of 0.5×10^{-4} ohm-cm.

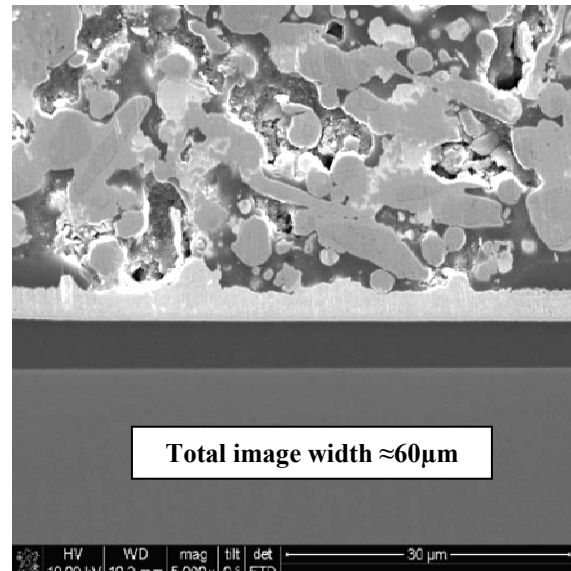


Fig 2: Intermetallic bond to die die pad

Scalability requirements to obtain thinner line widths for the dispensed metallization are driven by the scalability of individual components. Hence, nanometer dimensions will require nanoscale particles. Nanoparticles require innovative techniques to form stable dispersions without agglomerations. Agglomerations will adversely affect the uniformity and control of interconnect lines. This stability will

Table 1: Characterized VIP material selection

	Materials		
	Silver Paste	Cu SnBi Paste	Silver Nanoink
Readiness	Ready	Ready (In Technology Transfer)	Development
Viscosity (CPS)	30,000	500,000	<1000 (low)
Resistivities (Ohm-cm)	0.9×10^{-4}	0.5×10^{-4}	5×10^{-8}
Shear Strength (psi)	7000 (Al to Al)	1300 (Cu to Cu)	TBD
CTE (ppm/°C)	60 (alpha 1)	22	
Tg (°C)	82	none	none
Pitch Capability	$\geq 280 \mu\text{m}$	$\geq 150 \mu\text{m}$	$\leq 150 \mu\text{m}$
Dispense Head	DispenseJet®	DispenseJet®	Aerosol Jet®
VCI Application	FLASH, DRAM	FLASH, DRAM	Mixed Die ASIC+DRAM
Other Applications	Metal Traces, Die Attach Adhesives	Pb-Free Solder, Die Attach Conductive Paste, Z Axis Interconnect, Metal Traces	Solar Cell Metallization

need to be sustained during the dispensing process. Once dispensed, the nanoparticles will have lower temperature sintering characteristics as the high surface area will drive the sintering reactions. Two approaches exist for the creation and dispensing of the nanoparticles. The nanoparticles can be created and dispensed in the same process such as in laser ablation of microparticle aerosols.

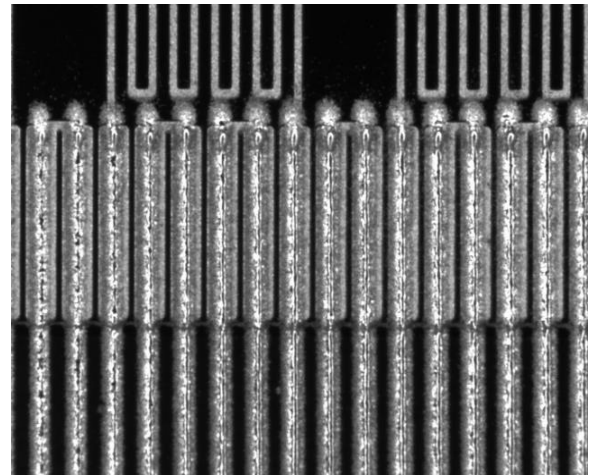
The second approach is aerosol jetting of Ag Nanoinks enabled by the patented formation Ag nanoparticles. These particles were dispensable to fine lines due to the aerosol capability with hindered agglomeration. Sintering occurred in two successive mechanisms. First, the protective coating was removed. Then the high surface area of the nanoparticles will drive the bonding of the nanoparticles and the reduction of microvoids. Early studies show passing results for bHAST, T/C and HTS –as mentioned in the introduction-.

Vertical Interconnect Machines

Minimum dispense machine requirements include the capability to find fiducials at a high magnification, volume production output (>100 UPH), and low mean time between failure / mean time between assist (MTBA/MTBF) rates. Typical MTBA is 4hours and 8hours MTBF. Platform selection is directly related to Vertical Interconnect (VIP) pitch requirements. The pitch between dispensed lines is also key to determining which material and application is optimal to construct the electrical interconnects. Systems dispensing electrical interconnects at pitches above $200 \mu\text{m}$ require a positional accuracy of $\pm 50 \mu\text{m}$ at 3-sigma to operate with 99% efficiency; for these applications an Asymtek Axiom is used. Systems operating at pitches $< 100 \mu\text{m}$ require accuracy ranges of $\pm 5 \mu\text{m}$ due to the dramatically reduced die pad size available for the electrical connection, characteristically

$16 \times 110 \mu\text{m}$ ($1760 \mu\text{m}^2$). For these applications an Optomec M³D system is utilized.

Each material requires a specific application method that enables the formation of the electrical interconnects. Two methods have been validated to apply the materials described in this paper: aerosol jetting and hybrid-jetting.

**Fig 3: Aerosol Jet® lines at 61µm pitch**

For aerosol jetting we employed an Aerosol Jet® valve to apply a low viscosity fluid to create very fine lines (fig 3). Typical ink viscosities range from 0.7-2500 cps. The material is atomized in a vial away from the dispense head. An inert carrier gas transports the dense aerosol of material to the deposition head at low pressure usually through a 1/8" thin tube. At the deposition head the dense aerosol air flow is encased by a separate inert gas laminar air flow that controls the line width for the deposited material. This method enables fine line printing from 10-150µm line width. One major advantage of aerosol jetting is that typical standoffs for parts range from 1-5mm. A standoff is the

distance in the Z-axis from the tip of the needle to the target substrate to dispense on.

The most common failures for this application method include shorting of lines caused by a disruption of the atomized spray beam arising from visible droplet formation in the supply hose, and random dispersion of silver particles onto the substrate caused by the shutter on the dispense head. Clogging of the needle tip by build-up of ink particles on the shutter while the valve is not in use can also create deposition issues. Solutions for these issues have been identified for high volume production (HVM) systems

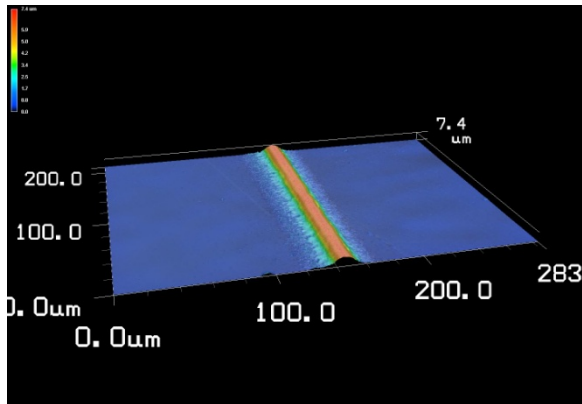


Fig 4: 3D laser profile of Aerosol Jetted line.

For hybrid-jetting we utilized a DispenseJet® valve. This method capitalizes on the micro-dot mass dispense capabilities of the JET valve that are necessary to obtain fine line dispense widths down to 100µm using medium to high viscosity materials. Proven viscosity ranges for the JET in this application are from 30,000 – 600,000cps. The second factor of hybrid jetting, analogous to traditional valve dispensing techniques, the needle to surface standoff requirement of an extrusion dispense valve is utilized to assist in material break-off, taking advantage of the surface tension of the substrate. Typical dispense heights range from 80-120µm using this method.

The hybrid-jetting process is currently under HVM transfer and presents an electrical end of line failure rate of 950ppm (0.099%) (Fig 5). Failures include line shorts, line opens and other non-VIP related failures.

Vertical Interconnect Process

The construction of the die stack follows a dice after grind (DAG) process flow. Due to the non-contact nature of the VIP very thin die can be stacked

and interconnected. The die thickness is limited by background planarity, wafer saw and stretch process control and stacking equipment capability. Typical die thickness used is between 50-60µm including die attach film (DAF). Die as thin as 30µm (20µm die + 10µm DAF) have been used for customer specific applications. All proprietary Vertical Circuits process steps are applied as a single block within this standard process flow making implementation into a production floor seamless and minimally disruptive. It is important to note due to the batch nature of this process, process steps are only executed once and do not need to be repeated for each layer, which results in less processing steps, smaller workforce, and reduced manufacturing floor space requirements, while enhancing overall throughput and yield. (Fig 6)

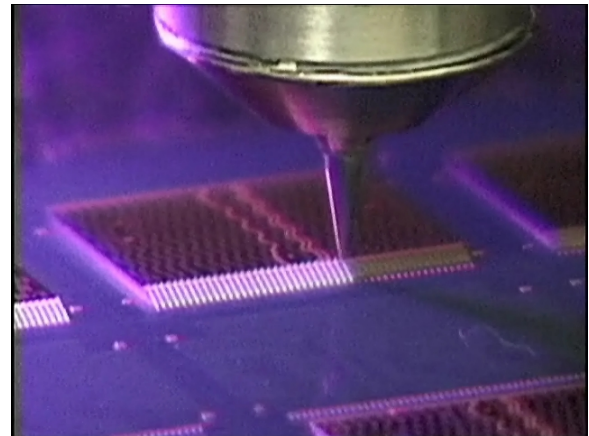


Fig 5: Hybrid-Jet application of VIP

To achieve near TSV dimensions die stack offsets must be minimized. Die stacks with offsets between die as small as 110µm have been qualified through reliability testing; 130µm being the typical die offset. Offset stacking allows the elimination of interposer layers and reduces overall Z height for the die stack while eliminating intermediate stacking steps. All stacks on a strip are built in a single pass utilizing 100% known good die (KGD). While single direction offset stacks have been qualified, stagger stack structures without interposer layers possessing single die offsets of 150µm are undergoing qualification

Before the formation of the VIP a dielectric coating is applied to prevent shorting of the conductive materials when in contact with the die in the stack. Selective laser ablation of the dielectric coating is required to create openings over the die pads that will be connected to VIP conductors.

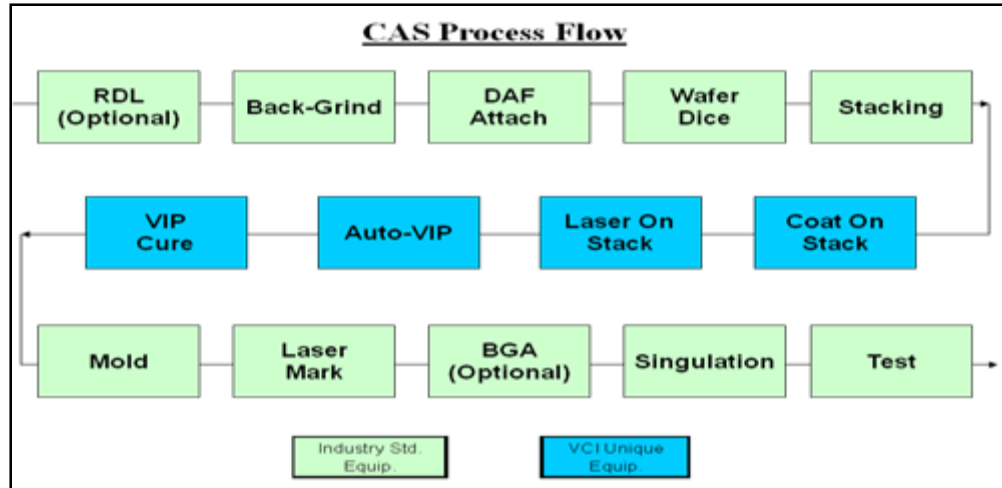


Fig 6: Coat after stack (CAS) process flow for die level dispensable electrical interconnects

The dielectric coating is applied to the completed die stack on a strip level by room temperature chemical vapor deposition (CVD). This results in a transparent coating with a target thickness of 2.5 μm ; standard 3-sigma variation is of 0.25 μm .

Laser ablation is performed using an excimer laser to remove the dielectric coating on selected pads. The laser is capable of ablating multiple rows of pads in a single exposure, only needing to re-focus for the next group of layers, making this process HVM friendly due to the batched execution of rows. Laser ablation is also used for encoding individual die in the stack for unique accessibility through the controller. Laser openings as small as $16 \times 110 \mu\text{m}$ ($1760 \mu\text{m}^2$) have been achieved with a CpK of 1.53 at >110 UPH.

minimize shorting between interconnects or pad skips which result in electrical opens on ablated pads. Line dimensions are controlled by dot weight and dispense gap. Typical dot weights are 4µg/dot with a process window of ±0.5µg/dot. The capability to maintain stable dot weights is critical to run uninterrupted production. Dot weight control simulating 8 hours of production produce a CpK of 4.06 (Fig 7). Normal dispense heights range between 80-120µm. Current UPH is >110 for units requiring 50 interconnects in a high mix low volume processing environment. It has been estimated that this same process can obtain >150UPH in a low mix high volume environment because of better characterization and control of incoming product.

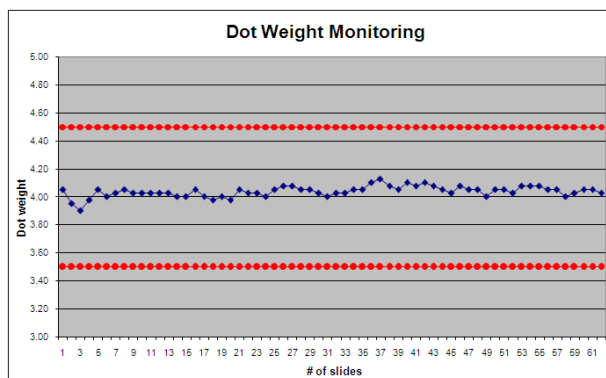


Fig 7: Dot weight monitoring graph

The VIP process deposits the electrically conductive materials over the die stack in parallel lines. Those locations where the excimer laser ablated the pads will make an electrical connection . Otherwise there will be an electrical open for that pad. Tight control of line dimensions are required to

Vertical Interconnect Development

Current development of 3D dispensable electrical interconnects is focused on mixed die (ASIC+Memory) stacks. The need to reduce footprint in XYZ while minimizing signal propagation time from memory to processor is a necessity as the mobile electronics industry continues incrementing functionality and reducing size. Third party electrical models show that dispensed conductors exhibit better electrical performance at higher frequencies when compared to wirebonds while having a considerable cost advantage over both wirebonds and TSV.

Our work on mixed die stacks has yielded encouraging first pass data through reliability and electrical test, demonstrating the capability of this technology for mixed die applications. Dispensed nano particle inks with line widths of 30um are being currently produced with height profiles between 12-15um. Electrical contact resistance is negligible and resistivity of 2x bulk silver has been achieved

following proprietary curing procedures (Fig 8). Reliability data displays capability of passing HTS, TC and bHAST. Complete reliability testing qualification is targeted to be completed by end of year.

Conclusion

By utilizing available back-end equipment it is possible to obtain near TSV die stack dimensions without incurring CAPEX costs typically required for TSV stacks. The materials used have passed reliability testing qualification criteria proving HVM readiness. The dispense methods have very low failure rates (0.099%) with a high CpK of 4.06 demonstrating HVM robustness. The ganged application approach for creating these die stacks result in faster product cycle times as well as manufacturing floorspace reduction for assembly houses. Further development of this process is enabling smaller offsets by staggering the die in alternating directions and eliminating the interposer layer from the stacks thus reducing the overall XYZ footprint. The economics of scale demonstrate that the higher the die stack the more cost effective this method becomes due to the elimination of repetitive stacking and wirebonding steps (figure 9).

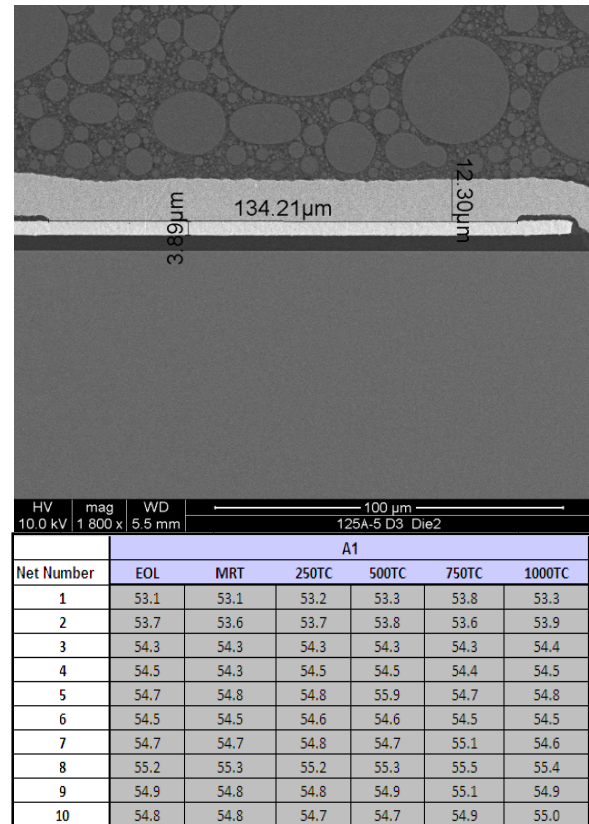


Fig 8: Cross section nanoink on die pad and TC data

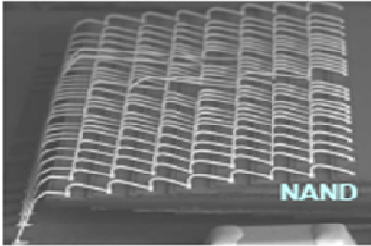
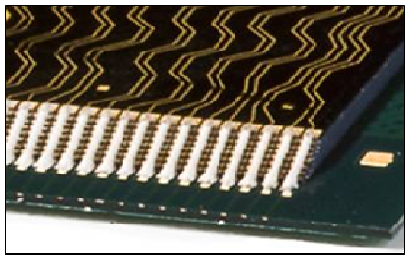
8-Die 1mm Wire-Bonded NAND		8-Die 1mm Conformal Interconnect
	Higher Yield Smaller Size Lower Cost	
• Sequential Process. • Gold Interconnect • Full contact process • 22 Process Steps, 1000 sq.ft Floor. • 40 Hour Cycle Time/Strip. • 16 Operator Workforce. • Die Thickness Required = 35µm		• Parallel Process. • Silver Interconnect • Non-contact process • 8 Process Steps, 250 sq.ft Floor. • 8 Hour Cycle Time/Strip. • 8 Operator Workforce. • Die Thickness Required = 50µm.

Fig 9: Side by side comparison of traditional 8-HI die using film on wire wirebond and VIP

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