

A Cost-Effective PVD Thin Film Deposition System for the 3-D TSV Barrier/Seed Application

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Abstract

As technology complexity continues to grow in advanced IC electronics packaging, more cost effective use of capital equipment becomes mandatory. The process and cost performance of a PVD system for 3-D TSV barrier/seed metallization solution is reported. A single chamber-multi-wafer bridge tool for multiple TSV generations is configured. The TSV hardware configuration with i-PVD for batch processing improves productivity and methods to prevent via necking and at mean time enable high step coverage on aspect ratio of 10:1 vias with CD down to 5 μm . Cross-section SEM analysis on the vias with various CDs and aspect ratios shows good step coverage as deposited. Conformal post-electro-plating results confirm the continuous seed coverage.

Introduction

The emerging 3D advanced packaging market is at a critical stage where R&D, design and integration needs to converge into an applicable solution. Through Silicon Via (TSV) is essential in making the 3D scheme feasible. TSV has been extensively employed in MEMS, and is now currently implemented in image sensors, memories, and ASICs.[1-3] Many challenges remain to make it fully scalable for integrated device manufacturers (IDMs), designers and foundries. Among all the challenges, cost of manufacturing is most severe. Capital equipment cost and wafer throughput are the two key contributors to the overall manufacturing cost. We present here a relative cost/benefit analysis of different TSV integration scheme and offer a cost-effective metallization solution for an integrated TSV solution involving barrier/seed deposition.

Many approaches for barrier and seed have been investigated. Table 1 compares the advantages and disadvantages of various approaches. The key advantage for PVD barrier/seed is its capability of achieving void-free plating, which is strongly dependent of the Cu seed thickness and continuity for sufficient plating current. A robust PVD barrier/seed also provides sufficient adhesion during subsequent process to avoid any reliability issue.

Among all, PVD approach has been well understood and characterized in terms of film quality, resistivity, contact resistance, and most importantly reliability in the back-end interconnect down to 32 nm feature sizes.[4] Although wet process enjoys superior step coverage compare to PVD, its lack of process control and its poor reliability make it unlikely a candidate for

production. Nevertheless, the challenge for PVD in TSV application remains. Due to the nature of high vacuum process, the PVD equipment is costly. The TSV size is now in the range of tens of microns, which requires increasing film thickness. The much larger via CD and via depth, makes the PVD throughput less desirable. Yet, the standard PVD sputtering is not sufficient to meet the step coverage requirement for TSV structures and the state-of-art PVD system is too costly to implement.

TSV Liner/Seed	Advantage	Disadvantage	Stages of Development
CVD	Conformal deposition, excellent step coverage, very high aspect ratio fill capable	High contamination risk, poor adhesion, poor reliability, high temperature, high cost	R&D
Wet	Conformal deposition, good step coverage possible, low temperature	High contamination risk, poor adhesion, poor reliability, poor process control, low process margin, production unproven	R&D
PVD liner + Wet seed	Conformal deposition for seed, good step coverage, low temperature	Liner/seed interface difficult to control, poor reliability	R&D
PVD	Excellent adhesion and interface control, good reliability, and production proven	Poor step coverage, higher cost, lower throughput	Production

Table 1 Comparison of different liner/seed deposition methods.

Cost Analysis

The cost of PVD Barrier/seed process for TSV application stems from two basic considerations. The system/hardware cost and performance cost. The system cost is comprised of depreciation cost of the equipment, the cost of consumables, and cost of utilities. The performance cost can be attributed to the required step coverage of the deposited films on designated TSV structures and wafer output per unit time (throughput). The complexity of calculating the performance cost lies in correlation between the required minimum step coverage and aspect ratio of the TSV.

In determining the total cost of PVD, several dependent variables beyond PVD needs to be explored. A perfectly smooth via is most desirable for PVD barrier/seed coverage and total required thickness of the PVD layers could be minimized. In reality, the balance between DRIE via roughness and DRIE throughput has been one of the most difficult challenges the industry has been facing. Typical isolation layer, such as PECVD oxide can only be deposited conformally and can hardly change the roughness profile. Scalloping, striation, and cornering are most frequent etch roughness types. In general, scalloping can be overcome by re-sputtering, vertical striation requires much more PVD coverage due to enlarged surface area; and most challenging profile is via bottom cornering, where there is a undercut at the corner of the bottom; thus a significant re-sputtering from the bottom of the via is imperative.

Figure 1 illustrates the three types of roughness encountered in the etch profile. Although some of the process data are drawn from very rough vias, a typical roughness of 150nm is required for all the process data presented in this study to ensure process repeatability.

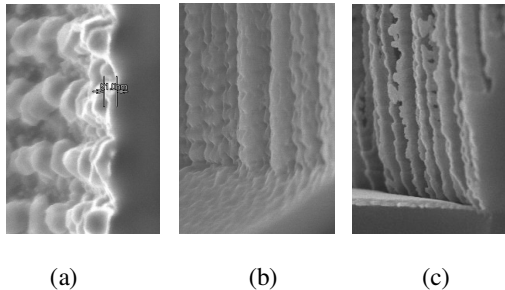


Figure 1 Typical etch profile roughness, (a) scalloping, (b) vertical striation, (c) cornering.

Another cost/performance consideration is the minimum thickness for plating.[5] The PVD deposition profile is inherently non-uniform inside the via. A very thick PVD coverage is not practical. In order to fully plate the via without seam, a bottom-up plating is preferred. Figure 2 shows a typical profile of PVD deposited barrier/seed. Since most of the TSV vias is 50um and above, and the diffusion length of additives is in the micron range, the required time for the additive to reach the bottom of the via is exceedingly long, making the plating the longest process steps in TSV formation. At present, to our knowledge, no detail study has yet been published on the minimum seed layer. A 50 nm thickness is currently assumed.

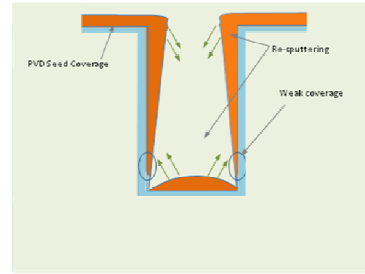


Figure 2 A typical PVD step coverage profile. Re-sputtering is used to improve step coverage

Performance Measures

Axcela has been designed to take advantage of multiple processing challenges in one platform. The flexibility in configuration and process control can help address various challenges in TSV barrier/seed deposition. Total of 9 different targets with one tool and 3 different chambers can be dedicated for various modules, with each chamber containing (4) 300mm wafers, or (6) 200mm wafers, and (10) 150 mm wafers. This configuration will invariably reduce cost in the overall of TSV implementation, compared with single-wafer system.

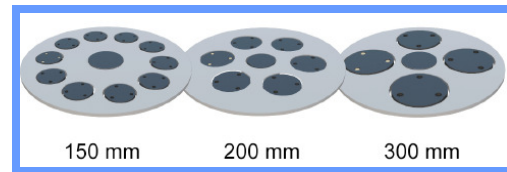


Figure 3 Batch wafer layout during deposition.

To deposit material into a vertical via is challenging using conventional PVD process and thus requires an ionized plasma source and long throw to enhance directionality of the plasma. This allows the ionized metals with sufficient biasing to be deposited into these long vias resulting in higher step coverage. The ionized metals can be steered using additional magnets for better side wall coverage. Since the distance from target to substrate has increased, the neutrals, which cannot be controlled by EM field and less directional, will be collected at the shield walls rather than the substrate, decreasing the collection efficiency, hence, the deposition rate. In summary, the long throw process with side confining electromagnetic field and wafer bias would acts as collimation through the confinement of the plasma and enhancement of directionality of the ionized metals. (see Figure 4)

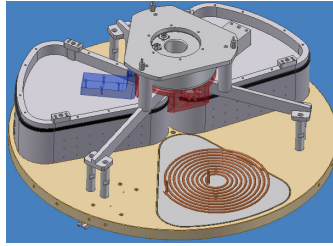


Figure 4 Axcela TSV chamber configurations

The PVD step coverage is critical both in plating performance as well as in cost of ownership in TSV application. Axcela's IPVD source in conjunction with high power DC source allows tuning our TSV process for various aspect ratio structures. Various TSV step coverage are shown in Figure 5-7.

In Summary The iPVD solution has been characterized for various TSV structures based on the TSV roadmap. [6] Successful plating has been shown on various TSV structures from 30um to 100um openings and 100um to 500um depths.

Conclusions

TSV implementation relies on synergies from multiples tool sets and design layouts. As cost remains a challenge, one of the areas where cost can be managed is using a bridge tool which is easily configurable and flexible while offering a competitive solution. Therefore Axcela offers cost effective metallization solution for integrating TSV application.

Acknowledgement

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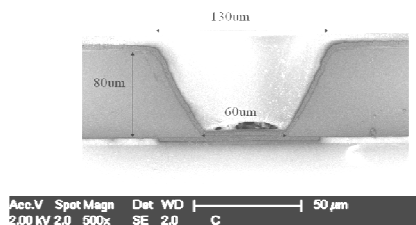


Figure 5 Profile with barrier/seed coverage on 130um x 80um.

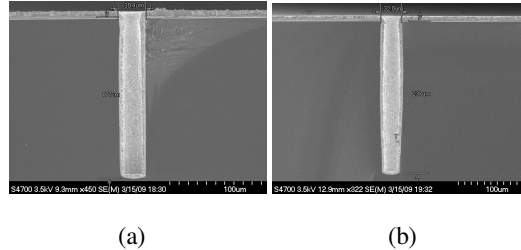


Fig. 6 Conformal plating on 30um x 180um (6:1) and 30 um x 240 um (8:1)

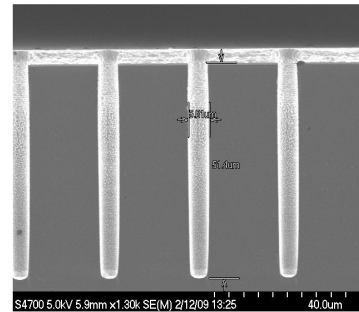


Fig. 7 Profile with barrier/seed coverage on 5um x 50um

References

- [1] T.Mitsuhashi, et.al, Development of 3-D packaging process technology for stacked memory chips, Mater. Res. Soc. Symp. Proc. Vol. 970. 2007.
- [2] P.Morrow, et. Al, Design and Fabrication of 3-D Microprocessors, Mater. Res. Soc. Symp. Proc. Vol. 970. 2007.
- [3] P. Singer, Through-Silicon Vias: Ready for Volume Manufacturing? Semiconductor International, Mar. 1, 2008
- [4] Armin Klumpp and Peter Ramm, "3D-IC Fabrication Challenges for More Than Moore Applications", Manufacturing and Reliability Challenges for 3D ICs using TSVs, San Diego 2008.
- [5] B. Kim, Through-Silicon-Via Copper Deposition for Vertical Chip Integration, Mater. Res. Soc. Symp. Proc. Vol. 970, 2007
- [6] Sitaram Arkalgud Phd., "A New Era: 3D TSV interconnect", Sematech Symposium Japan 2007.