

Reliability Impact of Defects in Lead-Free BGA Solder Joints – A Systematic Study

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Abstract

In high volume manufacturing environments, design rules and process variables must be tightly controlled to prevent latent defects in solder joints. These types of defects can arise due to deviations in PCB quality, assembly process, and handling. Poorly formed solder joints can escape in electrical tests and in-line non-destructive testing, only to cause early field reliability problems.

In this study, a systematic DOE approach has been adopted to study the long term reliability impact of lead free solder joint defects. A novel test vehicle was developed wherein daisy chain lead-free 0.8 mm pitch 60-ball BGA components were assembled on single and double-sided MiniDIMM cards. In addition to a normal production process, a variety of latent solder joint defects were intentionally introduced under controlled conditions. The types of defects introduced may stem from PCB design, PCB fabrication, solder paste printing, component placement, reflow, cleaning, and handling operations. Several defects were manufactured at two levels of severity. The cards were subjected to board level thermal cycling test from 0 to 100 °C, and the daisy chain resistances were continuously monitored during the test. The results showed that several types of latent defects had a very detrimental impact on long term reliability, while some of the other defects did not have a measurable impact on fatigue reliability.

Keywords: Lead-Free, BGA, Solder-Joint, Defect, Reliability

Introduction

In the past several years, the electronics manufacturing industry has been involved in a massive transformational effort to replace Lead (Pb) based soldering alloys with lead-free soldering alloys. While various segments of the industry, such as consumer electronics, are in advanced stages or have already completed this transition, several segments are yet to make this transition. Specifically, high end networking and server class products have a limited time exemption from the European Union's Reduction of Hazardous Substances (ROHS) directive because of the highly diversified supply chain, complex product design and manufacturing environment, stringent system level availability and long term reliability requirements. A major challenge with migration towards lead-free solder is that compared to eutectic tin-lead solder, the factors influencing the long term fatigue reliability of lead-free solder joints and accelerated qualification testing

requirements are not well understood. In addition, the higher reflow temperature, multitude of lead free solder alloy compositions, and reduced solder wetting characteristics makes the assembly and process control much more prone to defects which can impact product yield and long term reliability [1]. The IPC-A-610 is a widely used industry standard that defines the acceptability of various types of soldering defects [2]. In spite of stringent controls in process parameters, excursions in incoming quality or processing parameters can occur in highly complex Pb-free assemblies. While some defects can be readily detected in electrical board or system level testing, others may escape in electrical testing and in-line non-destructive inspections. These types of latent defects are particularly insidious because they represent a serious field reliability risk for the product.

The root cause for BGA solder joint defects may be traced to various stages of design, material procurement, assembly, and handling. For example,

the incoming components could have poor solder wetting due to black pad, oxidized or contaminated pads. High component warpage can cause malformed joints like head-in-pillow (HiP) defects. The incoming printed circuit boards (PCBs) could also have high warpage, contaminated or oxidized pads. A host of defects can also be introduced in the assembly process. For example, insufficient solder paste thickness, insufficient flux, use of oxidized solder paste, or an inappropriate reflow profile can cause partially wetted solder joints. Mis-registered solder paste, misplaced components, or mishandled PCBs prior to reflow can also result in malformed joints. Finally, during PCB or assembly level electrical testing and shipping, latent solder joint defects can be introduced due to excessive mechanical strain. For example, brittle solder joint fractures with Electroless Nickel Immersion Gold (ENIG) finish, and pad cratering in PCB pads have been well documented [3, 4].

While every effort must be made to prevent latent defects, their reliability implications have not been systematically studied. Many existing studies on effects of processing parameters are based on eutectic Sn-Pb solder [5]. A few studies on lead-free BGA soldering defects have focused efforts on evaluating the effect of a specific type of process variable [6-8]. In this study, a test vehicle was developed and a design of experiments (DOE) approach was adopted to study a variety of latent solder joint defects. Under tightly controlled conditions, these defects were intentionally introduced at the corner pads of a lead-free BGA test vehicle to assess their reliability implications in a thermal cycling environment.

Test Vehicle and Assembly

A 60-ball 0.8 mm pitch daisy chain plastic BGA package with lead-free Sn-3.5%Ag-0.5%Cu (SAC305) solder spheres was used in this study. The package size was 11.5 x 8 mm (figure 1). The solder ball diameter before reflow was 0.42 mm, the pads were non solder mask defined (NSMD) with 0.33 mm diameter and electrolytic Ni/Au finish. The organic substrate material was Bismaleimide Triazine (BT). The PCB was designed to conform to JEDEC's standard outline MO-244 for a 244-pin plug-in MiniDIMM module [9].

The PCB material was high T_g FR4. The PCB consisted of 16 layers and the total thickness was 125 mils. The surface finish for the PCB pads was high-temperature OSP material compatible with

lead-free assembly. The cards were either single sided or double sided. Each single sided card had five daisy chain BGA locations on each side. The double sided cards had 2 components per side in a back to back (clam shell) configuration. In the nominal defect-free condition, PCB assembly was done with Sn-3.8%Ag-0.7%Cu (SAC387) type 3, no-clean paste. The paste printing utilized a 4 mil thick, 0.38 x 0.38 mm (15 x 15 mil), square aperture stencil. Surface mount assembly was accomplished in an air environment with peak temperature between 236 °C to 238 °C, and time above liquidus (TAL) between 51 to 66 seconds.

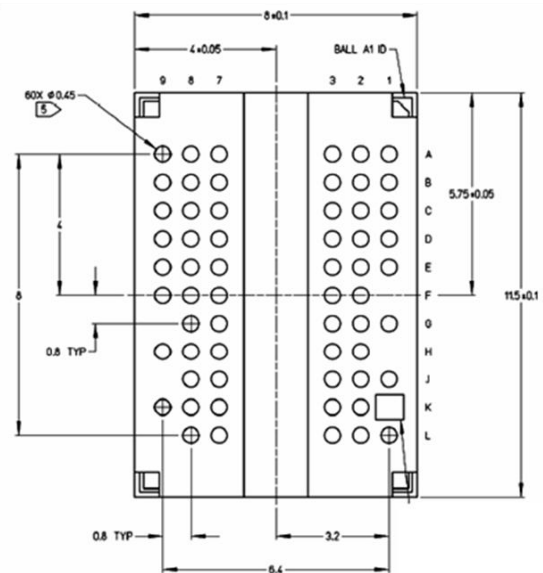


Figure 1 - Daisy Chain BGA layout

While some process-related solder joint defects may randomly occur at any location on a PCB and at any location within the component array, most of the defects such as those stemming from pad contamination, warpage, mechanical handling, or cleanliness, will be preferentially located near the BGA corners. Unfortunately this is also the location most likely to fail during board level reliability testing. For this reason, the pad specific defects intentionally created in this study were located at the 3 corner-most pads at all four corners of the BGA. Other defects that were not pad specific were applied on the whole card. Furthermore, the design of experiments (DOE) matrix was controlled so that no two defects would occur in the same component, i.e., only one defect was created at a time. This allowed the reliability impact of each defect to be quantified individually.

Table 1 lists the defects evaluated in this study. A total of 12 types of defects have been assigned alphabetical codes. The defect free (control) samples were assigned defect code "X". For most of the defects, two levels of severity were engineered. All the defects in Table 1 have been categorized based on the possible source, and the method for creating each defect has been listed.

Table 1 - Matrix of Defects Introduced in Test Vehicle

Defect Category	Defect Code	Level	Method
PCB Pad Contamination	C	1	50% solder mask coverage on corner pads
		2	70% solder mask coverage on corner pads
	D	1	50% silk screen coverage on corner pads
		2	70% silk screen coverage on corner pads
Oxidized PCB Pads	E	1	OSP finish stripped from corner pads and pads exposed to 2 days air environment
		2	OSP finish stripped from corner pads and pads exposed to 2 reflow cycles
Partial OSP Coverage on Pads	F	1	OSP finish stripped from 70-90% area of corner pads
Misaligned BGA before reflow	I	1	BGAs misaligned during pick and place by 50% of pad radius in diagonal direction
		2	BGAs misaligned during pick and place by 70% of pad radius in diagonal direction
Solder Paste Mis-registered	J	1	In screen printing, solder paste mis-registered by 50% of pad radius in diagonal direction
		2	In screen printing, solder paste mis-registered by 70% of pad radius in diagonal direction
Low Solder Paste Volume	K	1	Stencil aperture opening reduced to 0.24 x 0.24 mm
		2	Stencil aperture opening reduced to 0.2 x 0.2 mm

Low Peak Reflow Temperature	L	1	Peak reflow temperature reduced to 225 °C
High Peak Reflow Temperature	M	1	Peak reflow temperature increased to 265 °C
Reworked Components	H	1	Assembled components removed using rework tool, pads dressed with solder wick and new components assembled
PCB Bent After Assembly	B	1	Assembled module bent 3 times to 600 microstrain (0.2 mm)
		2	Assembled module bent 3 times to 1000 microstrain (0.33 mm)
Partially Lifted PCB Pad	G	1	Corner PCB pads lifted prior to assembly
Control	X	1	No Defects

Below is a more detailed account of how each of these defects was created:

(i) *Pad Contamination (Codes C and D):* Non-wetting contamination of PCB pads can result from defective PCB design, PCB fabrication, or a contaminating environment at assembly. Two types of contaminants were considered, namely; solder mask (code C) and silk screen (code D). The advantage of these contaminants, compared to others like flux residue, lubricant, dust, or packing materials is that their location and magnitudes could be easily controlled. The three corner-most pads of each component corner were intentionally covered during the PCB design stage. The coverage was along 50% of the pad diameter for level 1, and 70% of the pad diameter for level 2 defects. While the silk screen coverage was applied in a rectangular shape, the solder mask coverage was applied by offsetting the mask opening (see figure 2).

(ii) *Oxidized Pads (Code E):* Marginal solder-joints due to partially or completely oxidized pads may occur due to excursions in the PCB fabrication or storage conditions. While this type of defect could occur randomly at any location, the worst case condition was simulated by creating this defect at the 3 corner-most pads at all 4 corners of the BGA footprint. A peelable mask layer, completely covering the BGA corner pads, was placed underneath the OSP layer at the PCB design stage. By doing this, the OSP film at the corners was deposited on top of the

peelable mask at corner pads. Prior to assembly, the peelable mask was stripped, thereby also stripping away the OSP film at the corner pads. The level 1 defect was created by exposing the bare Cu pads to two days of ambient air environment prior to reflow. This resulted in a slightly visible discoloration of the corner pads. The level 2 defect was created by subjecting the MiniDIMM cards with exposed Cu pads to two reflow cycles prior to actual SMT assembly. This resulted in significant discoloration of the corner pads (figure 2).

(iii) *Partial OSP Coverage (Code F)*: This type of defect was created to simulate a marginal OSP coverage or poor handling of PCBs, which could result in partially exposed Cu pads. Similar to defect code E, a peelable mask layer covering approximately 70 to 90% of the corner pads was used to strip the OSP layer. The components were reflowed soon after that. Note that the exact placement of the peelable mask over pads was not possible during PCB fabrication, hence the coverage ranged from 70 to 90%.

(iv) *Misaligned BGA (Code I)*: This type of defect could be caused due to improper fiducial marks, improper programming of pick and place equipment or improper handling of the PCB after component placement but prior to reflow. The pick and place equipment was programmed to intentionally offset the component placement. The offset was 50% (for level 1) or 70% (for level 2) of the pad diameter along the diagonal direction (see figure 2).

(v) *Mis-registered Solder Paste (Code J)*: This defect could result from defective stencil or PCB design, or improperly handling the PCB or stencil prior to screen printing. The defects were created on a PCB level by intentionally offsetting the stencil by 50% (for level 1) or 70% (for level 2) of the pad diameter along the diagonal direction (see figure 2).

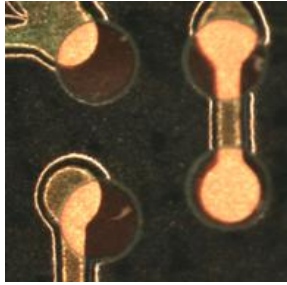
(vi) *Low Solder Paste Volume (Code K)*: This type of defect results from an improper stencil aperture or aspect ratio of stencil opening aperture. It could also be caused by use of inappropriate paste. The aperture opening was reduced to 0.24 x 24 mm (for level 1) and 0.2 x 0.2 mm (for level 2). The stencil thickness was kept constant (figure 2). The resultant average paste volume was measured to have reduced from $16.2 \times 10^6 \mu\text{m}^3$ (control) to $5.6 \times 10^6 \mu\text{m}^3$ (for level 1) and $3.4 \times 10^6 \mu\text{m}^3$ (for level 2).

(vii) *Lower or Higher Peak Reflow Temperature (Codes L and M)*: This type of process excursion can occur if the reflow chamber variables are not well controlled or if are unexpected changes to the thermal mass of the assembly. The normal card assembly was done with peak reflow temperatures in the range 235 °C to 245 °C. For defect code L, the target peak reflow temperature was reduced to 225 °C, the measured peak temperature ranged between 222 – 223 °C, and the time above liquidus ranged between 42 to 53 seconds. For defect code M, the target was increased to 265 °C, and the actual measured temperature ranged between 263 – 267 °C. The time above liquidus ranged between 83 to 89 seconds.

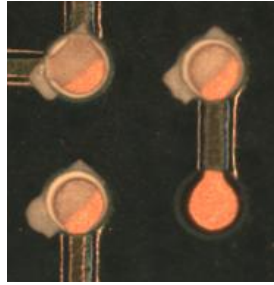
(viii) *Reworked Components (Code H)*: Marginal solder joints can sometimes result if an uncontrolled rework process is used. In this case, all components were first assembled using the normal process. Following this all components on single sided cards, and components from the primary side of double sided cards, were removed using an SRT rework station. The peak removal temperature was 240 °C. Following this the pads were dressed using a soldering iron and Copper wick. A tacky paste was spread on the pads, new components were placed using the rework station, and subsequently assembled using the normal reflow process.

(ix) *Bent PCB (code B)*: Brittle solder-joint cracking or pad cratering are serious latent defects that can be introduced by excessive PCB bending [3, 4]. In this case the cards were assembled using a normal assembly process. Following this the modules were subjected to 3 cycles of controlled 4-point bending according to IPC-9702 [10]. The strain rate was 8000 microstrain/second. The peak strain was 600 microstrain for level 1, and 1000 microstrain for level 2.

(x) *Lifted PCB Pads (Code G)*: This type of defect could result either from a defective PCB lamination process or due to excessive PCB pending. To create this defect one corner pad at each of the four corners of the pad array was designed to have a dummy trace attached to it. Prior to assembly, the dummy trace was peeled away from the PCB until the pad it connected to was completely lifted. Care was taken to ensure that the extent of pad lift did not break the connection of the pad to the 'live' trace.



C – 50% Solder Mask



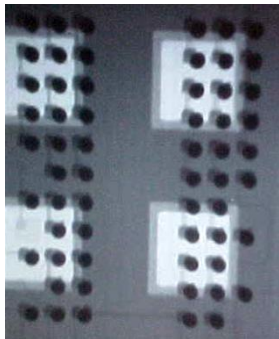
D -50% Silk Coverage



E – Oxidized Pad Level 1



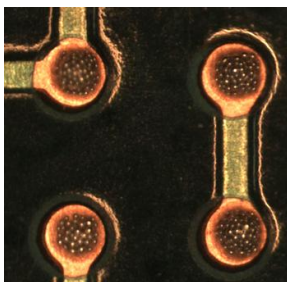
E – Oxidized Pad Level 2



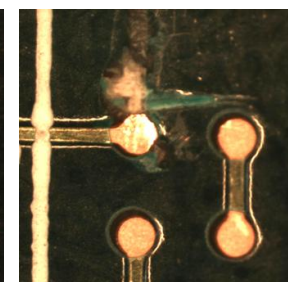
I – 70% Misalignment



J -70% Misregistration



K – Low Paste Volume



G –Lifted Pad

Figure 2 - Examples of Solder Joint Defects Created

Reliability Test and Results

The assembled single and double sided MiniDIMM cards were placed in a thermal cycling chamber. Accelerated Thermal Cycling (ATC) was

performed in a temperature range of 0 °C to 100 °C. The ramp rate was 10 °C per minute, and the dwell time at the hot and cold temperature was 10 minutes (figure 3). The resistance of each individual daisy chain device was continuously monitored using a data logger. A resistance value greater than 100 Ohm was logged as a failure. Once all devices on a card failed the card was removed from the ATC chamber and one device on each card was subjected to “Dye and Pry” and cross-section analysis.

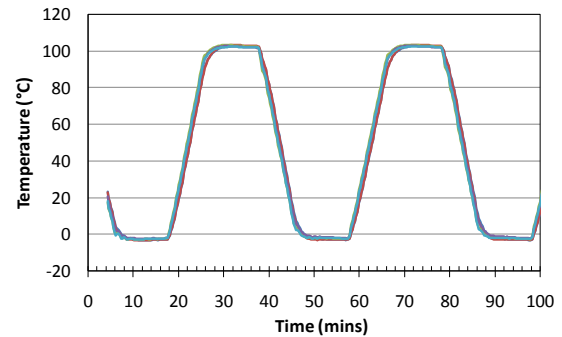


Figure 3 - Thermal Cycle Profile

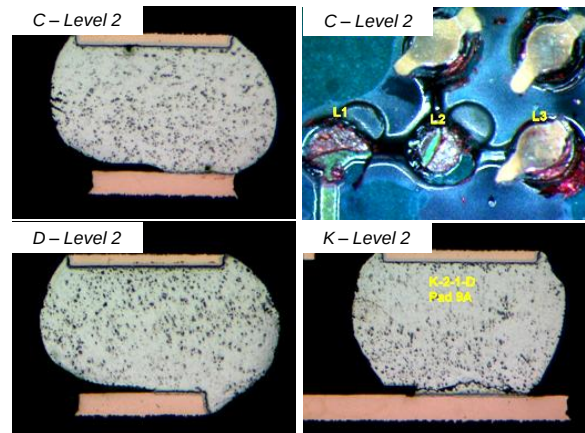


Figure 4 - Defective Solder Joints after Cross-section and Dye and Pry

Figure 4 shows examples of marginal solder joints (defect codes C, D, and K) observed from cross-sections and dye and pry. As expected, the failures were at the corner solder joints near the PCB pad interface. The ATC testing was still continuing at the time of this publication. The results after 4625 cycles are summarized in Tables 2 and 3 below for single sided and double sided card assembly.

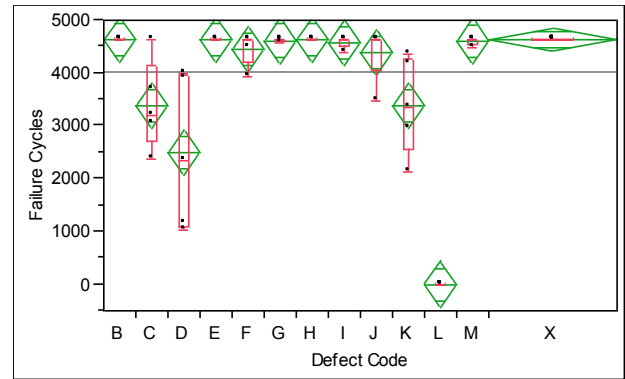
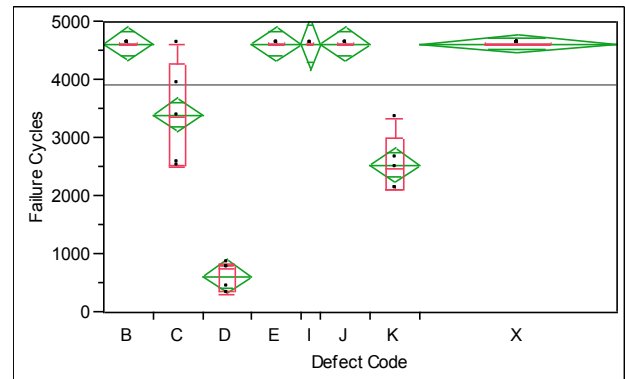
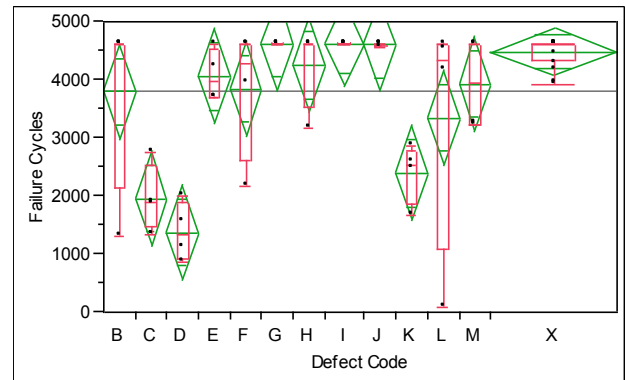
Table 2 - Summary of Single Sided Card Failures after 4625 Cycles

Defect Type	Defect Code	Level	Sample Size	First Failure Cycles	Cumulative Failure %
PCB Pad Contamination	C	1	5	2361	80%
		2	5	2513	80%
	D	1	5	1034	100%
		2	5	300	100%
Oxidized PCB Pads	E	1	5	No Failure	
		2	5	No Failure	
Partial OSP on PCB Pads	F	1	5	3920	40%
Misaligned BGA before reflow	I	1	5	4384	20%
		2	2	No Failure	
Solder Paste Mis-registered	J	1	5	3485	20%
		2	5	No Failure	
Low Solder Paste Volume	K	1	5	2130	100%
		2	5	2106	100%
Low Peak Reflow Temperature	L	1	5	1	100%
High Peak Reflow Temperature	M	1	5	4478	20%
Reworked Components	H	1	5	No Failure	
PCB Bent After Assembly	B	1	5	No Failure	
		2	5	No Failure	
Partially Lifted PCB Pad	G	1	5	4586	20%
Control	X	1	20	No Failure	

Table 3 - Summary of Double Sided Card Failures after 4625 Cycles

Defect Type	Defect Code	Level	Sample Size	First Failure Cycles	Cumulative Failure %
PCB Pad Contamination	C	1	4	1329	100%
		2	4	801	100%
	D	1	4	862	100%
		2	4	248	100%
Oxidized PCB Pads	E	1	4	3698	75%
		2	4	3554	50%
Partial OSP on PCB Pads	F	1	4	2163	50%
Misaligned BGA before reflow	I	1	5	No Failure	
		2	4	3600	75%
Solder Paste Mis-registered	J	1	4	4565	25%
		2	4	No Failure	
Low Solder Paste Volume	K	1	4	1676	100%
		2	4	846	100%
Low Peak Reflow Temperature	L	1	4	73	75%
High Peak Reflow Temperature	M	1	4	3211	50%
Reworked Components	H	1	4	3154	25%
PCB Bent After Assembly	B	1	4	1300	25%
		2	4	No Failure	
Partially Lifted PCB Pad	G	1	4	No Failure	
Control	X	1	16	3912	31%

Figures 5 to 8 show the scatter plots for all defect codes with levels 1 and 2, in single and double sided modules. Note that while many of the samples had not failed at the time of this publication, for the purpose of generating the scatter plots, all surviving samples were assumed to have failed at the next cycle (i.e., 4626 cycles). This conservative assumption was necessary in order to include the effect of the survivors on the mean and standard deviations.

**Figure 5 - Scatter plot of Single Sided Card Failures, Defect Level 1****Figure 6 - Scatter plot of Single Sided Card Failures, Defect Level 2****Figure 7 - Scatter plot of Double Sided Card Failures, Defect Level 1**

For single sided cards, defect code L (low peak temperature) was clearly the worst. While these devices had normal resistance after assembly, they failed within 3 thermal cycles. Subsequent visual observation revealed that the solder paste in some of the joints had only partially melted. Pad contaminating defects D (silk screen) and C (solder

mask) were the next most devastating, especially defect D with level 2 (silk screen with 70% pad coverage). Defect code K (low solder paste volume) was also very damaging. The effects of other types of defects cannot be statistically separated from the control (code X) samples.

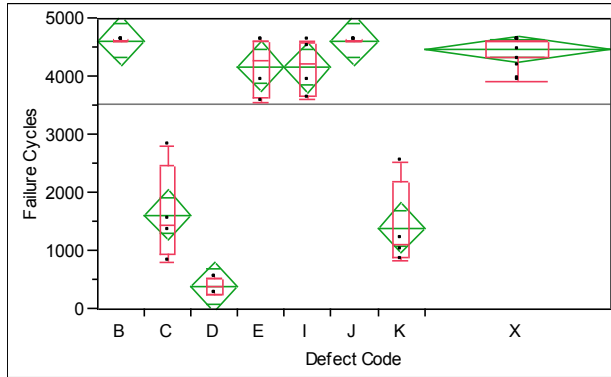


Figure 8 - Scatter plot of Double Sided Card Failures, Defect Level 2

For the double sided cards also, based on the first failure point and the scatter plots, defect code L (low peak reflow temperature) was the worst. This was followed by defect code D (silk screen contamination) which was particularly damaging at level 2. The next worst defect was code C (solder mask contamination), followed by defect code K (low solder paste volume). Based on a single failure, the next worst failure was the mechanically bent module (code B). This was followed by code F (partially exposed OSP pads). Based on limited sampling, codes M (high peak reflow temperature) and H (reworked components) also had some detrimental impact on reliability. At this time the effects of other defect codes could not be statistically separated from the control samples.

It is interesting to note that some severe defects like G (lifted pad), E (oxidized pads), I (misaligned BGA) and J (paste misalignment) have so far not shown early failures. In the case of defect G, the lifted pad may have reduced some stress on the solder joint. The result from defects I and J are showing that the molten BGA spheres and paste have excellent self aligning properties. While these defects have so far not caused early failures in thermal cycling, it is important to caution against underestimating their impact in other types of harsh environments like mechanical vibration or mechanical shock. Therefore the goal must be to always eliminate latent defects from manufacturing.

Summary

A novel test vehicle was developed wherein customized process parameters were used to intentionally generate a variety of latent defects in 0.8 mm pitch lead free solder joints. The cards were assembled in both single sided and double sided (back to back) configurations and subjected to board level ATC in the range 0 to 100 °C. At the time of this publication, 4625 cycles had been completed. Based on the early failures, the types of defects that had the most significant impact on solder joint fatigue life were identified.

In both single and double sided card assembly, lowering the targeted peak reflow temperature had the worst impact. Poorly formed corner solder joints due to a non-wetting contaminant on the PCB pads was the next most damaging type of defect. A reduced solder paste volume was also very impactful to reliability. In contrast to these variables, the solder joint fatigue reliability was found to be relatively less sensitive to some other process variants like a high reflow temperature, reworking the components, mis-registered solder paste, or misaligned BGAs.

While the test vehicle in this study was based on a MiniDIMM card, the results can be applicable to larger boards to gain some insights into a robust process “window”. In actual assembly practices, tremendous efforts are focused to optimize the design, processing, and handling of our products to ensure product quality and reliability.

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