

Advanced Wafer-Level Integration Technology with Ultra Fine Pitch Redistributed layers between Heterogeneous Devices

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Abstract

The authors have proposed Pseudo-SOC Technology realizing integration of heterogeneous devices with resin and have established basic key technologies. In this paper, the authors show summary of the technology as well as the results of the ultimate refinement of redistributed layer on the pseudo-SOC as the state of the art. It is indispensable to integrate heterogeneous devices with narrow gap and to interconnect them with fine pitch redistributed layer (global layer) to realize high-density integration in the pseudo-SOC. Vacuum printing condition was optimized for forming resin in the narrow gap without voids. The step was also reduced to less than 1 μ m by optimizing the condition of mounting devices and forming planar layer. Adhesion of the redistributed layer was also optimized by tuning the formation condition of planar layer. The etching condition was also optimized for reducing the line width of the redistributed layer. As a result, a fine pitch redistributed layer with as narrow as 1 μ m/1 μ m in line/space was realized on the pseudo-SOC by using wet etching technique. Finally, a pseudo-SOC where LSI and MEMS were integrated and connected with fine pitch redistributed layers was fabricated successfully as a demonstration of this technology. From these results, it was confirmed that high density integration of heterogeneous devices is realized by the advanced pseudo-SOC technology.

Keywords: Wafer-Level Integration, pseudo-SOC, Redistributed layers

1. Introduction

High density integration of heterogeneous devices such as LSI, passive components or MEMS (Microelectronic Mechanical System) has been required due to the demand of miniaturization of electronic devices for portable terminals such as cell phones and mobile PCs. Recently, integration of MEMS and LSI is demanded since MEMS can be utilized for various devices such as acceleration sensors, pressure sensors, optical engines for display and memory devices [1-2].

The main stream of the technology to integrate heterogeneous devices is SOC (System on Device) and SIP (System in Package) [3]. SOC technology realizes monolithic integrated devices by using the most advanced semiconductor process, realizing high-density device integration. However, it is not easy to integrate heterogeneous devices of MEMS and LSI by SOC technology due to the lack of the compatibility in both fabrication processes. On the other hand, SIP technology realizes the integration of heterogeneous devices of MEMS and LSI easily by using interposer substrate. However, the integration density is rather low as it is difficult to reduce the pitch of the interconnecting layers buried in the interposer substrate to a fine pitch of several microns necessary for the high-density device integration.

The authors have proposed pseudo-SOC technology that is set up with heterogeneous devices embedded with epoxy resin, planar layer and redistributed layer. Figure 1 shows the schematic view of pseudo-SOC. The pseudo-SOC is set up with heterogeneous devices formed by means of the corresponding fabrication technologies, with epoxy resin, planar layer and redistributed (thin-film metal) layer. The heterogeneous devices are separated and selected as KGD (Known Good Die) devices before being redistributed and integrated to a redistributed wafer. Thus heterogeneous devices are integrated in one device, same as SIP. By forming redistributed layer (global layer) with the most advanced semiconductor process, redistributed layer with fine pitch can be achieved. Thus, integration of MEMS and LSI with high density can be also achieved, same as SOC [4-8].

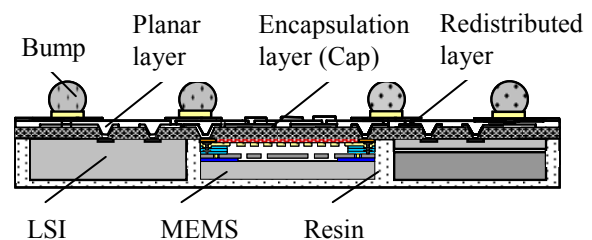


Figure 1: Schematic view of pseudo-SOC [8]

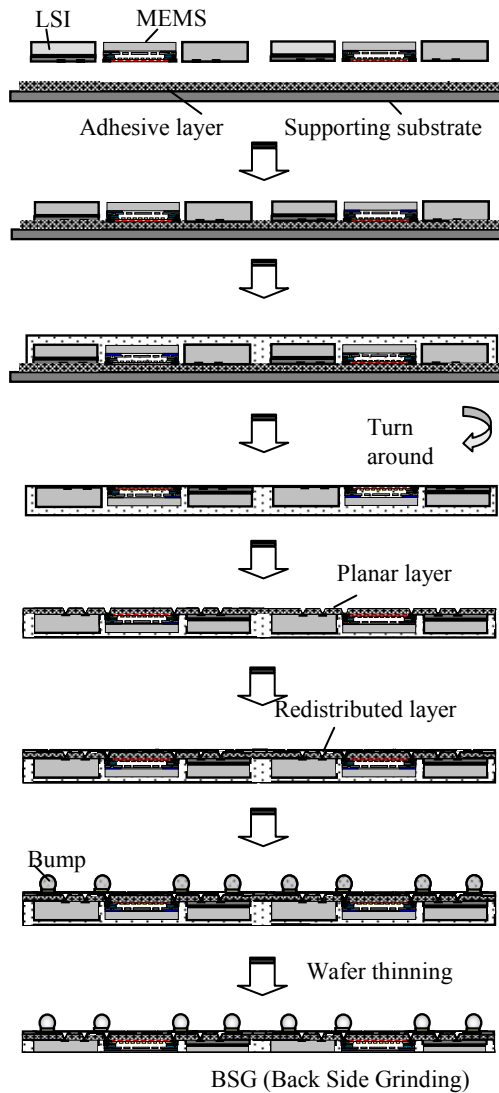


Figure 2: Basic process of pseudo-SOC [8]

The final goal is to realize the fine pitch of $1\mu\text{m}/1\mu\text{m}$ in Line/Space on pseudo-SOC in order to realize high-density integration of heterogeneous devices same as SOC. In the previous studies, redistributed layer with a fine pitch of $15\mu\text{m}/15\mu\text{m}$ in Line/Space was realized by optimizing the pseudo-SOC process. This paper presents summary of the pseudo-SOC technology and the results of the ultimate refinement of redistributed layer on the pseudo-SOC by tuning the etching process.

II. Basic Process of Pseudo-SOC

Figure 2 shows a basic fabrication process of MEMS-LSI integrated pseudo-SOC [8]. The process consists of three main steps: heterogeneous device reconfiguration step, redistributed layer formation step and pseudo-SOC wafer thinning process. In the heterogeneous device reconfiguration step, heterogeneous devices of MEMS and LSI, fabricated at individual fabrication technology are reconfigured on an adhesive layer

of a supporting substrate. The MEMS and the LSI are covered with epoxy resin by applying vacuum printing process. In the redistributed layer formation process, an insulating layer is formed on the reconfigured devices as a planar layer to the step between the resin and the devices. The thin-film metal layer is formed on the planar layer, formed as redistributed layer between the heterogeneous devices. By using the advanced semiconductor process, the redistributed layer is formed with fine pitch. In the pseudo-SOC wafer thinning process, the wafer is ground in order to achieve ultra-thin pseudo-SOC.

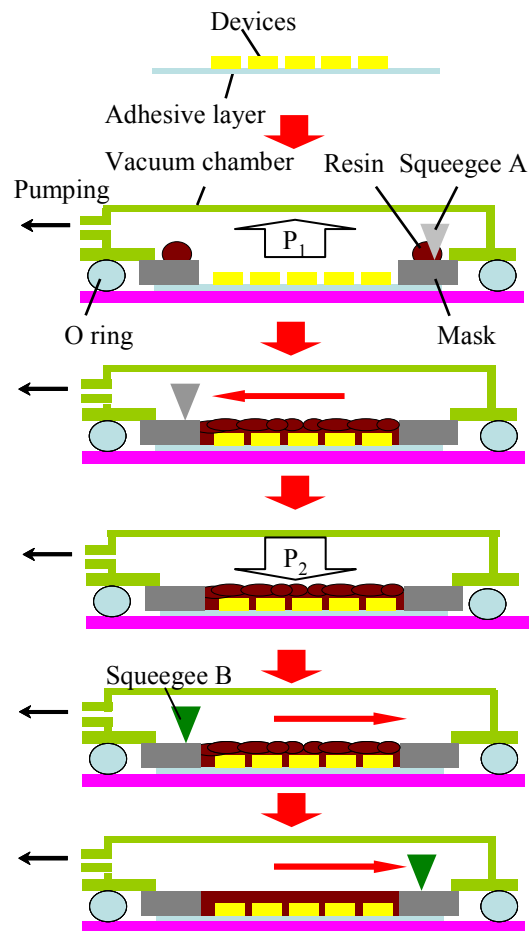


Figure 3: Vacuum printing process [7]

Figure 3 shows the detail of the vacuum printing process [7]. An adhesive layer on which devices are mounted was introduced into a vacuum chamber, and the pressure was reduced to a back pressure by pumping. The pressure in the chamber was controlled to a primary pressure and the resin was spread by a squeegee A. The pressure was changed several times between the primary pressure and a secondary pressure in order to reduce air bubbles mixed in the resin. The resin was planarized by a squeegee B in the secondary pressure. In the vacuum printing method, the

quantity of the bubbles in the resin can be reduced greatly by printing the resin in the diminished pressure atmosphere. Furthermore, good filling to the narrow gap region between the devices can be achieved by controlling the primary pressure and the secondary pressure.

III. Device Integration with Narrow Gap

A. Problems for device integration with narrow gap

Figure 4 shows a model of pseudo-SOC structure with narrow gap. In this structure, it is necessary to integrate the devices with enough position accuracy at the heterogeneous device reconfiguration step. Since the devices are mounted on the adhesive layer before being encapsulated with resin, the position accuracy at the mounting step must be elevated. At the printing step, it is indispensable to fill the narrow gap region with resin without voids in order to adhere the heterogeneous devices in the narrow gap between the devices. Thus, printing condition must be optimized for realizing good resin filling into the gap from the underside of this figure. Resin characteristics must be also optimized to increase the adhesivity as well as the mechanical strength in order to adhere and support the integrated devices.

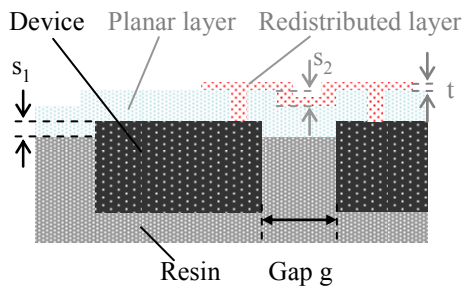


Figure 4: Model of pseudo-SOC with narrow gap structure

B. Optimization of mounting process

TEG (Test Element Group) chips (2.13mm x 2.13mm x 200μm) were mounted at room temperature on an adhesive supported on glass substrate, using flip chip bonder FCB3 (Panasonic Microelectronics). Mounting forces were varied from 1N to 100N and the relation between the mounting accuracy and the mounting force was evaluated. The deviations dx in x-direction and dy in y-direction of the alignment marks on the TEG chip and those of the glass substrate were measured using optical microscope. The mounting accuracy was evaluated from the mounting deviation dr defined as the following equation:

$$dr = (dx^2 + dy^2)^{1/2} \quad (1)$$

Figure 5 shows the measurement results of the relation between the mounting deviation dr and the mounting force F . As shown in this figure, the mounting deviation dr was decreased by decreasing the mounting force F . The mounting deviation decreased less than 1μm if the mounting force F was 1N.

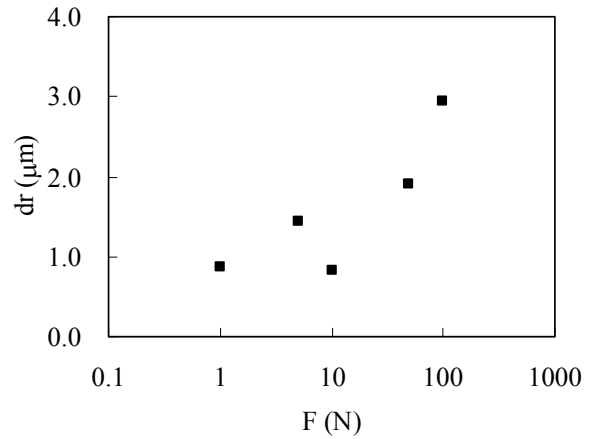


Figure 5: Relation between the mounting force F and the mounting deviation dr

C. Optimization of printing process

A bare silicon wafer of the thickness of 400μm with a gap region of 110μm in width formed on an adhesive layer was prepared and encapsulated with resin using the vacuum printing process. Printing condition was varied in order to maximize the filling ratio and to minimize the step s_1 . As the printing condition, the primary pressure P_1 and the secondary pressure P_2 were optimized. The primary pressure P_1 was varied from 0.2 to 80kPa where the P_2 was set to 80kPa. The pressure P_2 was also varied in the region between 0.2 and 2kPa where the P_1 was set to 0.2kPa. The step between the gap s_1 was measured using laser microscope.

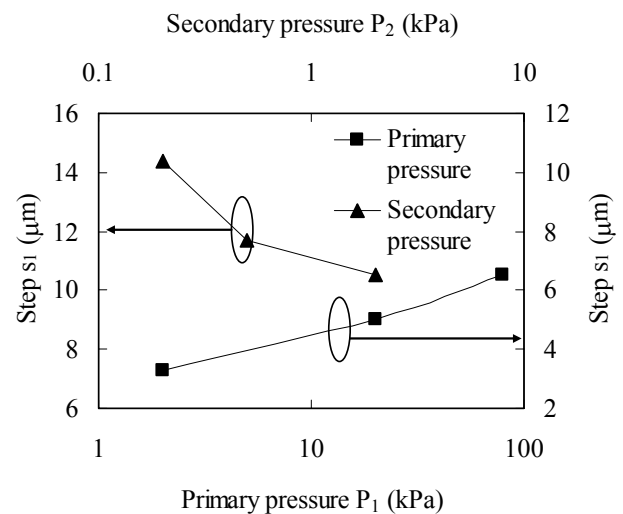


Figure 6: Relation between the step s_1 and the printing pressures P_1 and P_2 [7]

Figure 6 shows the relation between the printing pressure and the step s_1 . It was revealed that as the primary pressure P_1 decreases from 80kPa to 2kPa, the step between the chips and the resin at the gap region decreases to 70%. With regard to the secondary pressure P_2 , by increasing it from 0.2kPa to 2kPa, the step decreases to 70%. As the resin is spread by the squeegee A into the gap in the primary pressure P_1 , the resin can be filled into the gap without air bubbles or voids between the adhesive and the resin by decreasing the pressure of the atmosphere. On the other hand, since the resin can be pushed when being planarized with the squeegee B, it is preferable to elevate the secondary pressure P_2 . Thus, it would be preferable to control the secondary pressure P_2 to be more than the primary pressure P_1 in order to fill the resin into the narrow gap and to planarize the surface [7].

D. Optimization of resin characteristics

The characteristics of resin composed of base resin (epoxy) and filler (silica) was optimized by tuning the volume ratio of the filler V_f versus the base resin V_e to optimize the mechanical properties as well as the adhesivity of the resin. The fillers with rather large diameters, 20 μ m on average and with a maximum of 55 μ m, were selected. Under these conditions, only the filler volume ratio was varied.

The Young's modulus E was measured with the DMS (Dynamic Mechanical Spectroscopy) method using DMS6100 (SII Nano Technology Inc.). The modulation frequency was 10Hz, the heating rate was 10°C/min, and the sampling rate was 1sec. The material properties of the resin were analyzed from the material properties of the base resin and the filler. The Young's modulus of resin E was analyzed by the equation of Hopkins and Chamis, expressed as follows [9]:

$$E = E_e \{ 1 - V_f^{1/2} + V_f^{1/2} / \{ 1 - V_f^{1/2} (1 - E_e/E_f) \} \} \quad (2)$$

where E_e and E_f indicate the Young's moduli of base resin and filler, respectively. The Poisson's ratio of the resin ρ was analyzed by the following equation:

$$\rho = \rho_f V_f + \rho_e V_e \quad (3)$$

where ρ_e and ρ_f indicates the Poisson's ratio of the base resin and filler.

Figure 7 shows measurement results of the mechanical characteristics of the resin. The measured value (Exp.) and the analyzed value using the equations (Cal.) are plotted. The Young's modulus of the resin is increased rapidly by increasing the filler volume ratio, whereas the Poisson's ratio decreases. The dependences are

well fitted by the equations. Thus, the dependences can be explained from the model assuming that the resin is the composite of the base resin and the silica filler [4].

Table 1: Resin characteristics

Resin	O	A	B	C	D
Base resin volume ratio V_e (vol.%)	100	67	46	33	26
Filler volume ratio V_f (vol.%)	0	33	54	67	74

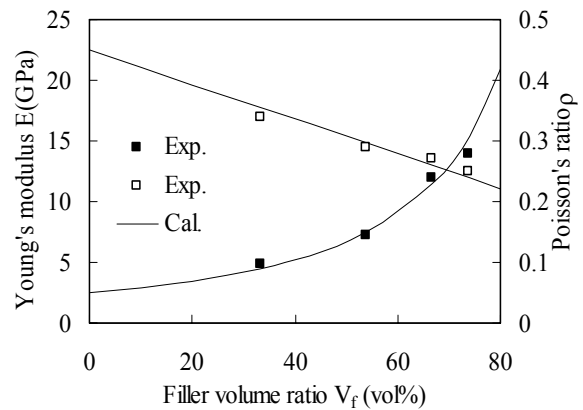


Figure 7: Mechanical characteristics of resin [4]

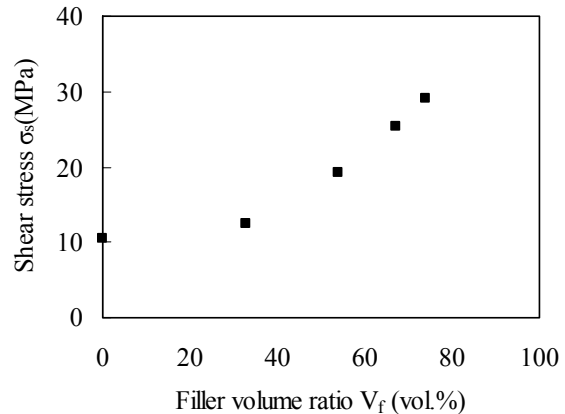


Figure 8: Relation between the shear stress and the filler volume ratio [6]

The adhesivity on the side of the chip and the resin governs the mechanical supportability especially the resin backside the chip is very thin or zero. On the side of the chip, shear stress may largely affect the adhesivity for the deflecting force. Thus the shear stress between the chip material and the resin was evaluated. Figure 8 shows the

measured results of the shear stress between Si substrate and the resin. As shown in this figure, the shear stress increased as the filler content increased. The shear stress of the resin C ($V_f=67\text{vol.}\%$) was about 3 times higher than that of the resin O ($V_f=0\text{vol.}\%$). From these observations, the breaking occurred on the surface between the Si substrate and the resin, and there were no residua on the breaking surface of the Si substrate as for the resin O and A, whereas there were some residua as for the resin B and C. Thus, the resin with higher filler had larger shear stress, and as a result the breaking occurred in the resin, not on the boundary between the substrate and the resin. This result implies that the resin with higher filler content has larger adhesivity contributing to the amelioration of the mechanical stability of pseudo-SOC [6]. Thus, it was revealed that the mechanical supportability of the resin increased by increasing the filler volume ratio.

E. Fabrication of pseudo-SOC with narrow gap

Figure 9 shows the overview and the cross-sectional view of a fabricated pseudo-SOC [4]. The gap was narrowed to $100\mu\text{m}$ and the resin thickness t_r was $400\mu\text{m}$. As shown in this figure, the resin was filled without voids. It was confirmed that the redistributed layer was formed on the planar layer across the inter-chip gap, indicating the surface step was lowered and planarized. Figure 10 shows thinned pseudo-SOC with narrow gap which were ground at the pseudo-SOC grinding process [8]. The gap was also narrowed to $100\mu\text{m}$ and the resin thickness was ground from $500\mu\text{m}$ to $300\mu\text{m}$ and $200\mu\text{m}$. No cracking, no peeling was observed between the resin and the integrated chips, indicating that the adhesivity and the mechanical supportability of the resin is sufficient high.

IV. Optimization of pseudo-SOC Surface and Formation of Fine-Pitch Redistributed layer

A. Problems for forming fine pitch redistributed layer

Figure 11 shows a model of pseudo-SOC with planar and redistributed layers. On the redistributed wafer surface, there may be induced a step s_1 between the devices and the resin due to the printing and the peeling process in the heterogeneous device reconfiguration step. Since the step s_2 may be induced even on the planar layer, the redistributed layer could be cracked or broken at the step if the coverage of the planar layer is insufficient. Furthermore, as the step s_2 increases, the resolution of the photo-resist pattern for redistributed layer may also deteriorate owing to the difference of the exposure gap under the mask at the UV exposure process. Thus, it is demanded to planarize the redistributed wafer surface in order

to realize a fine pitch redistributed layer. Adhesivity between the planar layer and the redistributed layer is also to be increased since the redistributed layer may be peeled off at the etching process. As the line width of the redistributed layer decreases, the adhesivity may decrease due to the decrease of the square between the redistributed layer and the underlying planar layer.

Finally, the etching condition of the redistributed layer must be optimized. In order to etch thin-film line and space pattern with fine pitch, dry etching technique such as Reactive Ion Etching (RIE) is utilized, since the thin-film layer can be etched with little undercut. However, RIE is rather costly process. From the viewpoint of cost reduction, wet etching technique is preferable. However, it is difficult to etch the thin-film layer without undercut. Thus the wet etching process was optimized to suppress the undercut and to realize fine-pitch redistributed layer on the pseudo-SOC.

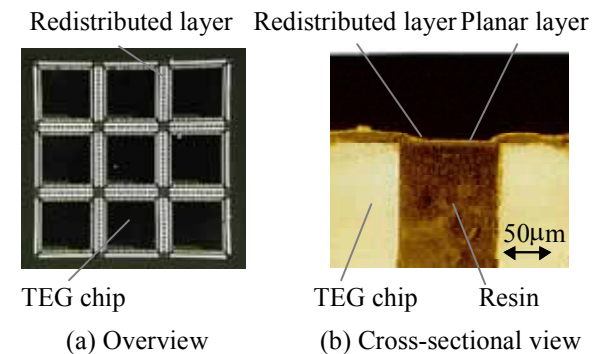


Figure 9: Overview and cross-sectional view of pseudo-SOC with narrow gap

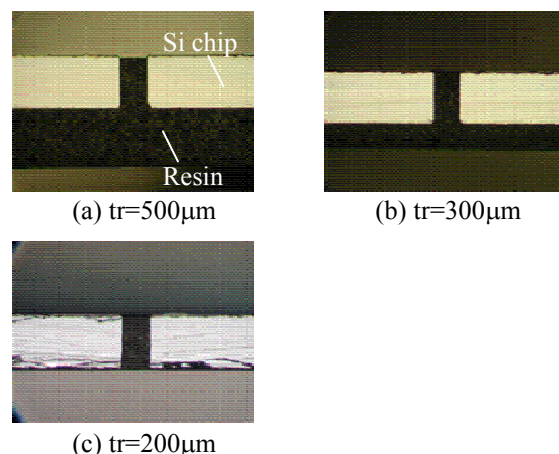


Figure 10: Cross-sectional view of thinned pseudo-SOC with narrow gap [8]

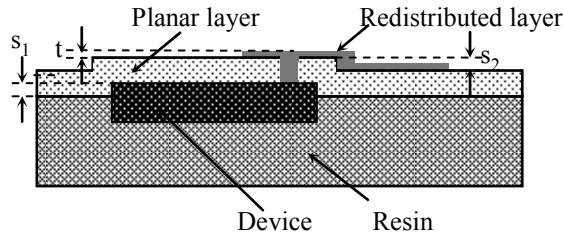


Figure 11: Model of pseudo-SOC with planar layer and redistributed layer

B. Planarization of pseudo-SOC surface

TEG chips (3.5mm x 3.5mm x 200 μ m) were mounted with flip-device bonder on adhesive sheet on a glass substrate. The adhesive sheet consisted of three layers: adhesive A, base film (PET) and adhesive B. The mounting force F was varied from 1N to 100N in order to investigate the effect of the deformation of the adhesive layer at the mounting process. The thickness of the adhesive A, indicated as d , was also varied from 4 to 50 μ m, as it is thought to be effective for reducing the deformation, while the thickness of the base film and the adhesive B was fixed to 100 μ m and 15 μ m, respectively.

Figure 12 shows the measurement results for the adhesive thickness dependence of the surface step on the redistributed wafer for various mounting forces. As shown in this figure, the step s_1 depends only on the thickness of the adhesive A, and by decreasing the thickness, the step can be reduced. By using an adhesive A of 4 μ m in thickness, the step s_2 was reduced to less than 5 μ m. The step was almost the same even if the force F was varied from 1 to 100N. Thus it was revealed that by decreasing the thickness of the adhesive A, the step s_1 may be decreased [7].

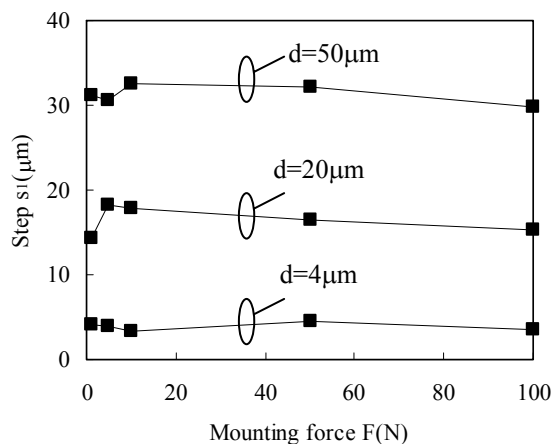


Figure 12: The relation between the step s_1 and the transfer condition: mounting force F and adhesive thickness d

C. Increase of adhesion of pseudo-SOC surface

Formation condition of the redistributed layer on the planar layer was optimized for forming redistributed layer with fine pitch. A plasma treatment was conducted with chemical dry etching machine CDE650 (Shibaura Eletec Co., Ltd.) The mixture of CF_4 and O_2 was plasma activated by the microwave power supply (2.45GHz) and then sprayed through the nozzles to the sample set on the rotating stage. Gas flow ratio of CF_4/O_2 was set to 40sccm/400sccm to confirm the adhesivity between the planar layer and the thin-film metal layer. Thin-film metal of Al/Ti was formed with the sputtering method. After photolithography process, the thin-film metal was etched with acidic solution.

Figure 13 shows the image after the etching of Al/Ti thin-film metal on a planar layer. Two materials A and B were prepared for the experiment. The line/spaces of the Al/Ti thin-film layer were 50 μ m/50 μ m, 15 μ m/15 μ m and 5 μ m/5 μ m. The etching condition, such as the etching time and etching temperature, was the same to compare the results. As shown in this figure, a part of the metal layer at finer pitch of 5 μ m/5 μ m in line/space was peeled off between the Ti layer and the underlying planar layer after the etching of Ti layer for material A cured at 220 $^{\circ}$ C whereas no peeling off occurred for the material A cured at 400 $^{\circ}$ C and the material B cured at 220 $^{\circ}$ C. Since the resin for pseudo-SOC is epoxy, the curing temperature must be the decomposition temperature of the epoxy material. Thus, the material B is preferable to the planar layer of pseudo-SOC on which fine pitch redistributed layer can be formed without being peeled off.

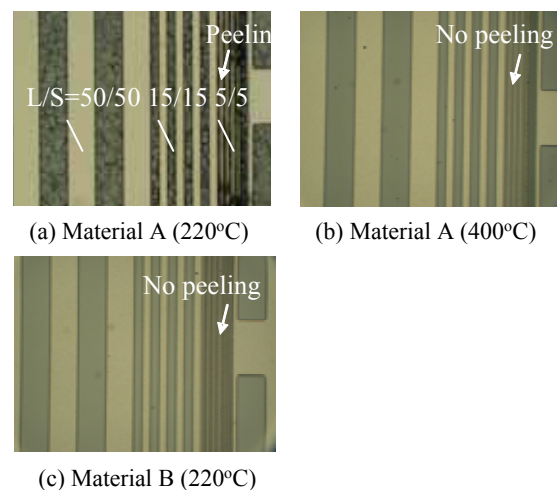


Figure 13: Relation between forming condition of the planar layer and the adhesivity of redistributed layer

D. Formation of fine-pitch redistributed layer on pseudo-SOC

Etching experiment was proceeded on planar layer of pseudo-SOC wafer to form line and space pattern with Al/Ti thin-film layer. After Al/Ti thin-film ($1.0\mu\text{m}/0.1\mu\text{m}$) was sputtered on planar layer of pseudo-SOC, photo-resist was formed using photo-lithography process, and then Al layer and Ti layer was etched sequentially with acid solutions and the pattern width of the line and space was measured. Figure 14 shows the relation between the pattern width on photo-mask and the width of the line pattern of the photo-resist, etched Al/Ti thin-film redistributed layer as well as the theoretical line indicating the limit of the finest line width according to the thickness of the Al/Ti thin-film layer. The thickness of the Al/Ti layer was varied in the theoretical estimation to evaluate the finest line width of the redistributed layer. Figure 14 shows the results. It was confirmed that the line width of the etched Al/Ti layer was narrower than that of the photo-resist pattern due to the undercut of wet etching process. Thus the finest line width of the Al/Ti layer ($1.0\mu\text{m}/0.1\mu\text{m}$) is estimated to be about $4.4\mu\text{m}$, whereas the line width can be narrowed to be $1\mu\text{m}$ if the thickness of the Al/Ti layer can be thinned to $1/5$.

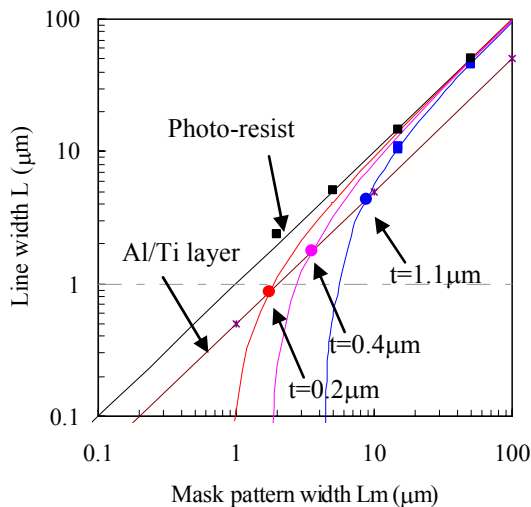


Figure 14: Relation between the line width of the redistributed layer and the photo-mask pattern

Figure 15 shows thin-film Al/Ti redistributed layers formed on the planar layer of the pseudo-SOC composed of TEG devices integrated with a narrow gap of about $100\mu\text{m}$ and epoxy resin encapsulating them. The thickness of the metal was $0.2\mu\text{m}$ for Al layer and $0.02\mu\text{m}$ for Ti layer. The line width was controlled from $3\mu\text{m}$ to $1\mu\text{m}$. Figure 16 shows line and space patterns of the Al/Ti redistributed layer. The thickness of the metal was $0.1\mu\text{m}$ for Al layer and $0.01\mu\text{m}$ for Ti layer. The

line and space of the layer was controlled from $5\mu\text{m}/5\mu\text{m}$ to $1\mu\text{m}/1\mu\text{m}$ by controlling the etching condition. No peeling and no cracking was observed even if the widths of the redistributed layer were thinned to $1\mu\text{m}$, indicating enough adhesivity and flatness was realized by tuning the redistributed layer process.

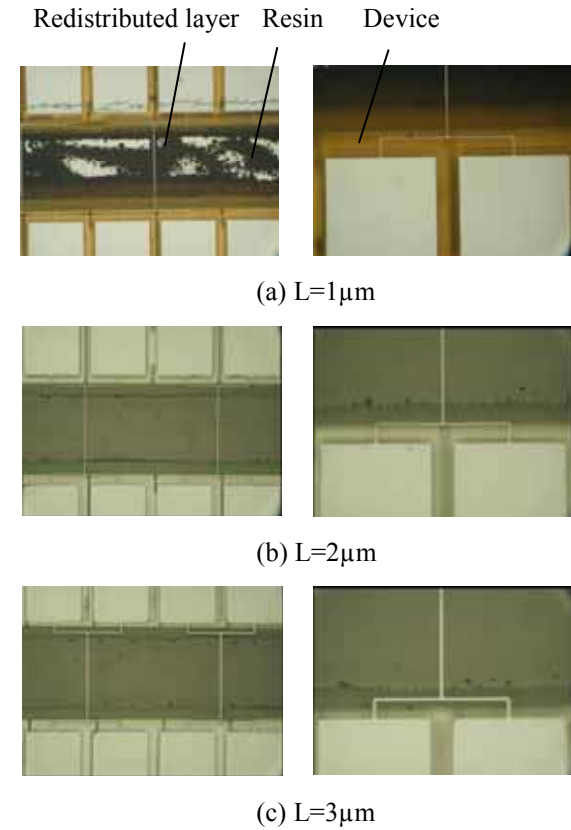


Figure 15: Overview of redistributed layer with fine line width on pseudo-SOC

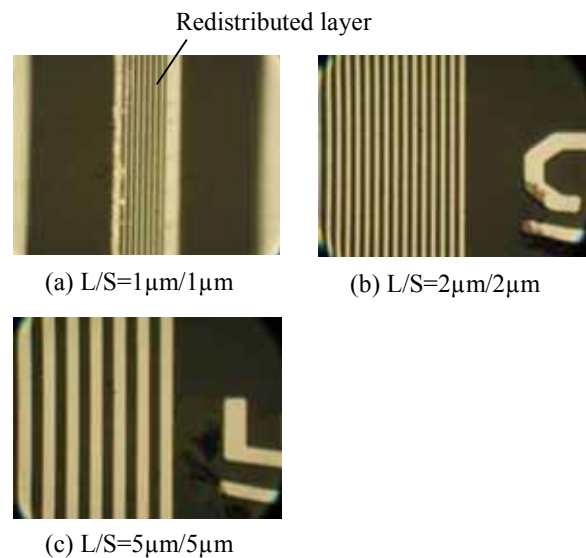


Figure 16: Overview of redistributed layer with fine pitch on pseudo-SOC

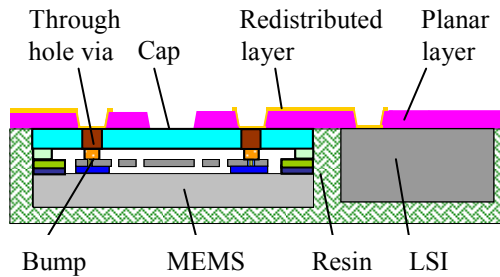


Figure 17: Schematic view of MEMS-LSI pseudo-SOC

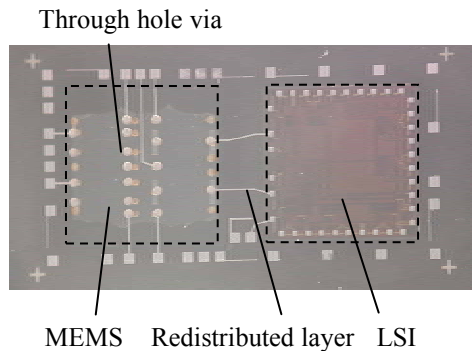


Figure 18: Overview of MEMS-LSI pseudo-SOC

E. Fabrication of MEMS-LSI pseudo SOC

Figure 17 shows a schematic cross-sectional view of MEMS-LSI pseudo-SOC and figure 18 shows overview of our developed MEMS-LSI pseudo-SOC. This pseudo-SOC is composed of MEMS for acceleration sensor element and LSI for sensing amplifier element. As shown in this figure, the heterogeneous devices are integrated and then connected successfully with thin-film redistributed layer with fine line width of $10\mu\text{m}$. It was confirmed that the MEMS and the LSI are connected with the redistributed layer from electronic measurement. As a result, heterogeneous devices of MEMS and LSI were integrated by the advanced pseudo-SOC technology with fine pitch redistributed layer.

V. Conclusions

The authors have proposed Pseudo-SOC Technology realizing integration of heterogeneous devices with resin. It is indispensable to integrate heterogeneous devices with narrow gap and to interconnect them with fine pitch redistributed layer (global layer) to realize high-density integration in the pseudo-SOC. Vacuum printing condition was optimized for forming resin in the narrow gap without voids. Furthermore, the step was reduced to less than $1\mu\text{m}$ by optimizing the condition of mounting devices and forming planar layer. Adhesion of the redistributed layer was also optimized by tuning the formation condition of planar layer and the etching condition of the redistributed layer. As a result, a fine pitch

redistributed layer with as narrow as $1\mu\text{m}/1\mu\text{m}$ in line/space was realized on the pseudo-SOC. Finally, a pseudo-SOC where LSI and MEMS were integrated and connected with fine pitch redistributed layers was fabricated successfully as a demonstration of this technology. From these results, it was confirmed that high density integration of heterogeneous devices is realized by the advanced pseudo-SOC technology.

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