

Development of Wafer Level Embedded SiP (System in Package) for Mobile Application

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Abstract

Recently the market for portable products, such as mobile phones, digital cameras, PDAs and game consoles, has been increasing rapidly and consumers like not only to carry small and light thing on the hand, but also have various functions with lower price. Accordingly, System in Package (SiP) technologies have been needed to get thin, small and light mobile products by putting various devices into only one electronic package. To satisfy the requirement, wafer level embedded system in package (WL-eSiP) has been considered and developed with the concept of wafer level flipchip bonding one or more chips inside a bigger chip (mother chip) and wafer level molding for underfilling and encapsulation by molding compound without special substrate to realize wafer level system in package (WLSiP) with thin and small size and high performance. Firstly, to realize Wafer Level System in Package (WLSiP), its structure and dielectric and molding compound materials have been selected and verified through reliability tests of MSL2, PCT (121°C/ 100%RH/ 2atm), TC (-40/125°C) and HTS (150°C) with specified experimental molded dies with various die size, dielectric materials and mold materials and they passed MSL2, 168hrs of PCT, 2000cycles of TC and 1000hrs of HTS. After optimizing WLSiP structure and its material, WLSiP test vehicle has been designed and fabricated to evaluate the package level and board level reliabilities for verifying process and package reliability. The mother chip of 4mm x4mm has been designed in daisy chain pattern electrically interconnected each other by solder bumps that are finally interconnected with redistribution layers on mold surface and solder balls to connect with the substrate for confirmation in terms of process and package and board level reliability. Its daughter chip size is 2.95mm x 2.31mm, of which thickness is 70um. First of all, whole manufacturing process of wafer level system in package (WLSiP) has been verified and developed, with redistribution, flipchip bumping (solder and Copper), wafer level flip-chip bonding, wafer level molding, Si and mold thinning and ball mounting technologies. Then, the fabricated WLSiP has been evaluated for package level reliability tests of MSL3, PCT (121°C/ 100%RH/ 2atm), TC (-40/125°C) and HTS (150°C) and all items have been passed. For the board level reliability test, daisy chain substrate has been designed and fabricated for TC (-40/125°C) and drop (1500G/ 0.5ms) tests and under evaluation.

Key words: Wafer Level embedded System in Package(WL-eSiP), Wafer Level Molding, Mobile Application

Introduction

As mobile phone leads the market, the market for portable products, such as mobile phones, digital cameras, PDAs and game consoles, has been growing rapidly and consumers like to carry small and light thing on the hand. In addition to that, they want more functions with lower price. So it's necessary to develop the semiconductor packages with thin and small size, high performance and low cost. Accordingly, System in Package (SiP) technology has been needed to get thin, small and light mobile products by putting various devices (functions) into only one electronic package. Of them, Embedded System in Package (eSiP) technologies have been emerging to get smaller, lighter and high functional package technologies by putting one or more chips inside one mother chip or the substrate.

Many companies have been developing and reported various types of embedded system in package, such as the embedded Wafer Level Ball Grid Array (eWLB) based on die placement, molding and thin-film process, the Redistributed Chip Package (RCP) using die placement, encapsulation and redistribution process. Moreover, Industrial Technology Research Institute (ITRI) in Taiwan and Institute of Microelectronics (IME) in Singapore have reported similar embedded technology based on die placement and encapsulation process. [2~8]

Recently, as embedded package come into the spotlight, wafer level embedded technologies with advantages of wafer level process has been emerging and published. Seemingly, wafer level system in package (WLSiP) looks like conventional wafer level

package (WLP), but WLSiP has two or more chips inside WLSiP that has daughter chips (smaller chip) onto mother chip (bigger chip) to expand WLP technology into SiP applications. Embedded packages are embedding one or more chips inside the substrate and one of the technologies to realize the packages with thin and small size and high performance but there is much room for improvement, such as process and reliability issues including yields. [1~8]

In this paper, wafer level embedded SiP (WL-eSiP) of which has daughter chip embedded onto mother chip by molding compound without special substrate has been developed in terms of structure, material and manufacturing process. Then, reliability tests have been performed for fabricated WL-eSiP to verify for the application of mobile products.

Experiments

Structure and Process Flow of WL-eSiP

Wafer level embedded SiP which has two chips inside one WLP of a mother chip and daughter chip has been developed to apply mobile products. Figure 1 shows cross-sectioned structure of wafer level embedded system in package (WL-eSiP). A flipchip bumped daughter chip is mounted on a mother chip and a daughter chip is embedded by mold compound onto the front side of a mother chip. So, the real size of WL-eSiP is the same as mother chip size.

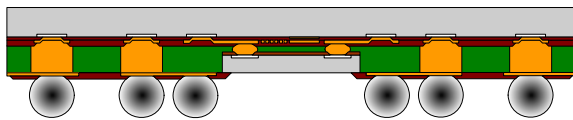


Figure 1. Wafer level embedded SiP structure

Figure 2 shows process flow to fabricate the WL-eSiP. Firstly, daughter chips and mother chips have been fabricated using redistribution, solder and Cu bumping process. Solder bumped daughter chips have been back-grinded down to 70um thickness on the wafer level and then diced. On mother chip, redistribution and Cu bumping has been done. And daughter chips have been cut and flip-chip bonded on mother chips at wafer level. After wafer level flip-chip bonding, compression molding has been performed at wafer level using epoxy molding compound. During this wafer molding process, under-filling of flip-chip bonding area and embedding of daughter chip has been done simultaneously. Then, grinding on the molded side has been performed until top side of Cu bump of mother chip is exposed. This exposed Cu surface will be electrically interconnected with Cu trace on mold.

From now on, the process is the same as conventional wafer level package with redistribution and solder bump. After wafer molding and mold side grinding, redistribution process has been and dielectric material has been spin-coated on Cu trace and mold surface and solder ball pad areas has been opened by photolithography. Finally, under bump metallurgy (UBM) and solder ball mounting process follow as shown in figure 2.

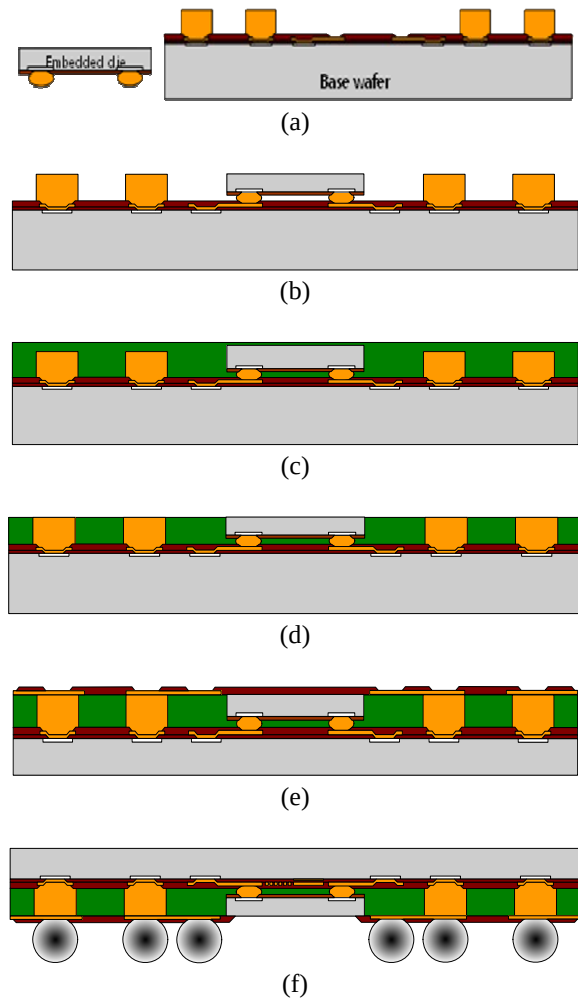


Figure 2. Process flow of Wafer level embedded SiP ; (a) Preparation of daughter chips & mother wafer, (b) wafer level flip chip bonding, (c) wafer level molding, (d) mold-side thinning, (e) redistribution process on mold surface and (f) Solder ball mounting & Singulation

Test Vehicle and Reliability Test Information

Before the design and fabrication of test vehicle, structure and materials for wafer level embedded

system in package (WL-eSiP) have been verified. To optimize the structure and materials of WL-eSiP, the reliability tests of Moisture Sensitive Level 2, Pressure cooker Test (168hrs, 121°C/100%RH/2atm), Temperature cycle (TC) test (1000cycles, -40/125°C) and High Temperature storage (HTS) test (1000 hrs, 150°C) have been performed with the test vehicles of 2 types of die sizes, 3 types of dielectric materials and 3 types of molding compound materials. Test vehicles have only three layers of Si chip, dielectric and mold compound material as shown in figure 3. More details will be discussed later in the part of Results and discussion.



Figure 3. Test Vehicle for optimizing WL-eSiP structure and materials

In view of the results of optimizing structure and materials as above, test vehicle of wafer level embedded system in package (WL-eSiP) of 4mm x 4mm mother chip size has been designed and fabricated with D2 dielectric and M3 molding compound materials. The daughter chip size is 2.95mm x 2.31mm and is needed to be grinded down to 70µm thickness. Figure 4 shows the design of 4mm x 4mm size WL-eSiP. Daughter and mother chips have been designed in the pattern of daisy chains and electrically interconnected by flip chip bonding of solder bumps of daughter chip onto redistribution layer of mother chip. This daisy chain loop on mother chip is also interconnected with the 2nd daisy chain loop that is rerouted on molding surface connected through Cu bump of mother chip. The 2nd daisy chain loop is also electrically interconnected with the 3rd daisy chain loop that is formed on the substrate through surface mounting by solder balls on WL-eSiP.

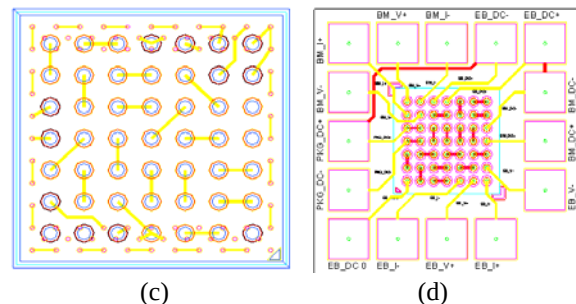
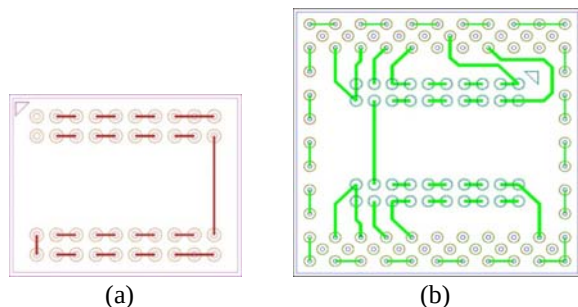


Figure 4. 4mm x 4mm size WL-eSiP test vehicle design ; (a) daughter chip of 2.95mm x 2.31mm size, (b) mother chip of 4.0mm x 4.0mm size, (c) redistribution on molding surface and ball pad and (d) Substrate for board level reliability test

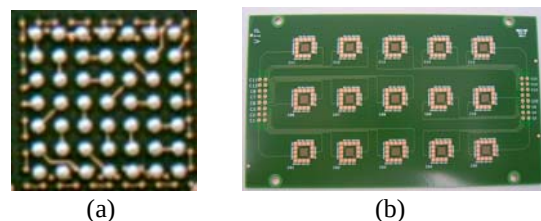


Figure 5. Board level reliability test vehicle images : (a) Fabricated WL-eSiP and (b) Temperature Cycle and Drop Shock Test Board

For fabricated WL-eSiP, reliability test has been performed at Package and Board level. Figure 5 shows fabricated WL-eSiP and Board for reliability items of PCT, HTS, TC and drop test. Board for TC and Drop test has been designed and fabricated based on JEDEC standard. Table 1 shows reliability test items and its conditions.

Table 1. Reliability test items and its conditions

Items		Condition
PKG level	Moisture Sensitive L2	24hrs@85%RH,85°C/reflow 3times@260°C
	Pressure Cooker Test	121°C, 100%RH, 2atm
	High Temp. Storage	150°C
	Temperature Cycle	-40~125°C
Board level	Temperature Cycle	-40~125°C
	Drop shock test	1500G/ 0.5ms

Results and Discussion

Optimization of Structure & Material of WL-eSiP

To design and optimize the WL-eSiP structure and materials, mold die test vehicles with 2 types of die sizes, 3 types of dielectric materials and 3 types of mold materials have been fabricated. Test vehicles

have only three layers of Si chip, dielectric and mold compound material. For the fabricated test vehicles, various reliability tests of MSL2, PCT (121°C/ 100%RH/ 2atm), TC (-40/125°C) and HTS (150°C) have been performed. First, TC items have evaluated for 3 types of mold compound and select MC3 mold compound. Then, reliability tests of PCT and HTS have been evaluated for each test vehicle.

Table 2. Summary of optimizing structure & materials

Items	Mold	Dielectric	Die size (mm ²)	Result
TC	MC1	D1	4 x 4	Fail
			6 x 6	Fail
		D2	4 x 4	Fail
			6 x 6	Fail
		D3	4 x 4	Fail
			6 x 6	Fail
	M2	D1	4 x 4	Fail
			6 x 6	Fail
		D2	4 x 4	Fail
			6 x 6	Fail
		D3	4 x 4	Fail
			6 x 6	Fail
PCT	MC3	D1	4 x 4	Pass
			6 x 6	Pass
		D2	4 x 4	Pass
			6 x 6	Pass
		D3	4 x 4	Pass
			6 x 6	Pass
HTS	MC3	D1	4 x 4	Fail
			6 x 6	Fail
		D2	4 x 4	Pass
			6 x 6	Fail
		D3	4 x 4	Fail
			6 x 6	Fail

In Table 2, test results for each test vehicle were summarized. All test vehicles passed moisture sensitive level 2 and PCT 168hrs. Test vehicles only with MC3 (molding compound 3) passed temperature cycle test except the test vehicle with D1 dielectric material and 4mm x 4mm die size. In case of high temperature storage test (HTST), the test vehicle with D2 dielectric material and 4mm x 4mm die size passed. According to the results as above, wafer level embedded system in package (WL-eSiP) of mother chip size of 4mm x 4mm with D2 dielectric material and MC3 molding compound material has been verified in terms of structure and material. Daisy chain for process optimization and reliability test will be designed based on the results so far achieved. The size of mother and daughter chips is 4mm x 4mm and 2.95mm x 2.31mm

respectively and daughter chip has 70um thickness. Figure 6 shows kind of failure modes that have been founded on the failed test vehicles, like delamination and crack.



Figure 6. Failure modes after reliability tests for test vehicles mold die ; (a) de-lamination between dielectric and mold materials and (b) Mold crack

Process Optimization

From the results of structure & material optimization, reliability test vehicle has been designed as shown in figure 4 and fabricated by process flow as shown in Figure 2. Firstly, daughter chips and mother chips have been fabricated using redistribution and solder or Cu bumping process on the wafer level. Fabricated daughter chips have been back-grinded down to 70um thickness. Mother chip is connected with redistribution layer on molding compound by Cu bump on mother chips that has 120um height. Process images of daughter and mother chip were shown in figure 7. And daughter chips have been cut and flip-chip bonded on mother chips at wafer level.

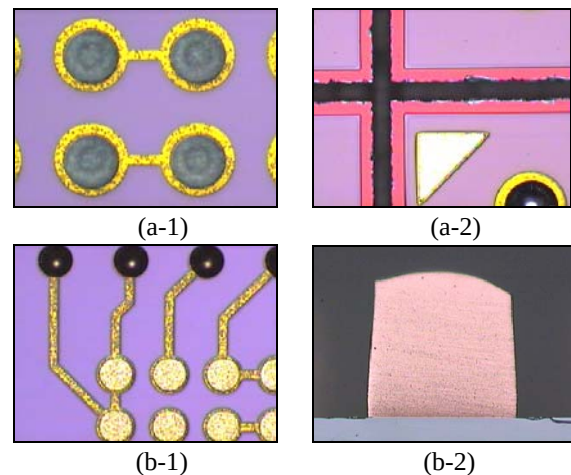


Figure 7. Process images ; (a-1) redistribution and solder bump, (a-2) thin wafer sawing line of daughter chip, (b-1) redistribution and solder bump and (b-2) Cu bump cross-section of mother chip

To confirm the quality of flip-chip bonding process, x-ray inspection and die shear test have been performed. As shown in figure 8, no void has been found within bonding areas and fracture mode of die shear test occurred in the inside of solder joint. Figure 8 shows flip-chip bonded wafer, its cross-sectioned image, x-ray inspection results and fracture mode of die shear test.

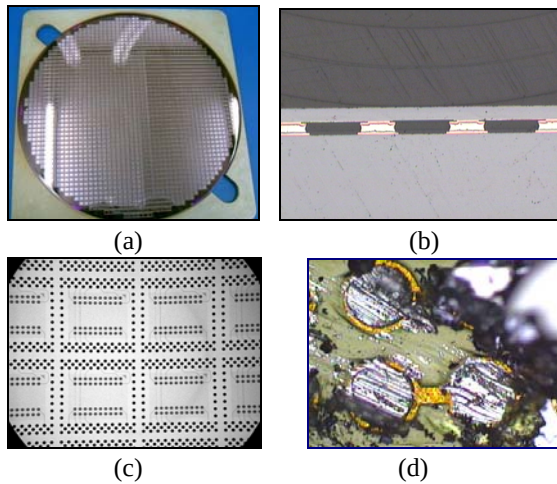


Figure 8. Images of (a) flip-chip bonded wafer, (b) cross-section, (c) x-ray inspection and (d) die shear fracture mode

After wafer level flip-chip bonding, wafer level molding process has been evaluated and finally verified at wafer level using epoxy molding compound in terms of encapsulation and underfilling between mother chip and daughter chip. Molding compound has small filler of maximum 10 μ m size to underfill the flip-chip bonding gap of low stand-off height. Molded layer thickness is 150 μ m. Through this wafer molding process, under-filling of flip-chip bonding area and encapsulation of daughter chip has been done at once. Figure 9 shows the images after wafer level molding process. Figure 9 (a) is mold wafer image and Figure 9 (b) is mold surface. There are no voids and any deformation on mold surface. Figure 9 (c) shows the cross-sectioned image after molding process. There is no void at gap filling of flip-chip bonding area and no voids or deformation for covering daughter chip.

For electrical interconnection between mother chip and redistribution layer that will be formed on molded wafer, grinding process onto the molded wafer side has been performed until top side of Cu bump of mother chip is exposed. This exposed Cu surface will be electrically interconnected with Cu trace on molded wafer surface.

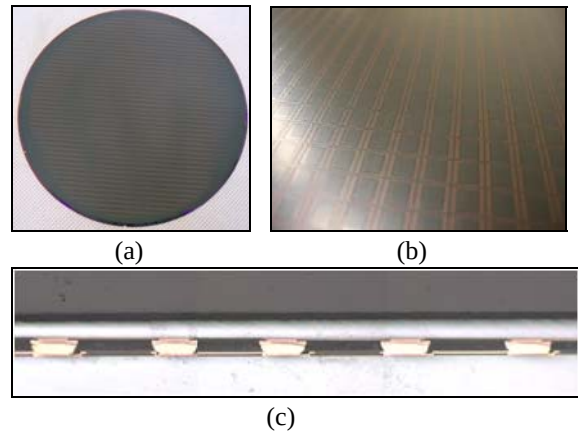


Figure 9. Images of (a) molded wafer, (b) molded wafer surface (c) its cross-sectioned image

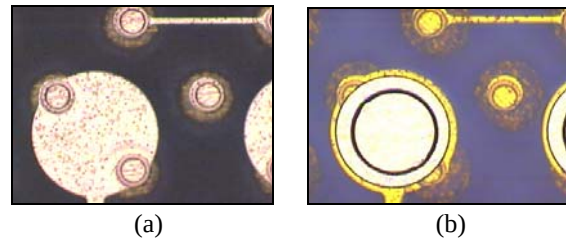


Figure 10. Images of (a) redistribution layer on molded wafer (b) UBM for solder ball mounting

After wafer molding and mold side grinding, redistribution process has been performed and trace is formed with copper by electro-plating method. Then, dielectric material has been spin-coated on Cu trace and mold surface. Solder ball pad areas has been opened by photolithography. Figure 10 shows the images of Cu trace, pad and pad opening on molded wafer surface. Under bump metallurgy (UBM) fabrication step followed. Then, back side of mother wafer has been thinned by mechanical grinding method to meet the requirement of final package thickness. Finally solder ball of SAC305 type has been mounted on UBM. Figure 11 (a) shows the top view of UBM and Figure 10 (b) is solder ball shape after solder ball mounting. Figure 10 (c) shows fabricated WL-eSiP by wafer level process and Figure 10 (d) shows its enlarged image.

Finally, individual WL-eSiPs for reliability test have been prepared by dicing for fabricated WL SiP wafer. Figure 12 shows the cross-sectioned images of fabricated WL-eSiP. Figure 12 (a) is whole WL-eSiP structure and there is no void in flip-chip bonding area and no mold deformation. There are no mold cracks or de-lamination as shown in figure 12 (b) for edge area

of WL-eSiP. Figure 12 (c) shows interconnection between Cu bump and solder ball.

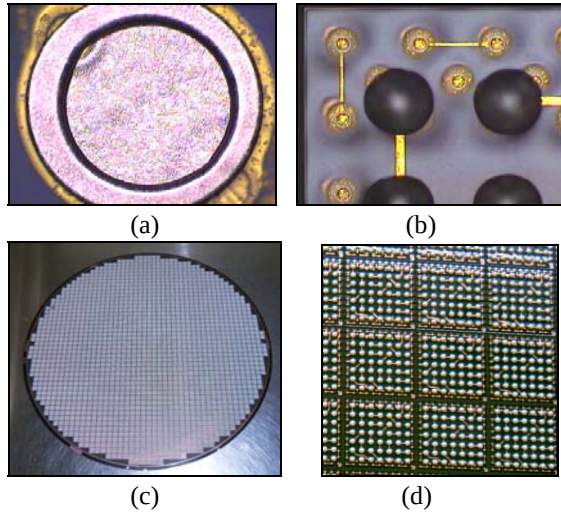


Figure 11. (a) top view of UBM for solder ball mounting, (b) solder ball shape of WL ESiP, (c) fabricated WL-eSiP and (d) enlarged WL-eSiP image

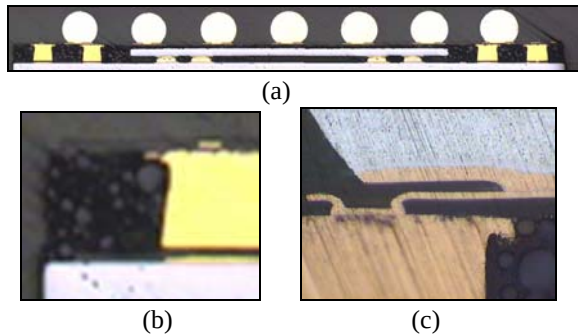


Figure 12. Cross-sectioned images of (a) whole WL-eSiP, (b) edge area of WL-eSiP and (c) interconnection between Cu bump and solder ball

Reliability Test Results

With the test vehicles optimized in terms of structure, materials and process, firstly, package level reliability tests of moisture sensitive level test (MSL2a), pressure cooker test (PCT) (168hrs, 121 °C/ 100%RH/2atm), temperature cycle test (500 cycles, -40/125 °C) and high temperature storage test (HTST) (1000hrs, 150 °C) have been performed and all test items have been passed. Table 3 shows the summary of reliability test items & condition, sample size and results of package level reliability tests.

Figure 13 shows inspection results after temperature cycle test. It has been confirmed that there are no dielectric cracks nor de-lamination at WL-eSiP surface as shown in figure 13 (a) and (b). And Figure 13 (c) shows no mold cracks, voids and de-lamination. Not only that, dielectric cracks or de-lamination and mold cracks, voids and de-lamination have never been found after humidity test (PCT) and high temperature storage test (HTST).

Table 3. Summary of Package level reliability items, conditions and the results

Items	Condition	S/Size	Result
MSL	Bake 24hrs@ 125 °C / Soak 24hrs@85%RH, 85 °C / reflow 3times@260 °C	30ea	MSL2a
PCT	121 °C, 100%RH, 2atm	5ea	168hrs
HTS	150 °C	25ea	1000hrs
TC	-40~125 °C	25ea	500cycles

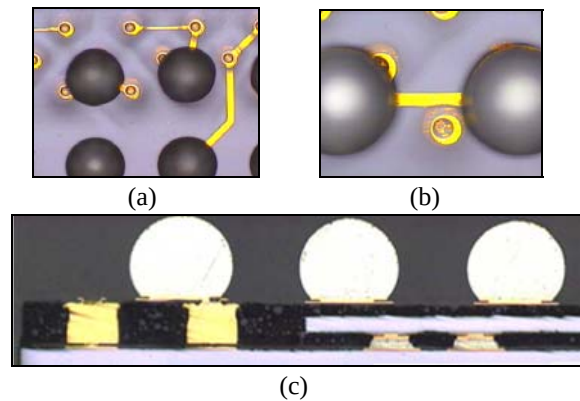


Figure 13. Inspection images after TC : (a) & (b) surface of WL-eSiP, (c) its cross-sectioned image

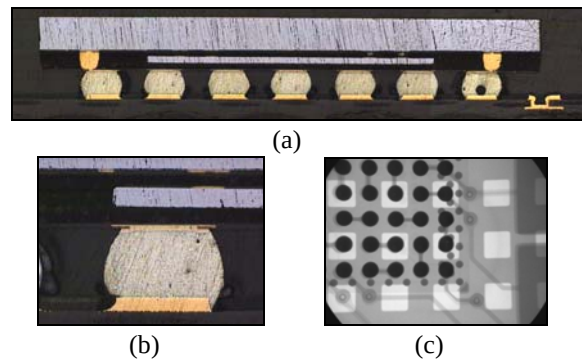


Figure 14. Cross-sectioned images of (a) whole WL-eSiP, (b) solder joining area and (c) x-ray inspection image after assembly onto the substrate

After package level reliability test, assembly has been performed to evaluate board level Temperature cycle and drop shock tests. Figure 14 (a) shows cross-sectioned image of WL-eSiP surface-mounted onto the reliability test board and Figure 14 (b) shows solder joint interconnection between WL-eSiP and Board. Figure 14 (c) shows the result of x-ray inspection after assembly and there are no voids. Now, the samples are under evaluation for temperature cycle test (TCT) (-40/125°C) and drop shock test (1500G/ 0.5ms) on-board level.

Conclusions

In this study, wafer level embedded system in package (WL-sSiP) structure and process have been suggested, evaluated and verified for mobile applications. And to realize the suggested wafer level embedded SiP (WL-eSiP), structure and materials has been evaluated and successfully optimized in terms of device size, dielectric and molding compound materials for WL-sSiP through various reliability tests of MSL2, PCT, TCT and HTST.

With the results as above, fabrication process of WL-eSiP has been evaluated and developed. Then, reliability test vehicles have been fabricated from the results of structure, material and process optimization. Then, the quality of suggested WL-eSiP has been confirmed through package level reliability test of Moisture Sensitive Level of level 2a, Pressure Cooker Test (168hrs, 121°C/100%RH/2atm), High Temperature Storage Test (1000hrs, 150°C) and Temperature Cycle Test (500cycles, -40/125°C).

Board level reliability tests of temperature cycle test (-40/125°C) and drop shock test (1500G/ 0.5ms) are under evaluation and will be discussed in the following publication.

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