

Reliability Study of the Bump on Flexible Lead for Wafer Level Packaging

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Abstract

The Bump on Flexible Lead (BoFL) is a chip-to-substrate interconnect technology which uses flexible structures to accommodate the CTE mismatch between the chip and PCB substrate and therefore eliminates the need for underfill. The concept of the BoFL is based on wafer level packaging processing methods, such as photolithography, electroplating and wet-etching. The flexible lead consists of a copper redistribution layer embedded in a polyimide bridge which is located over an air gap. For the BoFL only 3 additional processing steps are necessary, compared to the conventional redistribution technology for wafer level chip size package (WL-CSP). Prototype chips (10 mm x 5 mm) with different lead shapes were fabricated and assembled on low cost FR-4 boards. The assembled chips were subjected to thermal cycling (-55°C/+125°C). A big influence of the shape and the orientation of the BoFL on the board-level reliability can be seen. The best results were obtained with the banana-shaped BoFL. Key words: Wafer Level Package, WLP, flexible, BoFL

I. Introduction

Chip Size Packages (CSPs) are widely used in portable electronic equipment like cellular phones, because of their smaller size and better applicability to high-frequency devices than traditional lead-type packages like thin small outline package (TSOP). Wafer Level Chip Size Packaging (WL-CSP), which simply extends the back-end of line (BEOL) in chip production, is a packaging process where the package is completed directly on the wafer. The current transition to 300 mm wafers forces the WL-CSP, as the cost decreases with larger wafer size. After dicing, the WL-CSPs can be mounted onto the printed circuit board (PCB) using standard surface mount assembly techniques. Further benefits of the WL-CSP are thinner package profile with considerable weight reduction. The sales of portable electronic devices have broken records for already many years, and sales volume is still expected to grow. This is leading to grow manufacturing volumes of the WL-CSP in market [1].

Since there is no underfill for most of WL-CSP assemblies the board level reliability becomes a critical issue. The principal scheme of global deformation due to cooling down the mounted component is shown in Figure 1. The thermal mismatch is converted directly into an elongation difference between the substrate and the chip. Therefore in WL-CSP the solder joints have to carry the entire load. As a result

outermost bumps undergo a severe shear strain [2]. This problem increases with increasing chip size. The reliability of WL-CSP with die lengths exceeding 5 mm dramatically decreases [3].

Therefore, several compliant interconnect technologies have been studied [4-9]. Recently the Bump on flexible Lead (BoFL) has been introduced [8-9]. In this work, the fabrication steps of the BoFL are described and the results of the thermal cycling testing are discussed in detail. A big influence of the shape and the orientation of the BoFL on the board-level reliability can be seen. The best results were obtained with the banana-shaped BoFL.

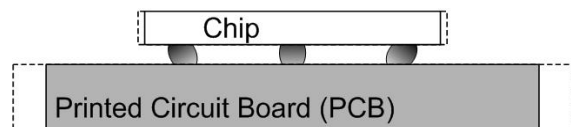


Figure 1: Principal FC deformation scheme for cooling down the whole assembly

II. Structure of the Bump on Flexible Lead

The concept of the BoFL is based on the redistribution technology of Fraunhofer IZM/ TU-Berlin [10]. For the BoFL only 3 additional processing steps are necessary, compared to the conventional redistribution technology for WL-CSP. To achieve a high flexibility in x-, y- and z-direction, and therefore avoiding excessive solder straining, the lead-free

bump is located on a flexible lead. The flexible lead consists of a copper redistribution layer (RDL) embedded in a polymer-bridge which is located over an air-gap (Fig. 2).

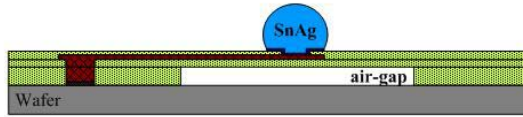


Figure 2: Bump on Flexible Lead (BoFL)

In PCB assemblies with conventional WLP, the solder joints have to accommodate the stress during thermal cycling. This leads to a repeated plastic deformation of the solder joint and finally results in fatigue damage. Since the flexible lead of the BoFL-WLP can take over the main part of the stress during thermal cycling, the risk of solder fatigue decreases and the reliability of the PCB assembly increases.

Table I: Specification of the test die and board

TEST DIE CHARACTERISTICS	
die size / die thickness	10 mm x 5 mm / 675 μm
maximum DNP	4.9 mm
number of bumps	54
bump pitch	0.7 mm / 0.95 mm
solder material	Sn3.5Ag
bump diameter	100 μm
bump height after board assembly	50 μm
TEST BOARD CHARACTERISTICS	
board material	high Tg FR-4
board thickness	1.5 mm
solder mask design	SMD
board pad opening	150 μm

The test chip and board characteristics are listed in Table I. The DRAM-type test chips have a size of 10 mm x 5 mm and 54 bumps with a minimum pitch of 0.7 mm. The maximum distance from neutral point (DNP) is 4.9 mm. The chips were mounted on a high Tg FR-4 board with a thickness of 1.5 mm. The solder material used in the process is electroplated Sn3.5Ag. The bump is 50 μm in height after assembly and the contact area on the chip pad is 100 μm in diameter. On the chip side, the bump is located on a polyimide bridge, with the embedded copper trace. The width and the thickness of the copper trace are 15 μm and 5 μm , respectively. The width and the thickness of the polyimide bridge are 100 μm and 25 μm , respectively.

Different BoFL shapes were fabricated. Figure 2 shows SEM pictures of all structures investigated within this study. Seven different BoFL shapes were investigated: a straight BoFL with a straight copper trace (Fig. 3a), a straight BoFL with an s-shaped copper trace (Fig. 3b), an s-shaped BoFL (Fig. 3c), a banana-shaped BoFL (Fig. 3d), a curl-shaped BoFL (Fig. 3e), an s-shaped BoFL with 3 polyimide arms (Fig. 3f) and an s-shaped BoFL with 4 polyimide arms (Fig. 3g).

Furthermore, two different orientations of the BoFL on the chip were investigated. The most test chips have an orientation of the BoFL parallel to the small chip side (Fig. 4a). Some test chips have an orientation of the BoFL along the direction of movement during the thermal cycling testing (Fig. 4b). The direction of movement of the outermost bump during thermal cycling is also depicted in Figure 4.

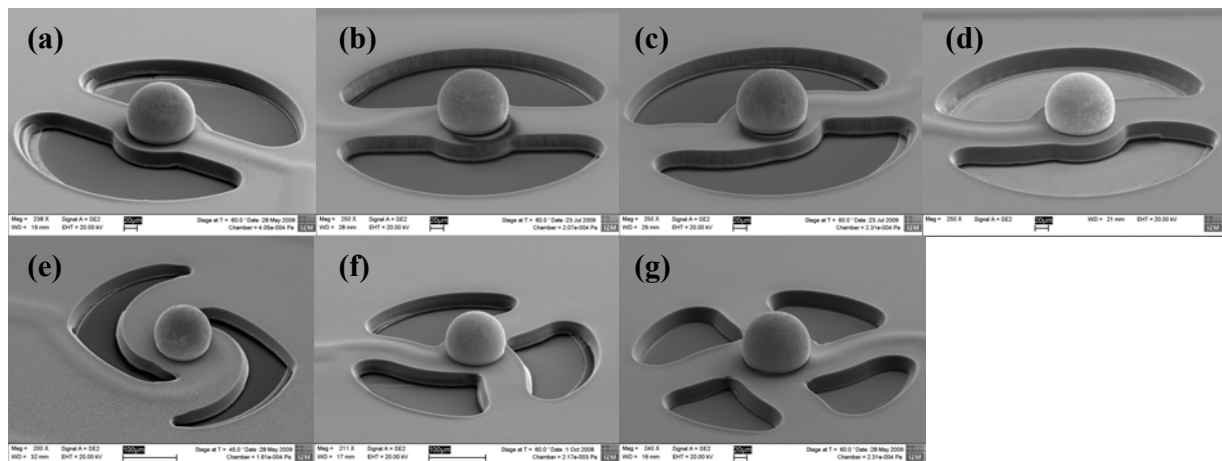


Figure 3: SEM pictures of different shapes of BoFL: (a) straight, (b) straight (cu s-shape), (c) s-shape, (d) banana, (e) curl, (f) s-shape (3 PI), (g) s-shape (4 PI)

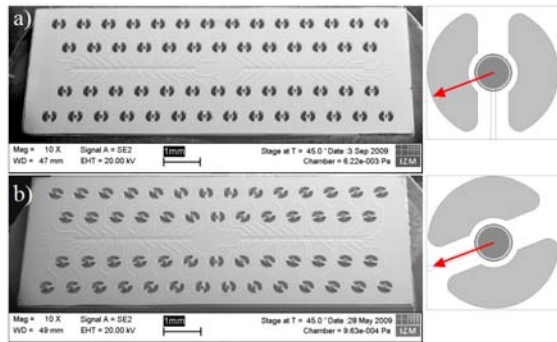


Figure 4: Test chips with different orientation of the BoFL: (a) parallel to the small chip side, (b) along the direction of movement during thermal cycling testing. The drawing depicts the direction of movement of the outermost bump.

Board level reliability AATC ($-55 / +125^{\circ}\text{C}$) was performed, following the JEDEC standard JESD 22-A104C test condition B. The cycle time was 30 min. A three chamber oven was used (10 min -55°C / 5 min $+25^{\circ}\text{C}$ / 10 min $+125^{\circ}\text{C}$ / 5 min $+25^{\circ}\text{C}$).

III. Fabrication

The concept of the BoFL is based on the redistribution technology of Fraunhofer IZM/ TU-Berlin [10]. In principle, WL-CSP provides a geometric translation from the chip scale elements of the device to the circuit board scale of the system. To relax the I/O pitch of front-end fabricated IC wafers, redistribution to an area array configuration is done. The first process step for redistribution is the deposition of a thin dielectric layer on the wafer to enhance the passivation of the die. Usually a photosensitive polymer is used, as e.g. polyimide (PI) or bencocyclobutene (BCB). For the rewiring electrochemical deposited copper is used, to achieve a low electrical resistivity. The copper metallization is then covered by a polymer passivation, which also serves as a solder mask. Finally the under bump metallization (UBM) and the bump is electroplated. Depending on the demands of the package different types of UBM and bump metallurgy are available [11]. In case of electroplated solder bumps, a final reflow is regularly done to homogenize the tin alloy and to form the spherical shape.

For the BoFL only 3 additional process steps are necessary, compared to the conventional redistribution technology for WL-CSP. A schematic sectional drawing of the process flow is shown in Fig. 5.

In contrast to the conventional redistribution technology, one starts with the electroplating of a copper sacrificial layer. In the same process step, copper studs are electroplated on the chip pads (Fig. 5a). A thin sputtered Ti:W/Cu layer serves as diffu-

sion barrier and plating base. Then, a thick polyimide (Du 7320) passivation layer is deposited onto the wafer by spin coating. To provide an access to the copper layer, the polyimide is planarized by chemical mechanical polishing (Fig. 5b).

At this point, the process of the conventional redistribution technology starts. This means, a photo-sensitive polyimide layer is deposited and patterned (Fig. 5c). Here the purpose of the deposited polyimide layer is to provide mechanical support for the bump, than to passivate the die. Polyimide (Du 7320) is used as the mechanical material since it can elongate significantly under thermo-mechanical stress, which is crucial for the flexibility of the structure. In the following step electroplating of the copper redistribution layer is done in the same way as the electroplating of the copper sacrificial layer (Fig. 5d).

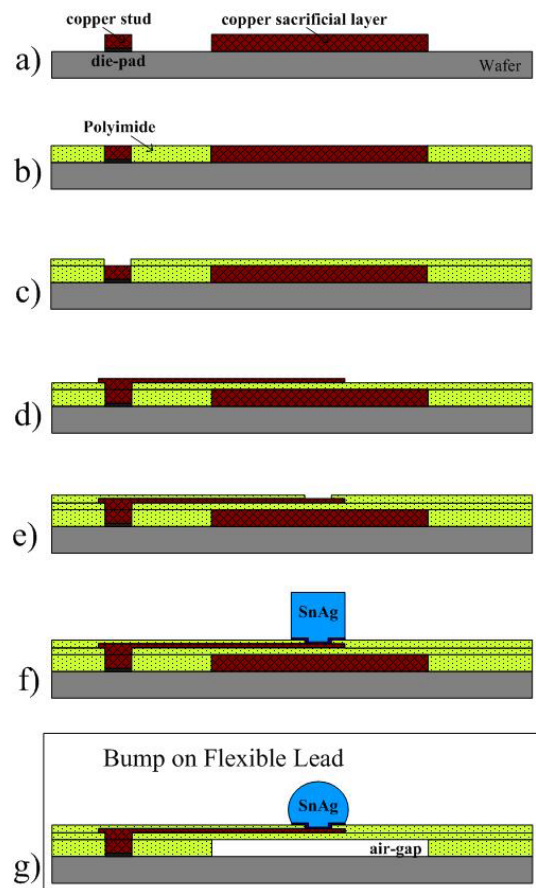


Figure 5: Process-flow of the BoFL

Then a polyimide soldermask layer is deposited and patterned (Fig. 5e). The next process step is the electroplating of the under bump metallization (UBM) and the SnAg solder bump (Fig. 5f). The UBM consists of a sputtered Ti (20 nm) adhesion

layer, and a sputtered Ni (300 nm) plating base. To obtain a reliable solder interconnect, about 5 μm nickel are electroplated [12, 13]. Figure 6 shows a cross section of a Bump on Flexible Lead after the electroplating of the SnAg bump. The copper sacrificial layer beneath the bump is clearly visible. Before the preparation of the cross-section, the sample was sputtered with thin gold. This was done to obtain a good visible boundary between the sample polyimide and the embedding material.

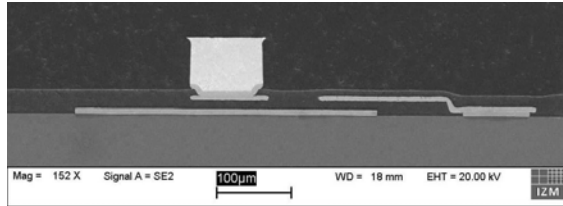


Figure 6: Cross-section before reflow and etching of the copper sacrificial layer beneath the bump

The last step of the redistribution technology is the solder reflow. For the BoFL an additional etching step is necessary to release the flexible leads. The copper sacrificial layer is wet etched for approximately 30 minutes in a copper chloride solution (Fig. 5g). Finally, the wafers are diced. During dicing the chips were protected with a photoresist.

Assembly of the test chips were done using a fineplacer with a split optic. The chips were dipped in flux (30 μm) prior to placing them onto the FR-4 board. Reflow was done in a convection oven with a peak-temperature of 262 $^{\circ}\text{C}$. Figure 7 shows a cross-section of an assembled chip.

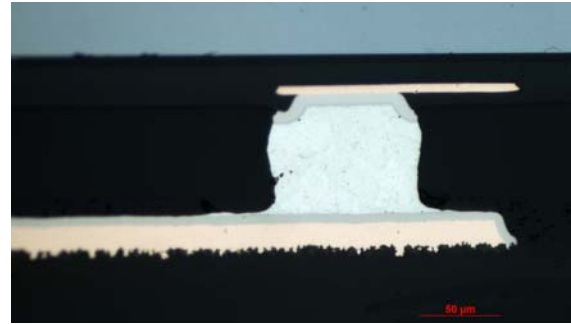


Figure 7: Microscopic picture of a BoFL WLP mounted on a PCB

IV. Results and Discussion

Of each design 4 chips were subjected to thermal cycling testing (AATC -55 $^{\circ}\text{C}$ / + 125 $^{\circ}\text{C}$). The assemblies were taken out of the test chamber every 50 cycles and the daisy chain resistance was measured. To be able to detect the location of a failed bump, the test chips contain several individual daisy chains, rather than one loop for all interconnects. An open circuit was determined as the criteria for failure. When all assemblies of the same board failed, the board was removed from the test chamber and the chips were then subjected to analyse by cross-sectioning. The results of the thermal cycling testing are listed in Table II.

The analysis by cross-sectioning showed, that the failure mode is solder cracking. The cracking occurred at the chip side. Solder bumps with the largest DNP failed first, as expected. No copper fatigue of the copper trace inside the polyimide bridge was observed.

Table II: Results of the thermal cycling testing (-55 $^{\circ}\text{C}$ / +125 $^{\circ}\text{C}$)

No. of cycles	Number of failed chips							
	straight (CTE)	s-shape (CTE)	s-shape (4-PI)	s-shape (3-PI)	curl-shape	straight	straight (Cu s-shape)	banana
0	0/4	0/4	0/4	0/4	0/4	0/4	0/4	0/4
50	4/4	4/4	4/4	1/4	0/4	0/4	0/4	0/4
100				3/4	2/4	1/4	0/4	0/4
150				4/4	4/4	2/4	3/4	0/4
200						2/4	4/4	0/4
250						4/4		0/4
300								0/4
350								0/4
400								2/4
550								4/4

Although the results are for a limited sample quantity, the experiments clearly show that the shape and the orientation of the BoFL strongly affect the reliability of the assembly. The best result could be obtained with the banana shaped BoFL. The first failure of the banana shaped BoFL occurred between 350-400 cycles.

The other test chip designs can be divided into two groups. Group 1 contains the test chip designs which have the worst performance, i.e. the test chips who failed before 50 cycles. These are the straight BoFL with an orientation along the direction of movement during the thermal cycling testing (Fig. 3b), further referred as straight BoFL (CTE), the s-shaped BoFL (CTE) (Fig. 3c) and the s-shaped BoFL with 4 polyimide arms (Fig. 3g), further referred as s-shaped BoFL (4-PI).

As depicted in Figure 1, the solder joints in WL-CSP undergo a severe shear strain by cooling down the mounted component. The PCB forces the solder joints to move toward the chip centre. The test chips of group 1 failed in a range as one would expect from WL-CSP without any compliant structure [14]. This indicates that the polyimide bridge is too stiff and impedes the in-plane movement of the bump.

Figure 8 shows a cross-sectional SEM image of an almost failed solder joint of an s-shaped BoFL (4-PI) after thermal cycling testing. The thickness of the polyimide bridge and the air-gap are about 25 μm and 5 μm , respectively. Thinner polyimide would increase the in-plane flexibility of the BoFL. On the picture one can further see the typical growth mechanism of the solder crack in SnAg. There are two cracks with the same length, one crack initiated at the outside of the solder joint and the other crack initiated at the inside of the solder joint [15].

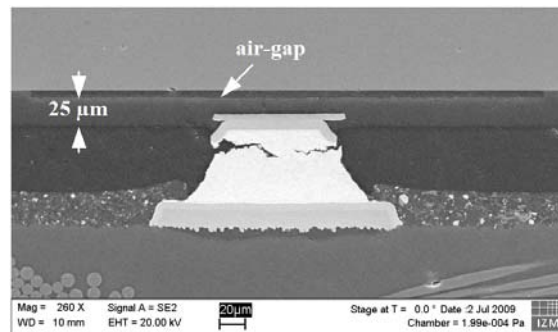


Figure 8: Cross section of BoFL after thermal cycling testing

In Figure 9, cross-sectional images of bumps along the outer-row of a straight BoFL (CTE) and an s-shaped BoFL (4-PI) are shown. Five solder joints per sample are shown, the left corner, the centre, the right corner and 1 solder joint each between centre and corner. The bumps of the straight BoFL (CTE) design (Fig. 3a) can move in the z-direction, which results in a tilting of the bumps toward the chip centre. The further away from the chip centre, the more pronounced is the tilting of the bump. After solder cracking, the bump relaxes and the tilting goes back.

The bumps of the s-shaped BoFL (4-PI) design (Fig 3g) cannot even tilt. The bumps are strongly fixed, due to the 4 polyimide legs. Nevertheless, tilting of the bumps alone cannot increase the reliability of the assembly. To increase the reliability, the in-plane flexibility of the bump is crucial.

Group 2 contains the test chip designs which have an intermediate performance, i.e. the test chips who failed between 50-250 cycles. These are the s-shaped BoFL (3-PI) (Fig. 3f), the curl-shaped BoFL (Fig. 3e), the straight BoFL (Fig. 3a) and the straight BoFL with an s-shaped cu-trace (Fig. 3b), further referred as straight BoFL (cu s-shape).

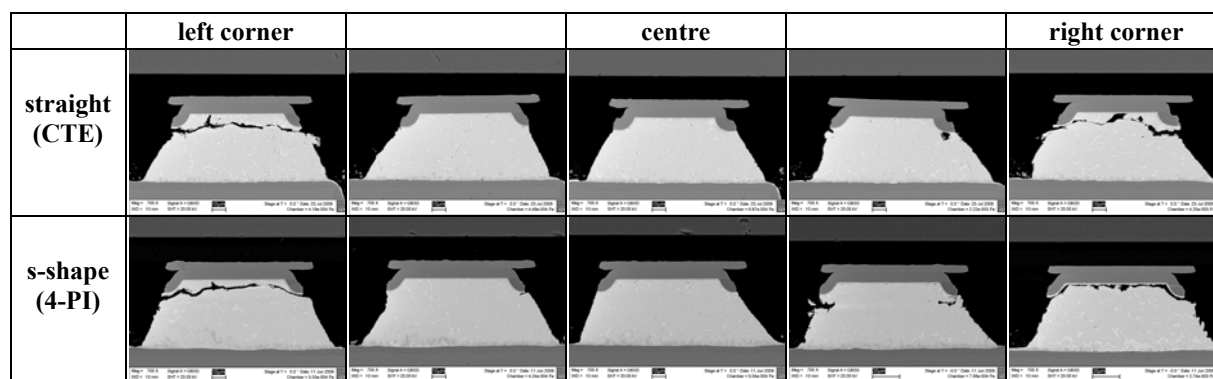


Figure 9: Cross sectional images of bumps along the outer-row

The reliability of these test chips is higher than the reliability of the test chips of group 1, since the in-plane flexibility is higher (Fig. 4). The limiting factor of the reliability is the shape and the orientation of the polyimide bridge and not the shape and the orientation of the copper trace inside the polyimide bridge, since all samples failed due to solder fatigue and not due to copper fatigue. Therefore, it is more favourable to use as less polyimide arms as possible (compare s-shaped BoFL (3-PI) and straight BoFL). There is no difference in the reliability of samples with the same PI design but different copper trace design (compare straight BoFL and straight BoFL (cu s-shape)).

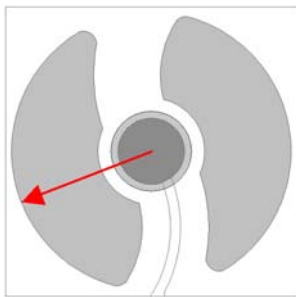


Figure 10: Direction of movement of the outermost bump of a banana shaped BoFL

The best result could be obtained with the banana shaped BoFL (Fig. 3d), since this design has the highest in-plane flexibility. The direction of movement of the outermost bump during thermal cycling is depicted in Figure 10. The first failure of the banana shaped BoFL occurred between 350-400 cycles, this is an increase in reliability by a factor of 8 compared to the reliability of group 1. New samples with thinner polyimide bridges (15 μm) were already fabricated and mounted on PCB. The reliability assessment is currently ongoing.

A design study by finite element analysis will be done to optimize the polyimide bridge regarding the flexibility. The polyimide bridge has to carry the entire load and therefore reducing the risk of solder fatigue. The new failure risks are mainly related to low cycle fatigue of the copper redistribution layer inside the polyimide bridge. Recently a study by finite element analysis investigated the plastic strain induced to the copper trace [9]. The induced plastic strain strongly depends on the direction and the shape of the BoFL. This means, further design optimization has to find a balance of metal straining and solder straining.

V. Conclusions

A WL-CSP with flexible interconnects, the Bump on Flexible Lead (BoFL), was introduced. The

fabrication process is based on the conventional redistribution technology of WL-CSP and therefore easy to implement. Test chips (10 x 5 mm²) with different BoFL shapes were assembled on PCB test boards without underfill. The solder standoff height was 50 μm . The board level reliability was investigated by thermal cycling (-55 / 125°C). The analysis by cross-sectioning showed, that the failure mode is solder cracking. No copper fatigue of the copper trace inside the polyimide bridge was observed. This in turn means that the limiting factor of the reliability is the flexibility of the polyimide bridge. Although the results are for a limited sample quantity, the experiments clearly show that the shape and the orientation of the polyimide bridge strongly affect the reliability of the assembly. The ability of bumps with a small standoff height to tilt is not enough to considerably enhance the reliability. The in-plane flexibility of the bump is crucial, to increase the reliability. To achieve this, the polyimide bridge should have an orientation perpendicular to the direction of movement. Further, the in-plane flexibility can be influenced with the shape of the polyimide bridge. The best results could be obtained with the banana shaped BoFL. The first failure of the banana shaped BoFL occurred between 350-400 cycles, which means an increase in reliability by a factor of 8 compared to conventional WL-CSP. It is expected to further increase the reliability by reducing the thickness of the polyimide bridge. Future work will include design optimization of the BoFL by finite element analysis and further reliability tests. Currently, reliability assessment of test chips with a thinner polyimide bridge is underway.

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