

Indium Thermal Interface Material Assembly Manufacturability and Reliability

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Abstract

Bonding silicon to an external copper lid with a solder requires extensive process development. This includes silicon metallization development, metallization of the lid cavity, extensive assembly process development to ensure good control in thermal interface material (TIM) bond line thickness (BLT), minimal voids at the interface, and the metallic bonding meeting all relevant reliability tests. Among many reliability tests performed to ensure product field life, high-temperature storage (HTS) test is critical. Therefore, a comprehensive HTS test was conducted to study its impact on thermal performance, inter-metallic compound (IMC) formation and growth, voids, and stability of BLT.

Two indium-TIM attachment methods were studied: pre-attached indium approach and indium pre-form approach. Pre-attach refers to pre-attaching indium-TIM on a lid cavity prior to assembling lid/indium with the microprocessor package. Indium pre-form refers to bonding indium pre-form to lid and silicon concurrently. HTS was conducted on thermal test vehicles (TTVs) built with indium to measure thermal resistance at each read point of HTS. Research found no significant change of thermal resistance up to 1,000 hrs of HTS at 125°C. C-SAM was used to monitor structural changes in indium such as void size. There is no significant change in voids after 1,000 hrs of HTS.

SEM and TEM were used to study IMC formation at each HTS read point. Two types of IMC were identified: AuIn_2 and $\text{In}_{27}\text{Ni}_{10}$. This research found that IMC thickness at the indium/silicon interface is very stable and does not increase with HTS time. However, significant IMC thickness increase is observed at the lid/indium interface. This observation can be explained by the nickel layer thickness used in the lid cavity and silicon backside. However, the increase of IMC at the lid/indium interface does not result in any thermal degradation or reliability degradation. This study concludes that indium-TIM is stable under HTS test.

Key words: thermal, indium, interface, assembly, manufacturability, reliability

Introduction

As microprocessor silicon technology advances, heat density increases. This poses a major challenge for conventional microprocessor packages with organic TIM to transport heat from the core of the microprocessor to an external heat sink. Therefore, solder-TIM -- in particular, indium-TIM, with much higher thermal conductivity than

organic-TIM -- is the solution for many high-power (and high power-density) microprocessors. Indium is chosen mainly because it meets thermo-mechanical requirements for microprocessor packages, has a relatively low melting point for assembly manufacturability, and is lead-free. At room temperature, indium is already at very high homologous temperature and does not work-harden. Re-crystallization happens readily, relieving most stresses that develop at the interface.

However, bonding silicon to an external copper lid with a solder requires extensive process development. This

includes silicon metallization development, metallization of the lid cavity, and extensive assembly process development to ensure good control in TIM BLT, minimal void at the interface, and that metallic bonding meets all relevant reliability tests. Among many reliability tests performed to ensure product field life, HTS is critical. Therefore, a comprehensive HTS test was conducted to study its impact on thermal performance, IMC formation and growth, voids, and stability of BLT.

Indium-TIM assembly process development

Gel-type TIM has been used on microprocessors for many years. It is typically consists of fillers with high thermal conductivity such as aluminum oxide, aluminum, or silver particles in a low thermal conductivity organic matrix. The thermal conductivity of the gel-type TIM therefore relies on the filler density and the degree of intimate contact between these filler particles. The effective thermal conductivity of gel-type TIM is a function of clamping pressure and BLT. Therefore, due to its relatively low thermal conductivity, gel-type TIM is only suitable for medium- and low-power microprocessors. Solder-TIM with much higher thermal conductivity is needed to meet the thermal design requirement for high-power microprocessors. After in-depth material selection process, pure indium was chosen as the preferred solder TIM. Indium has very unique physical properties: 157°C melting temperature, and malleable at room temperature (high homologous temperature). This means recovery and recrystallization occur as fast as work-hardening is induced. Mechanical failure of indium solder joint tends to be stress overload or creep. Creep in indium solder joint can usually occur sufficiently fast to ensure that stress is always close to zero, with roughly 80% stress relaxation occurring within seconds of step change in strain [1,2].

In a typical high-volume manufacturing (HVM) assembly process design, a metal boat (or carrier) is used to transport the microprocessor packages from one assembly process to another. Depends on the package size, a metal boat can typically carry from 10 to 40 packages. The microprocessor packages are loaded in the metal boat prior to all assembly processes.

Assembly process for gel-TIM is relatively simple. After microprocessor package goes through the standard wafer dicing, flip-chip re-flow, and underfill cure process, it is ready for gel-TIM lid attach. To meet HVM needs, Gel-TIM is formulated to have the right rheology (viscosity and thixotropy index) to ensure good manufacturability. The typical material deposition methods are needle dispensing or stencil printing. HVM needle-dispensing and stencil-printing equipment is commercially available from major assembly equipment manufacturers. After lid adhesive and gel-TIM deposition, lid attachment is carried out. Lid attachment is done with a proprietary designed assembly fixture. Significant effort was invested to develop a fixture that will ensure uniform clamping pressure and result in very good manufacturability and high product quality and reliability.

The lid adhesive and gel-TIM are then cured in an oven. Fig. 1 shows that typical process flow for gel-TIM assembly.

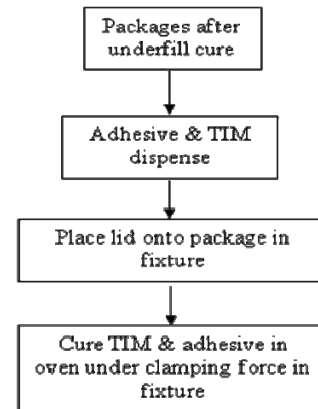


Fig. 1. Assembly process for a typical gel-type TIM.

Assembly process development for indium-TIM was very challenging. Leveraging the experience and know-how from gel-TIM assembly, a process development team was formed to develop a HVM assembly process for indium-TIM. We explored two assembly approaches: pre-attached and pre-formed. Pre-attach approach refers to attaching indium pre-form onto the lid cavity first, prior to attaching to the microprocessor package. The advantages of pre-attached indium to lid are that aggressive flux can be used since flux cleaning on lid is feasible. This also means lid with gold spot plating is not required. Aggressive flux is capable of removing oxide from nickel-plated lid cavity and indium can be successfully re-flowed on it. A subsequent flux cleaning process is required to remove the aggressive flux, which is highly corrosive. After flux cleaning, a layer of flux is applied to the indium dome. The re-flowed indium will form a dome in lid cavity due to surface tension. A coining step is required to flatten the dome-shape indium to ensure no lid tilt problem during assembly. After adhesive deposition on the microprocessor package, lid attachment is carried out. Similar to gel-TIM assembly, a proprietary lid attach fixture is used to ensure even and optimized clamping pressure. The lid adhesive is then cured in an oven. This is followed by a reflow process to form an indium solder joint. Fig. 2 shows a typical indium re-flow process flow (pre-attached approach).

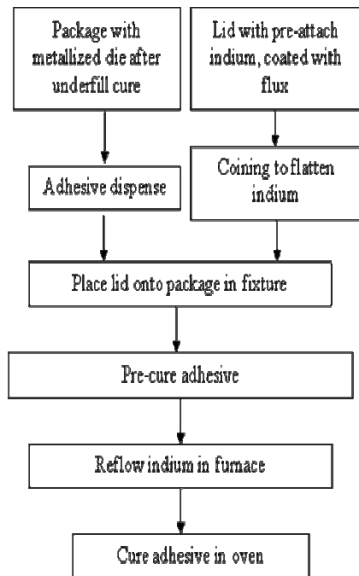


Fig. 2. Assembly process for indium-TIM (pre-attached approach).

In addition to the pre-attached approach, a pre-form indium-TIM assembly process was developed. In this assembly approach, adhesive is dispensed on underfilled package, then liquid flux is sprayed on the metallized die, followed by indium pre-form attach. Another layer of flux is sprayed on indium pre-form, followed by lid attachment. After curing of adhesive in oven, reflow of indium in a belt furnace forms the indium solder joint. Fig. 3 shows the typical indium process flow (pre-form approach). This assembly approach requires gold-plated lid cavity to ensure good wetting of indium to lid cavity since no-clean flux is used. It is not feasible to clean the lid-attached packages after indium re-flow. Therefore, aggressive flux cannot be used in this approach. Only no-clean flux that is not corrosive can be used. No-clean flux has relatively less oxide removal activity, so requires a lot more flux formulation and process optimization.

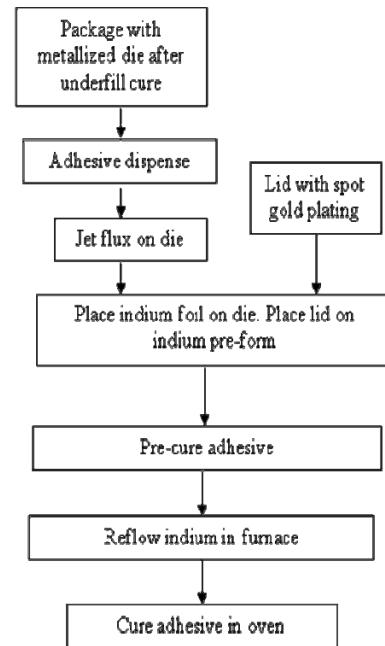


Fig. 3. Assembly process flow for indium-TIM (pre-form approach).

Reliability Tests

A major part of indium-TIM development involved package-level reliability testing. The goal was to develop an indium-TIM assembly process with good manufacturability (high process Cpk, low defect rate, high through-put, and low cost) and high product reliability (pass and exceed all required stress tests to ensure product field life).

A comprehensive set of reliability tests was carried out from the early stage of process development through product qualification. Power cycling, HTS, highly accelerated stress test (HAST) tests, mechanical shock test, and vibration test were among the key reliability tests.

With any solder joint, IMC formation at high operating temperature is a concern. Therefore, we carried out in-depth study on indium IMC formation and its effect on thermal resistance and solder joint integrity because of HTS. The HTS test was performed on both pre-attached approach and pre-form approach.

High-temperature storage test result

HTS was conducted on TTVs with indium in pre-attached and pre-form methods. The TTVs were subjected to 125°C for up to 1,000 hrs. CSAM was used to monitor the structural changes between the lid/indium interfaces at four intervals of 250 hrs each.

Both pre-attached and pre-formed TTVs showed no significant changes on the average voids sizes during the 1,000 hrs of HTS. As shown in Fig. 4, no significant difference in CSAM images before and after HTS was observed. Fig. 5 shows effect of HTS on void. On average,

only 0.07% and 0.18% growth in void sizes was observed in pre-attached and pre-formed TTVs, respectively, after 1,000 hrs of HTS.

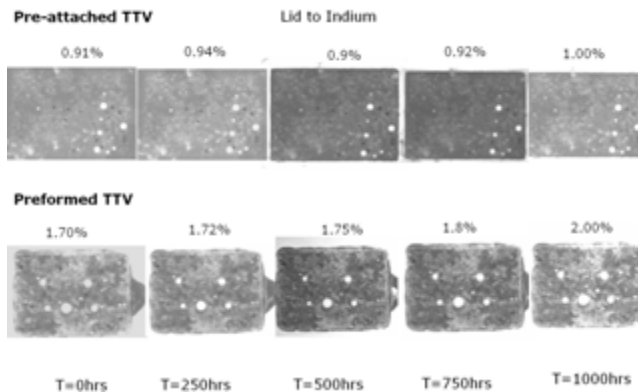


Fig. 4. CSAM images on pre-attached and pre-formed TTVs after HTS.

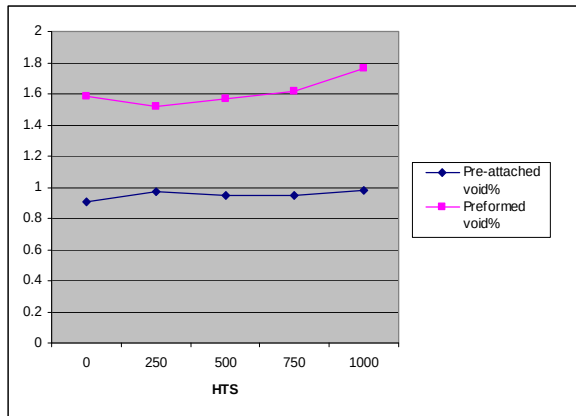


Fig. 5. Effect of HTS on indium void size (pre-attached and pre-formed).

Thermal resistance was measured at each read point of the HTS, and no significant changes of thermal resistance were observed during 1,000 hrs of HTS. Fig. 6 shows theta-JS after HTS. There is also no significant difference in thermal resistance between the pre-attached and pre-formed methods.

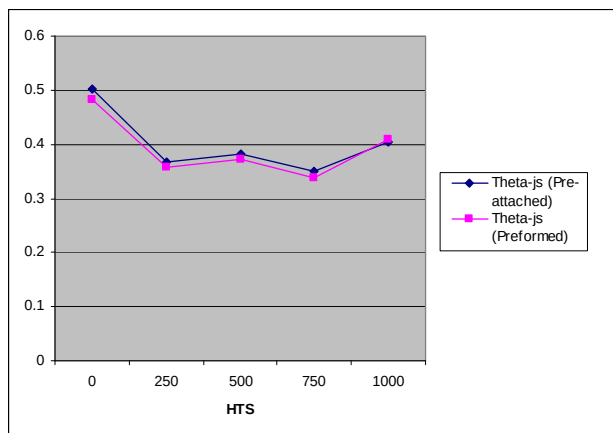


Fig. 6. Theta-JS vs. HTS on pre-attached and pre-formed TTVs.

IMC thickness on lid/indium interface grew from 0.46 μm to 4.75 μm on pre-attached TTVs after 1,000 hrs of HTS. As for pre-formed TTVs, the IMC thickness on lid/indium interface grew from 2.8 μm to 8.15 μm . The IMC growth on indium/silicon interface was slower. IMC on pre-attached TTVs grew from 0.34 μm to 2.11 μm , while IMC on pre-formed TTVs grew from 0.38 μm to 1.28 μm (see Fig. 7 for IMC thickness as a function of HTS). IMC on lid/indium interface grew significantly during the 1,000 hrs of HTS due to the thick layer of nickel on the lid cavity. The IMC on the indium/silicon was more stable because the nickel layer on the silicon was very thin.

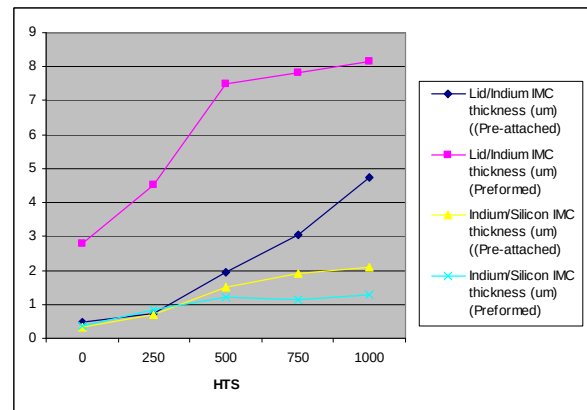


Fig. 7. IMC thickness after HTS.

IMC characterization on pre-formed indium-TIM

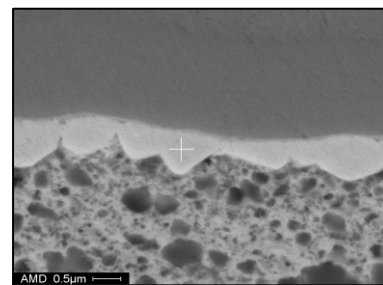


Fig. 8. SEM at lid/indium interface of pre-formed indium at time 0.

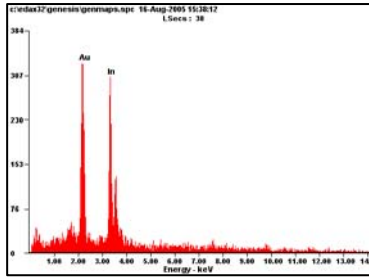


Fig. 9. EDX spectra corresponding to the white spot in Fig. 8.

It was shown in Fig. 5 that the scalloped morphology IMC was observed after re-flow. EDX with quantitative analysis has confirmed that this IMC was AuIn_2 , which agrees with the phase diagram. [3] The morphology of this AuIn_2 did not change with longer testing of HTS because the layer of Au deposited on the surface of lid has been fully reacted with indium to form IMC. However, indium reacted with Ni continuously to form $\text{In}_{27}\text{Ni}_{10}$ when the unit was under HTS testing. The IMC-forming mechanism has been described in [4,5,6]. Fig. 10 shows the thickness of IMC $\text{In}_{27}\text{Ni}_{10}$ increased with increasing HTS from 250 hrs (a) to 1,000 hrs (b). Some of AuIn_2 IMC during HTS 1,000 hrs dropped to indium side due to aging effect.

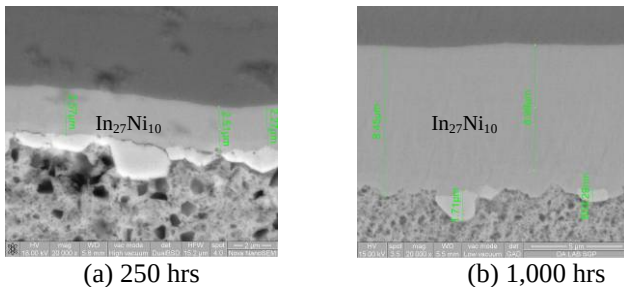
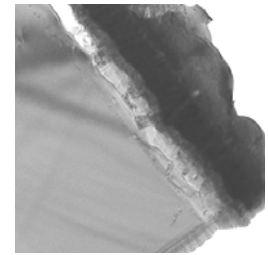
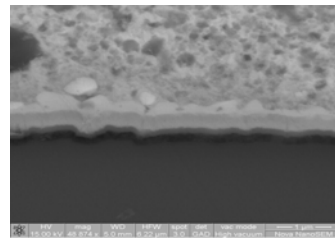


Fig. 10. SEM at lid/indium interface after 250 hrs (a) and 1,000 hrs (b) of HST, respectively.

Fig. 11 shows the SEM/TEM image on IMC between indium/BSM interface on the pre-formed indium unit. As the smaller feature of BSM film deposited on surface of silicon, TEM in combination of EDX has been used in this project to check IMC morphology. The results confirm that the IMC phase formed at indium/BSM is $\text{In}_{27}\text{Ni}_{10}$. It also can be seen there is no void formed in the interface of BSM as well as IMC with indium.

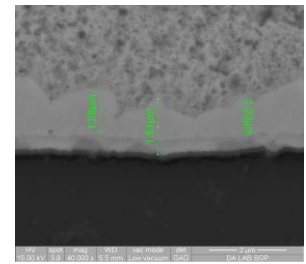
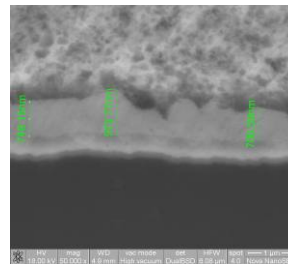


(a) SEM

(b) TEM

Fig. 11. SEM/TEM at indium/BSM interface of pre-formed indium at time 0.

As seen in Fig. 12, the IMC has become slightly thicker after increasing the HTS testing from 250 hrs (a) to 1,000 hrs (b). However, there is no IMC phase change during the testing.



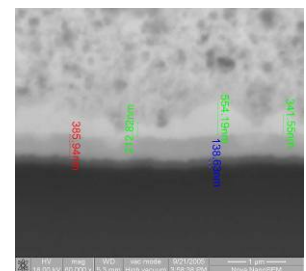
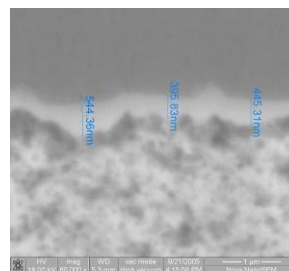
(a) 250 hrs

(b) 1,000 hrs

Fig. 12. SEM at indium/die interface after 250 hrs (a) and 1,000 hrs (b) of HST, respectively.

IMC characterization on pre-attached indium-TIM

Compared to the processing of pre-formed indium, there is no gold on the surface of lid before TIM re-flow. As such, only Ni/In IMC was observed at the interface of lid/indium, shown in Figs. 13 (a) and (b).

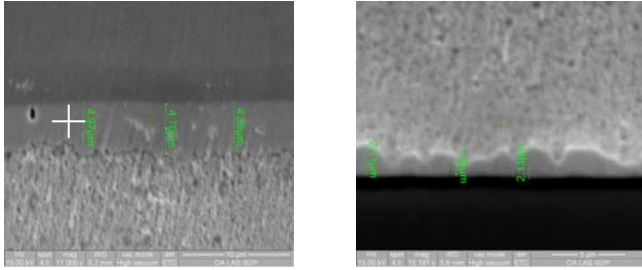


(a) Lid/indium

(b) Indium/die

Fig. 13. SEM at interface of pre-attached indium at time 0.

The Ni/indium IMC phase, shown in Figs. 14 (a) and (b), did not change when units were under HTS testing after 1,000 hrs on both interfaces. This result has been confirmed by EDX quantitative analysis (Fig. 15).



(a) Lid/indium

(b) Indium/die

Fig. 14. SEM at interface of pre-attached indium after HST 1,000 hrs.

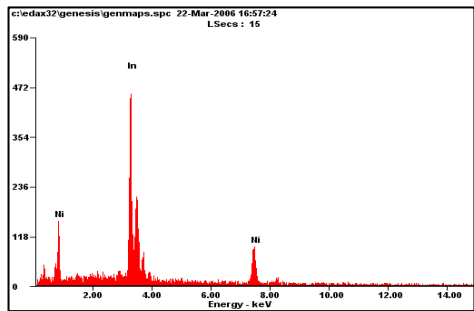


Fig. 15. EDX spectra corresponding to the white spot in Fig. 10(a).

Conclusion

After extensive assembly process development and reliability testing, we have successfully developed a high-yield indium-TIM manufacturing process for microprocessors. Indium-TIM is proven reliable based on all the reliability tests we performed. The test results show there is no thermal degradation or delamination after 1,000 hrs of HTS at 125°C. There is also no reliability risk from IMC study.

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