

Effects of Solder Voids on Thermal and Reliability Performances of PQFN Packages

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Abstract

Power Quad Flat No-lead (PQFN) packages are extensively used in automotive applications. Features such as solder die attach material, thick copper lead frame, exposed heat sink and heavy gauge aluminum wire, are adopted to ensure good thermal management and reliability performance. Solder voids, cavities formed between power die and lead frame during solder reflowing process, are major defects in die bonding process, and are detrimental to packages' thermal, mechanical and reliability performances. In this study, the effects of solder voids on the thermal performance of PQFN package are first evaluated by numerical simulation. The thermal response of the package is predicted for different void sizes and locations. The solder voids raise slightly the junction temperature of the package when the voids do not cover a major portion of the die attach area. Then, the effects of the solder voids on the package's reliability performance are assessed by carrying out two tests, Temperature Cycling (TC) and High Temperature Operating Life (HTOL), to the actual samples of different void sizes and locations. The electrical function inspection and Scanning Acoustic Microscope (SAM) inspection are performed to the samples at planned time points to find any electrical and mechanical failures. No functional failure or abnormal delamination has been observed throughout 500 cycles of the TC test and 408 hours of the HTOL test.

Key words: solder voids, junction temperature, reliability performance, PQFN package.

Introduction

The PQFN packages have been designed to meet high power dissipation requirements of automotive and other applications. A typical PQFN package has a control die and gold wires to execute electrical functions, a power die and aluminum wires to carry high current, and a lead frame substrate to perform IO connections and heat dissipation. Solder die attach material, thick copper lead frame, exposed heat sink and heavy gauge aluminum wire are adopted in the PQFN packages to ensure efficient heat transfer out of the packages and good reliability performance for the packages.

Solder voids, cavities formed between power die and lead frame during reflowing solder paste in reflow oven, are main defects within die bonding process. Formation of solder voids is complicated and involves solder paste composition, lead frame surface quality, die back metallization, bonding and reflow process [1, 2, 3]. Solder paste material and solder reflow process are considered as the top two factors influence the void formation [4, 5, 6, 7]. Studies of the mechanism of solder voids by Lee et al [4, 5, 6] showed that solder voids were generally

caused by outgassing of entrapped flux in solder paste and fluxing reactions during solder reflow process; the outgassing substances were mainly generated by the evaporation of solvent and other additives in solder paste and by the metallization of solder powder, substrate and component. Investigations of die bonding process by Yu et al showed an optimized solder reflow profile [8], forming gas atmosphere in reflow process [9] and controlled dispensed solder paste amount [10] reduced the solder void defects in actual PQFN package assembly.

Figure 1 shows typical solder voids in present study. It is noticed that the voids are through-holes and relatively evenly distributed across the die attach layer. The solder void size is defined as ratio of total area of all individual voids to the entire die attach area, in %.

A semiconductor package's thermal performance may be degraded by the solder voids. Biswal et al [11] evaluated the effects of solder voids on the peak temperature of a silicon die of a high power electronic module during transient operations by Finite Element (FE) simulation. They reported that maximum single void size and total void fraction

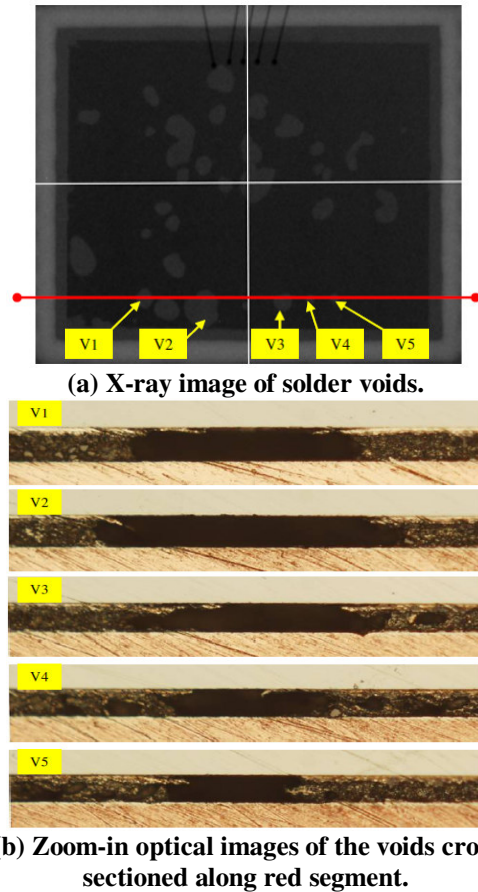


Figure 1 Typical configuration of solder voids.

caused profound temperature rise of the silicon die whereas the void distribution appeared to be a pretty weak contributor to the temperature rise. Fleischer et al [12] investigated the effects of void size, configuration and position on the thermal resistance of Chip Scale Packages (CSPs) by carefully controlling the void geometry and distribution in experiments and FE simulations. Their results showed that for small random voids, the thermal resistance R_{th} increased linearly with void volume percentage V according to relation $R_{th} = 0.007V + 1.4987$, and for large contiguous voids, the increase followed exponential relationship $R_{th} = 1.427e^{0.015V}$. Zhu [13] reported that large coalesced solder voids had more significant effects on the thermal impedance of power devices than small distributed solder voids.

Solder voids may also degrade a package's reliability performance. Yu et al [14] have found from experiments and FE analyses that solder voids in the solder joints of a CSP not only accelerated crack initiation but also decreased the solder joints' fatigue life. Yunus et al [15] observed from the torsion tests and air to air thermal cycling tests that big solder voids in BGA/CSP solder joints,

irrespective of the location, reduced the characteristic life of the packages, and multiple small voids might accelerate the package failure when they were near the chip side. Tummala et al [16] pointed out that peripheral voids, especially the voids at the corners of a die, might reduce a package's lifetime while the central voids normally did not impact its mismatch fatigue much. On the contrary, power packages were more sensitive to the central voids as heat accumulation might build up leading to premature failure of the die bonding.

In this study, the effects of solder voids on the thermal and reliability performance of a PQFN package have been investigated. The test vehicle is first introduced. The numerical simulation used to predict the junction temperature in the package is described and the predicted thermal response due to different void sizes and locations is presented and discussed. And finally, a description of actual reliability tests and the test results are presented regarding the reliability performance of the package.

Test Vehicle

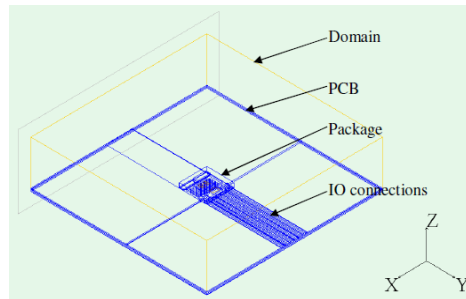
The test vehicle is a 12mm x 12mm x 2.1mm, 16 lead PQFN package. The package has 20mil thick copper lead frame substrate, a power die and a control die attached to the lead frame side by side by solder paste and epoxy respectively, gold wire and aluminum wire fulfilling the interconnections between dies and leads, and molding compound which encapsulates the dies and the interconnections. The power die is 5.43mm x 3.92mm x 0.25mm. The solder die attach layer is around 1mil thick and has high thermal conductivity. There are four 1.2mm x 0.8mm Field Effect Transistors (FETs) in the power die and each FET constantly dissipates 0.5W heat during operation.

In the numerical simulation, the model was created and the power loads were imposed based on the above package description, and the related boundary conditions were decided according to the package's actual applications. In the tests, the package samples were built following standard assembly process in internal PQFN production line. Assembled packages of normal electrical functions and different solder void sizes were chosen as the samples for the tests.

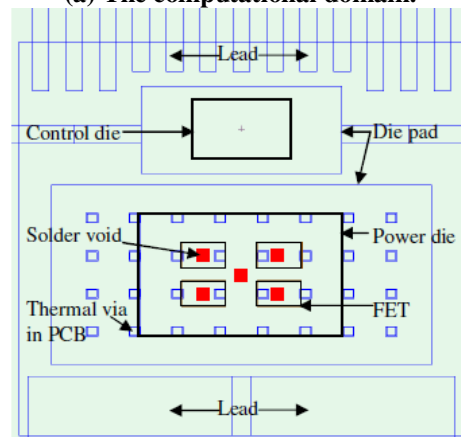
Effects of Solder Voids on Thermal Performance

The numerical simulation was performed by a commercial Computational Fluid Dynamics (CFD) software package, Flotherm [17]. The model was built according to the actual package geometry and configuration. The package was mounted on a 4-layer

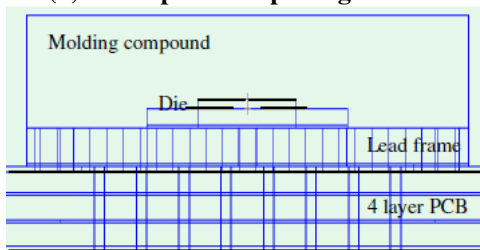
PCB incorporating a 4 x 8 thermal via array per JEDEC standard. Figure 2 shows the model and computation domain. The overall domain is 76mm x 76mm x 20.1mm.



(a) The computational domain.



(b) The top view of package model.



(c) The lateral view of package model.

Figure 2 The computational domain and model.

The related material properties in the computation are listed in Table 1. The boundary conditions were 85C isotherm on the back surface of PCB and natural convection heat transfer coefficients around the package ranging 5~15 W/m²K. A thorough grid independence study was conducted to identify a suitable grid for the computations, able to capture the physics of the model accurately yet not too expensive regarding the computation time. The final grids were 219 x 156 x 82 in x, y, z directions respectively. As the 4 FETs are uniformly powered at 0.5W each, the simulations were steady state computation.

Table 1 Material properties of the package.

Material	k (W/mK)
Copper lead frame	380
Silicon die	$117 - 0.42 \times (T - 85^\circ\text{C})$
Solder paste	50
Epoxy	0.3
Al wire	240
Molding compound	0.7

The solder voids were modeled as “solid vias” through the die attach layer. The voids were treated as air-filled cavities and the equivalent thermal conductivity of air (0.03 W/mK).

Considering the actual void distribution from test samples, the voids were modeled as 5 evenly distributed cavities in die attach layer, represented as red boxes in Figure 2(b). The total void size was defined as the total area of the 5 identical voids normalized by the die attach area. The total void size was increased by proportionally increasing the individual void dimension in all voids.

The void locations were on purpose arranged as one void right under an FET and the fifth one at the center. Although this generally is not the case in reality, the arrangement represents the worst situation of the voids regarding the heat transfer from the FETs, and this extreme situation should cover any other void distributions in practice.

Figure 3 shows the temperature contour in the package when total solder void size is 6.14%. It is seen that the highest junction temperature occurs in those FET regions, which is in accord with the physics. Taking the 85C as the reference temperature, the junction temperatures under different void sizes are shown in Figure 4. The thermal resistance was also calculated by formula $R_{th} = (T_{max} - 85)^\circ\text{C} / (4 \times 0.5) \text{ W}$ and were plotted in Figure 4.

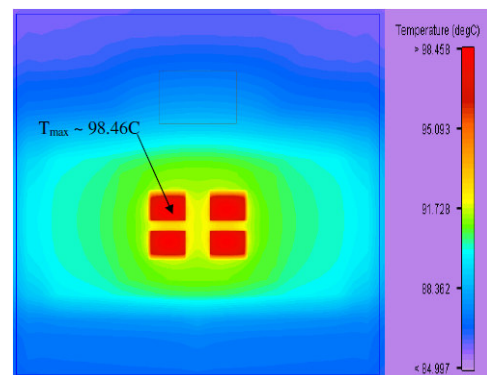
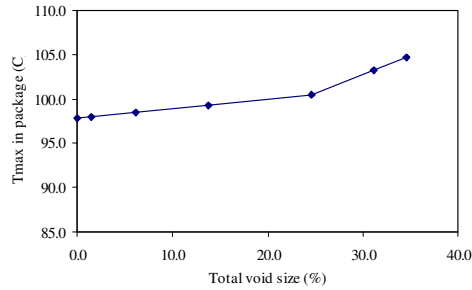
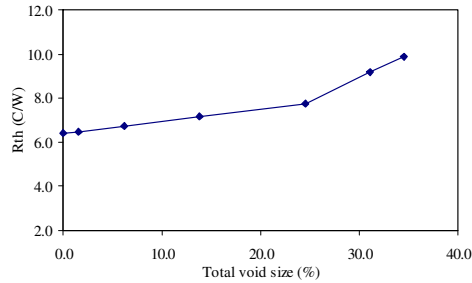


Figure 3 Temperature contour when total void size is 6.14%.



(a) Junction temperature.



(b) Thermal resistance.

Figure 4 Junction temperature and thermal resistance under different void sizes.

It is seen that although the highest junction temperature and thermal resistance increase as the total void size goes up, the increase is quite small. When the total void size reaches ~35%, the junction temperature increases to 104.74°C, which is still well below the 150°C limit for the silicon die in the package.

The reason that the junction temperature increases moderately when void size is quite large may be attributed to the fact that although the voids are large and placed directly underneath the heat sources, the highly thermally conductive solder die attach material can establish alternative paths for heat to escape and be conducted through the die attach; accordingly heat accumulation in die does not increase significantly.

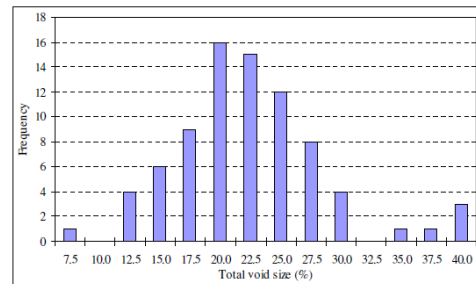
Effects of Solder Voids on Reliability Performance

Two tests, Temperature Cycling (TC) and High Temperature Operating Life (HTOL), have been carried out to investigate the effects of solder voids on the package's reliability performance.

The overall TC tests included Pre-Conditioning (PC) test and TC test. The PC test consisted of baking at 125°C for 24 hours, soaking at 30°C and 60%RH for 192 hours and convection reflow of 245°C peak temperature for 3 times. During a TC test cycle, the samples were dwelled in a chamber held -65°C for 10 min, then transferred into a second chamber held at +150°C and dwelled there for another 10 min, and one

cycle was 30 min long. This TC test accelerated the effects of thermal expansion mismatch among the different components within the package and accordingly might find mechanical problems related to the thermal mismatch, such as wire bond failure, delamination, die/package cracking which could be more easily triggered by the presence of solder voids.

A total of 80 samples went through the test procedures, first PC then TC. The void size varied from 7.0% to 39.3% and is summarized in Figure 5. Samples of large void size were on purpose included in the tested group so void effects can be easily observed.

**Figure 5 Histogram of void size of the samples in the TC test.**

The overall test ran up to 500 cycles of the TC test. All samples were inspected for electrical and mechanical failure at beginning of PC (time = 0), end of PC (time = PC), 200 cycles of TC test (time = 200 cycle) and end of TC test (time = 500 cycle). In electrical inspection, each sample was checked for electrical function at Room Temperature (RT) 25°C, High Temperature (HT) 125°C and Low Temperature (LT) -40°C. In mechanical inspection, each sample was checked for delamination by SAM. Electrical or mechanical failures were not accepted.

Table 2 summarizes the results of the electrical inspection. No electrical function failure was found.

Table 2 Summary of results of electrical inspection. Sample size = 80 units.

Check point	Time=0			Time=PC			Time=200cycle			Time=500cycle		
Check condition	RT	HT	LT	RT	HT	LT	RT	HT	LT	RT	HT	LT
Results	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass

While all samples were inspected for mechanical failure by SAM, the SAM results of 5 units, whose void size was 7.0%, 14.8%, 20.1%, 25.4%, 29.6% and 38.6%, are shown in Figure 6. The results are phase scan images. The Through scan image of the five units at time = 0 are also included in Figure 6. The voids are approximately the dark regions within the die attach area.

The red patches along package edge were the delaminations due to saw singulation process of package assembly and not related to the solder voids under power die. The weak delamination showed up around power and control dies from 200cycles of TC. They were due to the contaminations generated in solder and epoxy reflow process and were also observed in units of little and no voids. During the PC/TC tests, no delamination was observed within the power die attach area of the tested samples.

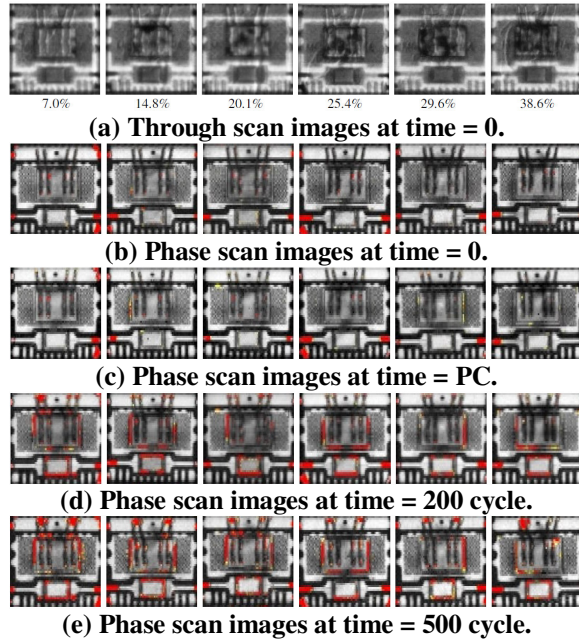


Figure 6 SAM results at planned time points.

The reason that large void size does not affect the package's reliability performance is attributed to the strong bonding force generated by the solder paste, softness of the solder paste and relatively even distribution of the solder voids across the die attach layer.

As the solder voids were considered to cause heat accumulation in power die, and the HTOL test accelerates failure mechanisms that are thermally activated through the application of extreme temperatures and the use of dynamic operating conditions, the HTOL test was also conducted to investigate the void's effects on the package's reliability performance.

A total of 44 samples were tested. The void size of the samples is summarized in Figure 7. Again, samples of large void size were on purpose included in the group so possible impact of solder voids on package's reliability performance was easily observed.

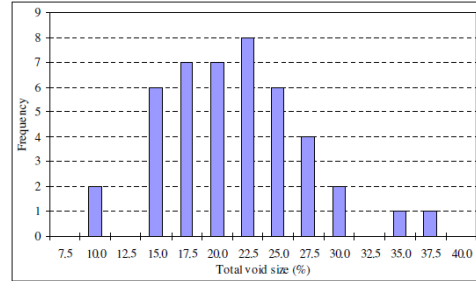


Figure 7 Histogram of samples for HTOL test.

During the test procedure, the 44 units were mounted in burn-in boards and the dynamic electrical signals to each unit were kept on and off for 408 hours in a chamber in which the ambient temperature was maintained at 150C.

Table 3 summarizes the results of the electrical inspection at planned time points, 0, 168 and 408hours. It is seen that all units passed the HTOL test and there were not any abnormal behavior observed during the electrical inspection.

This is attributed to the fact that the solder paste and copper lead frame can remove the heat from the power die efficiently even with the presence of large voids and therefore there is no large heat accumulation to impact package's electrical performance.

Table 3 Summary of results of electrical inspection. Sample size = 44 units.

Check point	Time=0			Time=168hour			Time=408hour		
Check condition	RT	HT	LT	RT	HT	LT	RT	HT	LT
Results	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass

Summary

The effects of solder voids on the thermal and reliability performances of a PQFN package have been investigated by numerical simulation and actual reliability tests.

The simulation shows that the presence of voids only slightly raises the junction temperature in the package and the temperature increase is well below the temperature limit in application. The TC and HTOL tests show that there is not unacceptable mechanical or electrical function failure observed throughout the tests.

The limited influence of the solder voids on the package's thermal and reliability performances may be attributed to the soft and thermally conductive die attach material; the copper lead frame and the strong bonding force created by the solder die attach material.

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