

Break Down Failure Process of the Flip Chip Bumps Caused by Current Stressing

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Abstract

Break down failure process by electromigration in flip chip bump connections under current stressing at certain temperatures was studied. The flip chip bumps used for these experiments consisted of Cu post formed with electroplating and SnAg_{3.0}Cu_{0.5} solder. Under bump metallurgy was electroless plated Ni(6um)/Au(0.5 um) on Cu pad. Electron flow to induce the electromigration was from organic substrate side (Cu pad) to chip side (Cu post) with current density of $4.0 \times 10^4 \text{ A/cm}^2$ at 165 °C. As a result of that, the failure process of the bumps under current stressing was found to be progressed in several stages. As the first stage, diffusion of Au was significantly occurred within a few hours. In the second stage, Cu₆Sn₅ intermetallic compound (IMC) formation was enhanced on the surface of the Cu post and the IMC was reached to the surface of the under bump metallurgy. In the third stage, this stage was frequently occurred at the same time of the second stage, Ni diffusion into Cu₆Sn₅ IMC and the formation of (Cu,Ni)₆Sn₅ IMC were simultaneously occurred. In the last stage, narrow gaps and voids were generated at the intra- and interfaces of (Cu,Ni)₆Sn₅ IMC.

Key words: electromigration, flip chip bump, intermetallic compound, failure process

1. Introduction

These days flip chip bump connection is essential way to connect Si chip and organic substrate with fine and dense bumps. Flip chip connection utilizing solder bumps in adequate alloy systems demonstrates several advantages over conventional wire bonding method. It is achievable for finer connection with superb placement accuracy by self alignment system during melting solders using conventional furnace in assembly facilities, higher I/O density, with better electrical performance. Increasing demand for high performance computation has the flip chip connection led to general standard process in chip connection which enables higher signal integration in interface connection. As the flip chip connection gets to move scale down in the pitch, current density at the bump connection gets to increase, which is expected to be in the order of 10^4 A/cm^2 [1, 2]. This current density is about two orders of magnitude smaller than the value caused to induce mass transportation in Cu and Al, but it is sufficiently critical order for the bump connection at device working temperature [3, 4].

As influenced by Europe Union RoHS

regulations, from the view point of environmental protection, lead-free solders has come into used. Tin (Sn) base solder has generally used for flip chip connection bump. Therefore, electromigration of lead-free solders, such as Sn-Ag-Cu (SAC), is the most serious and persistent reliability issues and received a lot of attention in the microelectronics industry [5, 6].

In this work, the failure process caused electromigration in the flip chip bumps was studied. The bumps consisted of Cu post at chip side, electroless Ni/Au on Cu pad at organic substrate side, and SnAg_{3.0}Cu_{0.5} (SAC305) solder ball had been prepared. Electron flowed from organic substrate side (Cu pad) to chip side (Cu post) with current density of 10^4 A/cm^2 at 165 °C. After the electromigration tests, cross-section area over the bumps was analyzed by scanning electron microscopy (SEM) and electron probe micro analyzer (EPMA).

2. Experimental

In this work, electromigration test were carried out according to the JEDEC standard JEP 154. A schematic diagram of the cross-section of the bump used for the electromigration test is shown in Fig. 1.

Cu post with 50 μm high and 100 μm diameter was fabricated by electroplating on the pad of Si chip. The surface finish of the Cu pad opening at organic substrate consists of electroless plated Ni and Au, 6 μm and 0.5 μm of thickness, respectively. SAC305 solder ball with diameter 75 μm was used to fabricate of the bump for connecting Si chip and organic substrate.

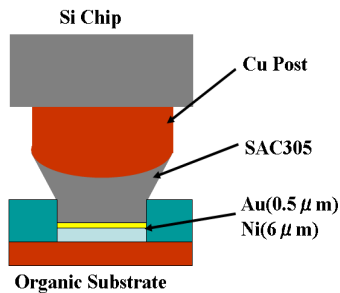


Fig. 1 Schematic diagram of the cross-section of the bump.

In order to excite failures of only one polarity of bump, multiple bumps providing current to the object bump were used. Schematic diagram of the unit of current supply structure to the object bump is shown in Fig. 2.

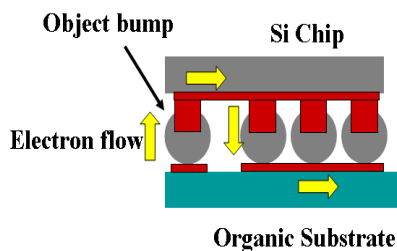


Fig. 2 Schematic diagram of the bump current supply structure unit. Yellow arrow means electron flow direction.

10 series of the unit shown in Fig. 2, in other words, a daisy chain of 10 object bumps was constructed in a sample. The sample prepared for electromigration test is shown in Fig. 3.

Si chip and organic substrate were connected by reflow process utilizing the SAC305 solder ball. Mechanical stress caused by the difference in the coefficient of thermal expansion between Si chip and organic substrate was presumed to exist. In order to inhibit the effect of such mechanical stress, underfill resin were introduced around the connection after the reflow process.

The samples were put into the socket to connect with outer leads electrically. During the current stressing, temperature of the object bumps increase caused by

Joule heating. In order to minimize the effect of Joule heating, aluminum fin was attached on the Si chip with thermal conductive paste. Joule heating emitted to ambient atmosphere through the fin with adequate thermal transition performance.

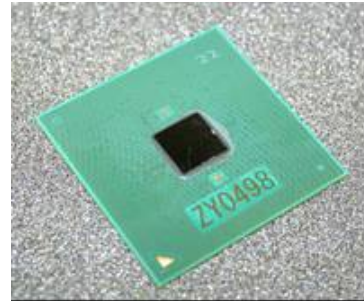


Fig. 3 Electromigration test sample.

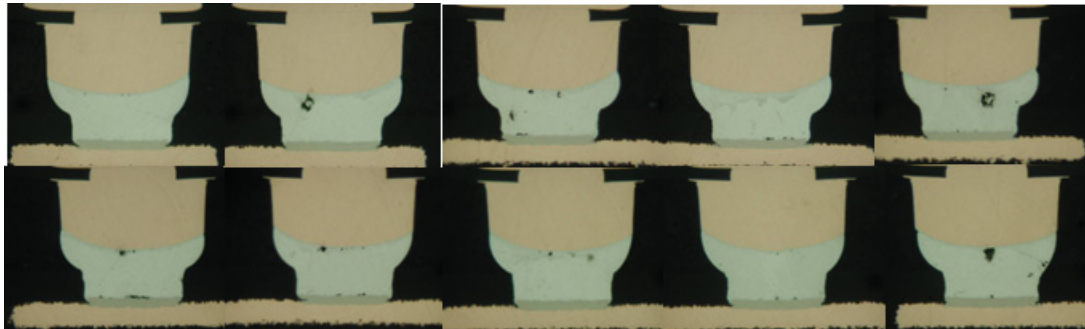
The electromigration tests were carried out in a oven kept at 165 $^{\circ}\text{C}$. Electron flow direction was from organic substrate side (Cu pad) to chip side (Cu post) with current density of $4.0 \times 10^4 \text{ A/cm}^2$. The current density was determined by smallest cross-section area of the bump, namely, the Cu pad solder mask defined diameter. The resistance of the daisy chain of the ten object bumps was monitored by automatically computing system. Four-terminal method was used for canceling the resistance of the organic substrate wiring.

As mentioned above, temperature increased by Joule heating is serious problem in electromigration tests [7]. In this work, the Si chip contained resistor circuit was chosen for construction of the samples. The temperature of sample was monitored by the chip resistor. This temperature monitoring method is superior to use thermocouple that was attached to the outside of the sample. Because temperature monitoring resistor is close to the object bumps, accurate temperature monitoring could be achieved. The effect of Joule heating by the current stress of the sample was confirmed in the range of 2 to 3 $^{\circ}\text{C}$ higher than the atmospheric temperature of 165 $^{\circ}\text{C}$ in this work.

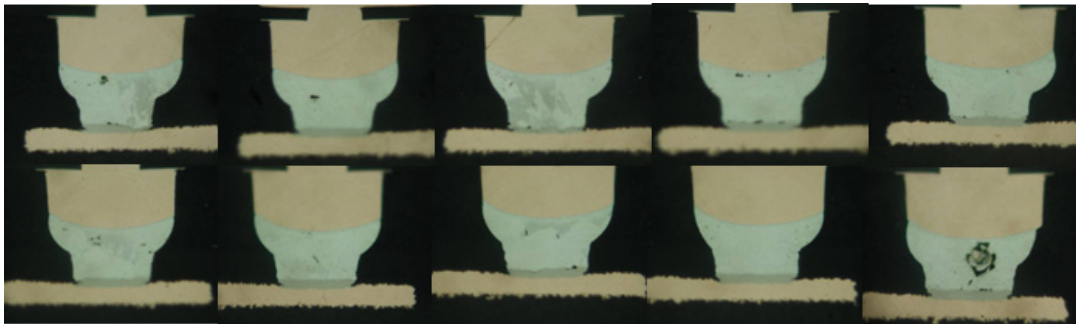
The electromigration test was carried out for appropriate times at above condition. To ensure the failure process of the bumps caused by electromigration, the change of microstructure and solder composition were investigated after the test. The object bumps were cross-sectioned and observed by optical microscope. After that, the bumps were treated with focused ion beam (FIB) and analyzed by SEM and EPMA. Energy dispersive X-ray fluorescence spectrometer (EDX) was also used to identify the composition of the IMCs.



(a) Current stressed bumps for 3 hours.



(b) Current stressed bumps for 6 hours.



(c) Current stressed bumps for 24 hours.

Fig. 4 The cross-sectional views of current stressed 10 object bumps in one sample on different current stressed time.

3. Result and discussion

3.1. Variety progress of IMC grown in solder bump

SAC alloys consist of approximately 97 atomic percent Sn. The micro bumps of SAC alloys were comprised of a few very large Sn grains and such Sn has a tetragonal crystal structure and highly anisotropic behaviors in physical properties [8, 9, 10]. A clear dependence of the thermomechanical response of SAC solder joints on microstructure and Sn grain orientation was reported by T. R. Bieler *et al.* [9]. It was also reported that the electromigration damage strongly depended on the Sn grain orientation from the results of wire sample

experiment by M. Lu *et al.* [10]. They concluded that one of the failure mechanisms was caused by faster diffusion of Cu and Ni through the Sn crystal along the c-axis compared to that of the a- or b-axis [10]. From the outstanding two reports above, profitable orientation of Sn grain is trade-off between thermomechanical view point and electromigration view point.

Fig. 4 shows the cross-sectional views of 10 object bumps in one sample by optical microscope. Fig. 4 (a) (b) (c) show current stressed bumps for 3, 6, 24 hours, respectively. The shadow in these solder bumps means the growth of IMCs that was confirmed by EPMA analysis latter. In this work, a daisy chain

of 10 object bumps was constructed in a sample. Therefore, these 10 object bumps were same structure except some void in solder and served to same condition electromigration test. In spite of that, the growth of IMCs progressed in some bumps much faster than that of in neighboring bumps in a same sample. As current stress time was longer, the number of IMCs grown bumps tended to increase and IMCs observed more clearly. At the non-current stressed bumps, those were neighboring of the object

bumps in a same sample, IMCs growth was not observed by optical microscope. Therefore, the growth of IMCs in the bumps caused current stress. It suggested that the variety progress of IMCs grown in solder bump observed in Fig. 4 was caused by the Sn grain orientation effect, that was pointed out by M. Lu *et. al.* from the results of wire sample experiment [10]. In the investigation of flip chip solder bump failure process by electromigration, the Sn grain orientation effect must be considered.

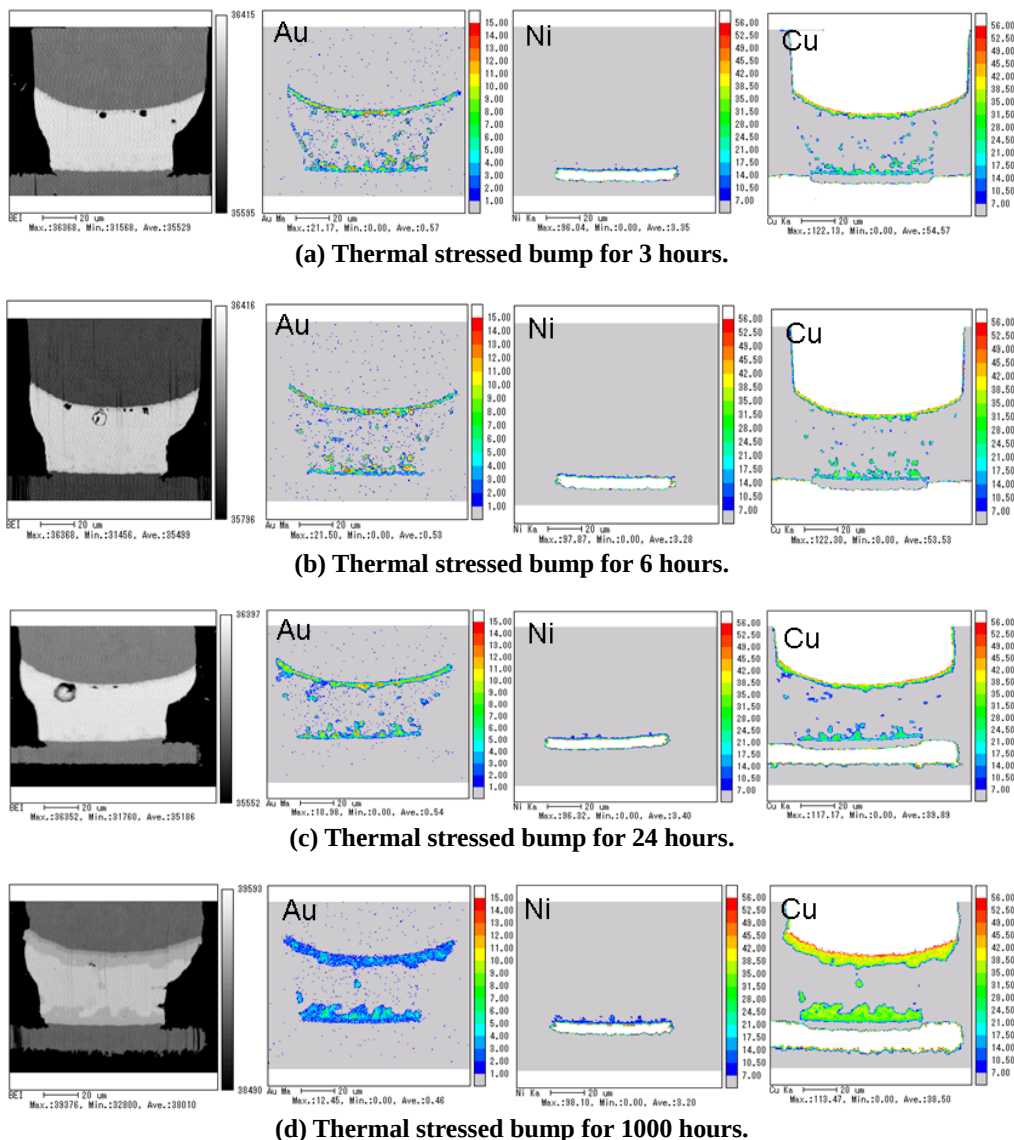


Fig. 5 SEM images and EPMA color maps of cross-sectional thermal stressed bumps.

3.2. The bump failure process by electromigration

3.2.1 The effect of thermal damage

In the electromigration test, solder bumps were damaged by current stress and thermal stress.

To distinguish the two damages, only thermal stress damage for the bumps was firstly investigated. Fig. 5 shows SEM images and EPMA color maps of cross-sectional thermal stressed bumps. Fig. 5 (a)-(d)

are non-current stressed bumps after electromigration tests for 3, 6, 24, 1000 hours, respectively. Each EPMA color maps are focused on Au, Ni and Cu elements, respectively and detected intensity are shown in side bar.

Fig. 5 and EPMA analysis of cross-sectional bumps of after reflow process suggested that Au, that was electroless plated on Ni, was diffused into the solder rapidly in the reflow process. After the diffusion into solder, Au was concentrated at IMCs phases that were grown at Cu post/solder and solder/Ni interfaces by continuous thermal stress. In the only thermal stress case, Au amount in the each site of IMC phases were approximately same. Ni that electroless plated on the Cu pad was very stable under thermal stress in this condition. Only small amount of Ni diffusion into the IMC was observed

with continuous thermal stress. Cu acted significant behavior as follows. SAC solder contains a small amount of Cu initially, and this Cu formed the IMC layer on the Ni surface at reflow process. At the same time, two kinds of IMCs were formed at Cu post/solder interface. Cu diffused from Cu post to solder, and IMCs at Cu post/solder interface and solder/Ni interface were grown by the continuous thermal stress of the test condition. IMCs at Cu post/solder interface were Cu_3Sn and Cu_6Sn_5 , therefore, the structure of the interface was consisting of Cu post / Cu_3Sn / Cu_6Sn_5 / solder. On the other hand, IMCs at solder/Ni interface was Cu_6Sn_5 and $(\text{Cu},\text{Ni})_6\text{Sn}_5$. The structure of the interface was consisting of solder / Cu_6Sn_5 / $(\text{Cu},\text{Ni})_6\text{Sn}_5$ /Ni. These IMCs were identified by EDX analysis.

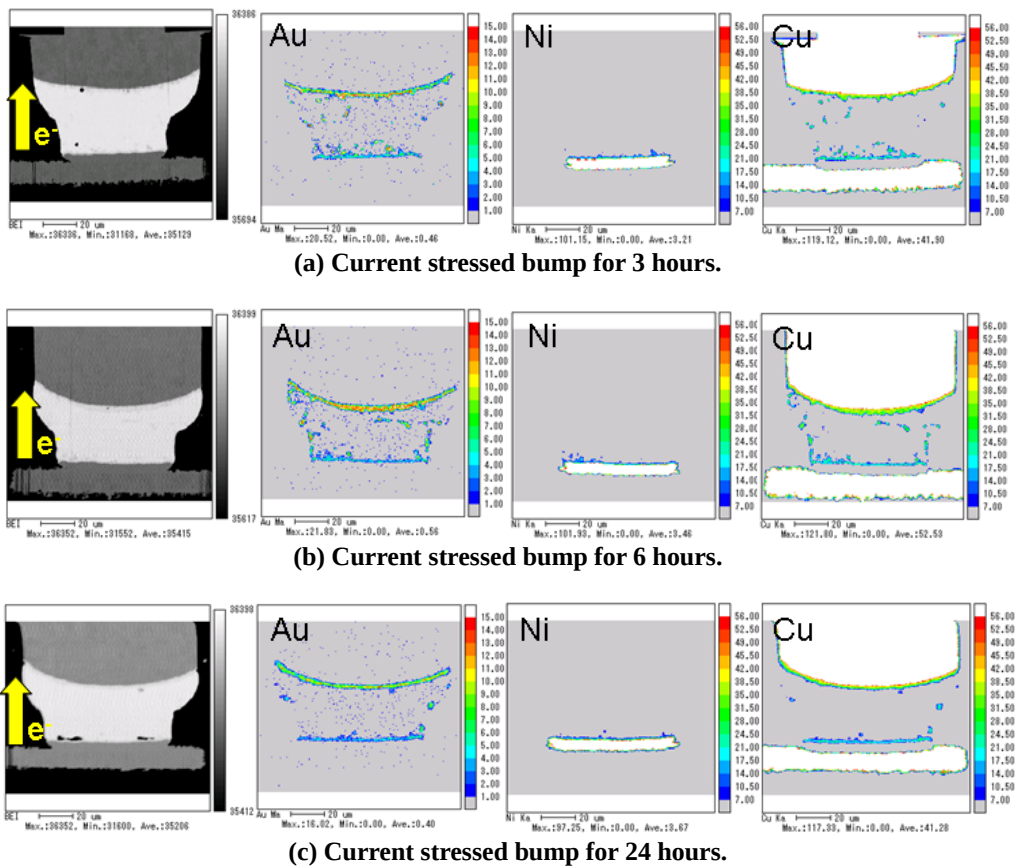


Fig. 6 SEM images and EPMA color maps of cross-sectional current stressed bumps for Au movement stage.

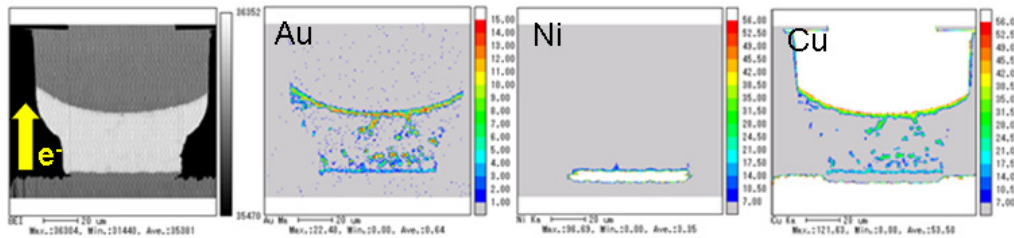
3.2.2 The first stage of bump failure process

It appeared that, Au is the first element moved in solder bump by current stress. Fig. 6 shows SEM images and EPMA color maps of cross-sectional electromigration tested bumps. Fig. 6

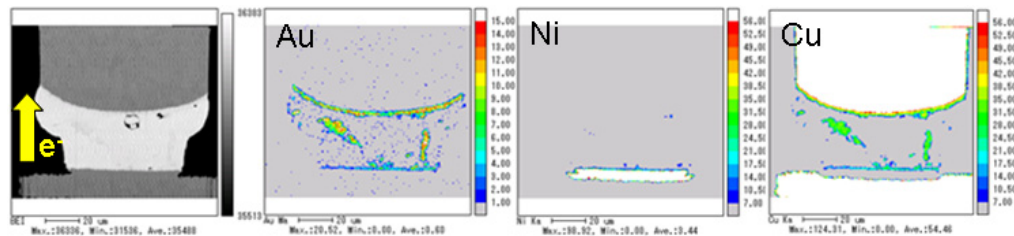
(a)-(c) are current stressed bumps after electromigration tests for 3, 6, 24 hours, respectively. EPMA color maps are focused on the same element as previous chapter. In SEM images, yellow arrows mean the direction of electron flow.

As mentioned above, Cu and Ni diffusivity were affected by Sn grain orientation. In spite of the same test sample, the IMCs in some bumps grew faster and the IMCs in other bumps grew little. To make sure the movement of Au, the bumps shown in Fig. 6 are chosen in condition of little growth of IMCs in solder, because Au tends to be concentrated and detected at IMCs in solder bump. Compared with

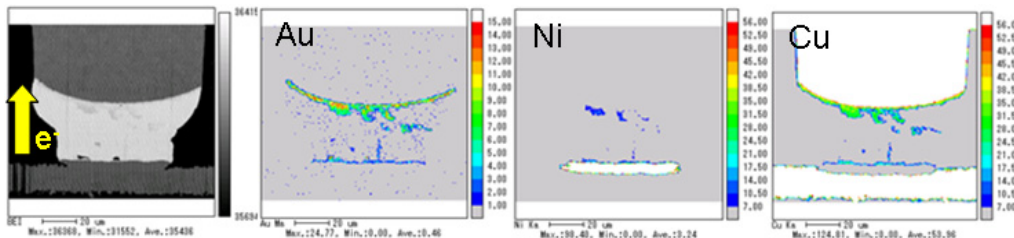
the EPMA color maps of Fig. 5 that was only a thermal stressed bump, Au was more concentrated to upper side IMCs in a few current stressing times as shown in Fig. 6. It suggests that Au was rapidly moved from Cu pad side to Cu post side in the solder bump by current stress, even though the distribution of Ni and Cu and their IMCs did not change remarkably.



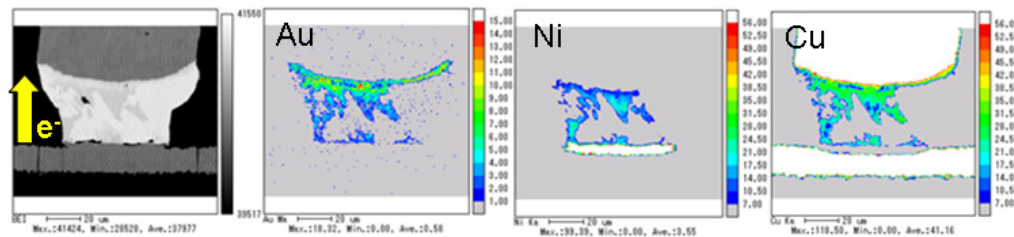
(a) Current stressed bump for 3 hours.



(b) Current stressed bump for 6 hours.



(c) Current stressed bump for 6 hours.



(d) Current stressed bump for 24 hours.

Fig. 7 SEM images and EPMA color maps of cross-sectional current stressed bumps for Cu, Ni diffusion stage.

3.2.3 The second and third stage of bump failure process

Cu and Ni diffusion into solder was started, after the movement of Au. Fig. 7 shows SEM images

and EPMA color maps of cross-sectional electromigration tested bumps at this stage. Fig. 7 (a)-(d) are current stressed bumps after electromigration tests for 3, 6, 6, 24 hours,

respectively. These bumps are chosen and shown based on progressive IMCs growth in each experimental condition, relatively. Fig. 7 (b) and (c) are same test time bumps taken from a same sample. Fig. 7 (b) is relatively analogous to (a) and Ni diffusion into solder is little observed. On the other hand, Fig. 7 (c) is relatively analogous to (d) and Ni diffusion into the solder is observed clearly.

From Fig. 7 and EDX analysis of IMCs, it appeared that Cu was diffused from Cu post to solder and Cu_6Sn_5 was formed and grown by the continuous current stress. This growth of Cu_6Sn_5 was faster than

that caused by the thermal stress and it reached to the surface of the under bump metallurgy. Such growth of the IMC at anode side by current stress was already reported [4]. At the same time or later, Ni diffused into the Cu_6Sn_5 and formed $(\text{Cu,Ni})_6\text{Sn}_5$.

It was observed by EPMA analysis that the formation of the IMCs in solder bumps was not uniform and not linearly-progress with the current stressed time, even in the same sample. That attributed to the difference of the diffusivity of Cu and Ni into the solder. Although, it appeared that the IMCs in solder bump were formed in this process.

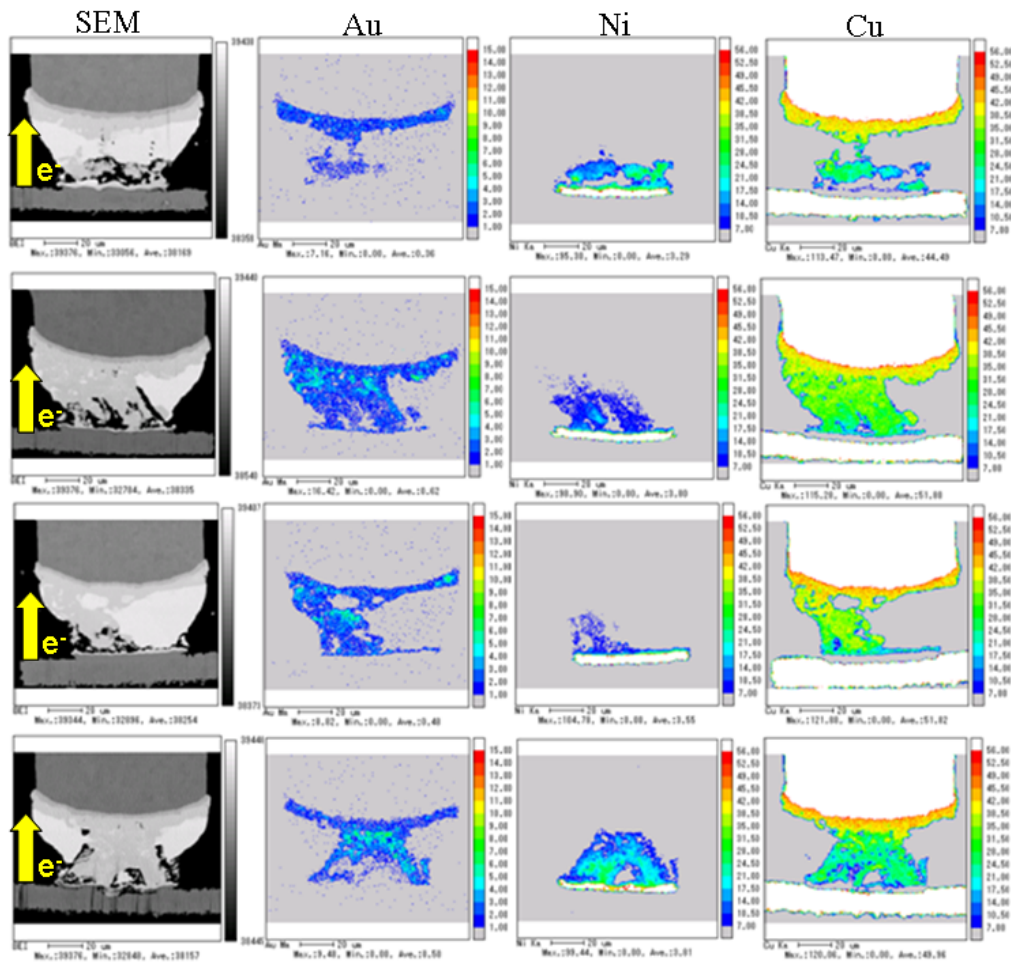


Fig. 8 SEM images and EPMA color maps of cross-sectional current stressed bumps for propagation of gaps and voids stage.

3.2.4 The last stage of bump failure process

After the growth of IMCs in the solder, it was frequently occurred at the same time, narrow gaps and voids were formed at the intra- and interfaces of $(\text{Cu,Ni})_6\text{Sn}_5$ IMC. Fig. 8 shows SEM images and EPMA color maps of cross-sectional

electromigration tested bumps for 1000 hours. In the EPMA color maps, Ni distribution area was including Cu distribution area. The IMC containing Cu and Ni was identified $(\text{Cu,Ni})_6\text{Sn}_5$ and only Cu distributed area was Cu_6Sn_5 . It was a result of the Ni diffusion into Cu_6Sn_5 . Cu_3Sn was also observed at the interface

of Cu post/solder. Au distribution in IMCs was also observed.

From the comparison of each SEM image and EPMA color map in Fig. 8, the locations of narrow gaps and voids in the bumps are roughly coincident with Ni distributional area. It was concluded that, therefore, the narrow gaps and voids occurred and grew at the intra- and interfaces of $(\text{Cu,Ni})_6\text{Sn}_5$ IMC in the bumps. There is a possibility that the growth of the gaps and voids in the bump was accelerated by a thermo-mechanical stress of temperature change after the end of the tests. But at least, it is clear that the electromigration is the cause of the gaps and voids. As a result of this failure process, the resistance of the bumps was increased by current stress.

4. Conclusion

The failure process of the flip chip bumps under current stressing was investigated. Flip chip bumps, in this work, consist of Cu post for chip side, electroless plated Ni/Au on Cu pad for organic substrate side, and $\text{SnAg}_{3.0}\text{Cu}_{0.5}$ solder (SAC305) ball. Electron flow direction was from organic substrate side (Cu pad) to chip side (Cu post) with current density of $4.0 \times 10^4 \text{ A/cm}^2$ at 165°C . From the analysis of tested bumps, the failure process of the flip chip bumps were concluded that:

- The failure process was not linearly-progress with the current stressed time even in the same sample. It suggested that the diffusions of Cu and Ni into the solder were effected by the Sn grain orientation of the bump.
- The failure process of the flip chip bumps under current stressing was found to be composed of several stages as below

First stage:

Movement of Au by current stress was significantly occurred within a few hours.

Second and third stage:

Cu diffused from Cu post into solder and Cu_6Sn_5 IMC was formed and grown by the continuous current stress.

Ni was diffused into the grown Cu_6Sn_5 and $(\text{Cu,Ni})_6\text{Sn}_5$ was formed.

Last stage:

The narrow gaps and voids yield at the intra- and interfaces of $(\text{Cu,Ni})_6\text{Sn}_5$ IMC and flip chip bumps.

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