

Advanced Lead-Free Server Hardware Reliability Test Methods: Power Age / Power Cycling and Four Point Bend Test Data Results

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Abstract

Reliability assessment of high complexity, high reliability lead-free Server class hardware continues to mature. OEM firms competing in Server and Storage market segments continue to contribute to the industry thermomechanical reliability database through their efforts to assess longer term reliability performance of their electronic hardware products.

Many firms, including IBM Corporation, continue to evaluate system reliability using a suite of accelerated environment tests to assess thermal fatigue, static / dynamic mechanical performance, and combination thermomechanical behavior. These tests typically include (but may not be limited to) accelerated thermal cycling, high temperature Storage, highly accelerated life testing, pull testing, drop testing, pad cratering assessments, and combination shock / vibration exposures.

This paper examines the results of two additional test methods explored to help identify reliability risk points within electrically functional lead-free hardware assemblies. Power Age / Power Cycling / Mini Cycling and Four Point Bend Testing are discussed, with summary results compiled from multiple lead-free Server class hardware product trials. The goal of this compilation assessment was to determine if these additional tests are indeed valuable, and if they can help to identify potential reliability hazards.

Through continued study, the capability of lead-free electronic card assembly and test is being systematically assessed for the extension of its applicability to high complexity, high reliability Server printed circuit board assemblies.

Key words: Lead-free Server, high complexity, high reliability, Power Age Power Cycle testing, four point bend testing, electronic card assembly and test

I. Introduction

With the latest European Union RoHS exemption review now complete [1] [2], many OEM firms building high complexity, high reliability electronic hardware are refining their technical and supply chain management strategies. Funding models and experimental test hardware programs are now being implemented to improve overall understanding of the risks associated with discontinuing various RoHS exemptions. These exemptions are currently in place to protect high performance, high complexity, high reliability applications where continued operation is critical. Several exemptions still in use today will likely not be supported after the upcoming 2012 review, thereby requiring this segment of electronic products to be designed and manufactured using new material sets and assembly processes.

Therefore, it is imperative that thorough reliability assessments be conducted for these high performance systems ahead of the next exemption review. Specifically, for electronic card assembly and test, it is critical that high reliability products currently invoking exemption 7b "Lead in Solder for Servers" exemption [3] continue to be tested and evaluated using lead-free soldering processes.

II. Background

Traditional methods of assessing thermomechanical reliability have been shown to yield acceptable results [4] [5] [6] [7] using a suite of tests. Thermal fatigue performance has typically been assessed using accelerated thermal cycling (ATC) and high temperature Storage (HTS) test methods. Mechanical fragility assessment has consisted of

combination shock, vibration, assembly process strain gauge monitoring, drop, and bend/torque testing. The aggregate results of these tests has been used to help determine reliability risk points and corrective actions at a functional system level for several low to medium complexity Server/Storage class hardware systems to date. In general, these tests have proven to be quite valuable in contributing to overall lead-free system level reliability performance assessment of this class of hardware. However, as can be expected, there have been several drawbacks noted with the suite of tests described above.

With respect to thermal fatigue resistance, ATC and HTS testing are accelerated tests which require acceleration factor (AF) calculations to properly link laboratory test results to actual field condition performance. Significant effort has been expended to date to determine new AF coefficients and model applications [8] [9] [10] [11] [12] suitable for lead-free assembly. Although progress continues in this area of study, a convergence of AF coefficients and predictive model validation using field hardware has not yet occurred; making high reliability field application warranty predictions high risk at this time.

In terms of mechanical fragility assessment of lead-free printed circuit board assemblies (PCBAs) it is well known that SnAgCu based solder alloys are much more brittle than eutectic SnPb alloys. Various tests can be conducted to evaluate sensitivity to this increased mechanical fragility during the PCBA assembly process (routing, compliant pin attachment, manual assembly, heat sink attachment, card merge, and in-circuit test) and/or final system assembly (node plugging, rack mounting, chassis harnessing, etc). The main challenge noted with mechanical fragility assessment is linking actual mechanical failure mechanisms during field operation to relevant laboratory testing methods. For example, drop testing assessment is much more important for mobile consumer electronics, while static/dynamic load assessments are more applicable to large Server/Storage type equipment. Determining appropriate mechanical test methods for field application is the main issue.

This paper discusses two reliability tests aimed at expanding reliability performance understanding of high reliability systems. First, Power Age / Power Cycling (PA/PC) along with Mini Cycling is discussed highlighting method development and test results. Secondly, Four Point Bend Testing is reviewed; again highlighting the test method used and results obtained to date. Most importantly, the work summarized here attempts to assess the value (benefits/drawbacks) of these advanced test protocols.

III. Objectives

The multiple objectives of this work are outlined below:

1. Expand thermomechanical reliability assessment and understanding of high complexity, high reliability electronic assemblies.
2. Examine two advanced reliability test protocols to evaluate lead-free PCBA system reliability performance.
3. Develop and evaluate a functional Power Age / Power Cycle test to monitor hardware thermal fatigue resistance during simulated system operation.
4. Evaluate a Four Point Bend testing protocol to characterize second level assembly hardware mechanical fragility.
5. Assess the value of each advanced reliability test: (i) Power Age / Power Cycling / Mini Cycling, and (ii) Four Point Bend Testing.

IV. Approach

A system level approach was taken when assessing the value of each test. Laboratory test results were to have a strong relation to *actual system performance in the field*. If conclusions could not be drawn from testing and related to field performance, then the assigned value of the test would be deemed low. If however, the test performance was a strong indicator of actual system performance then the test would be considered high value add. If significant value was identified, the test method could then be added to the standard suite of tests used for high reliability system assessment.

V. Power Age / Power Cycle Test Development

The method for this test was developed by IBM engineering with the intent to simulate actual product operating environments.

To perform the test an IBM Blade Server Chassis was utilized as shown in Figure 1, enabling flexibility to test a wide range of Blade Server configurations. In total, three different Blade Server types were tested during this assessment. The fully operational system consisted of a rack, chassis, fully loaded Blade Servers, all required mechanical hardware, hard drives, memory, and central processing units (CPUs) with the intent of drawing maximum thermal duties during operation.



Figure 1: Blade Chassis for Power Age / Power Cycle and Mini Cycle Simulation Tests

In Figure 2, a single Blade Server is shown, highlighting the complexity of each PCBA tested. As can be observed, each Blade Server was functionally complete with processors, full memory, hard drive, and full mechanical hardware.



Figure 2: Inside a Blade Server; fully functional hardware with CPUs, memory, and hard drive

Two different test conditions were defined and evaluated (a) Standard (or Quick Cycle) Power Age / Power Cycling and (b) Mini Cycling. Standard PA/PC settings were defined to simulate actual system operation including power-on, firmware load, complete memory and CPU checks, operating system boot, with full CPU loading. Mini Cycling on the other hand, was developed to simulate system operation with power save mode enabled [13].

System temperature was controlled with left and right fan modules located at the back of the chassis, drawing air from front to back of the unit. Fan speeds were controlled to simulate maximum temperatures required in actual field operating environments as measured at critical components, CPUs, voltage regulators, heat sink interfaces, etc. as well as ambient system locations.

A. Operating Environment Simulation

The Blade Server used in this study integrated an automatic shut off safety feature if CPU temperatures exceeded 94C (201F). Actual system testing was therefore set nominally near 90C (194F) as measured at the CPU locations to simulate maximum thermal duties.

System operation simulation was achieved using a combination of data exercisers and program control scripts. Together this custom designed software allowed the system to power on, run specified system read/write operations, and power the system down. In general, the following process constituted a single power cycle:

1. System power-on
2. Automated timing file load which controlled:
 - a. Cyclic power on / off
 - b. Data exercisers (read/write)
 - c. Thermal measurements of system
 - d. Hourly macro data file output

B. Test Conditions & Pass / Fail Criteria

A standard (single) power cycle was characterized by the following elements:

- Blade type tested / configuration used
- System power-on
- Firmware loading
- Memory and CPU checks
- Operating system loading
- Inclusion of a hot dwell at maximum temperature
- Data software exerciser run time
- Thermal data collection macro run time

Table 1 shows the various test condition options that were developed based on the times taken to complete steady state operation temperatures from the listing above.

	Test Condition	Test Duration (cycles)
Standard PA/PC	40min power on / 20min power off	2,500
Quick Cycle PA/PC	20min power on / 10min power off	2,500
Mini Cycle (Power Save)	10min power on / 10min power save mode	20,000

Table 1: PA/PC and Mini Cycle Test Parameters

Power-on of the system ensured maximum CPU and memory usage. Test duration limits were determined based on system warranty requirements. Although this test was able to simulate real operating thermal gradients, it was *not* however, designed to

simulate frequency and isothermal dwell effects as observed during actual product field use.

C. System Thermal Profiling

In order to assure maximum operating temperatures and control necessary fan speeds, detailed thermal profiling was conducted. Various Blade configurations tested had very different boot and steady state times, therefore driving the need to carefully profile each card type during system operation. Figure 3 shows Blade slot five as it is being profiled within the system.

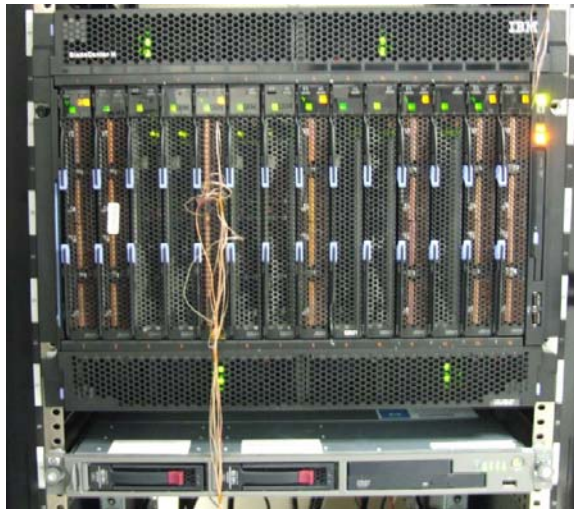


Figure 3: Blade profiling during system operation

Profiling included 16 thermocouples per Blade slot, repeated within multiple slots to monitor temperature gradients across the 14 bay chassis. Various locations were monitored including CPUs, ambient system temperatures, heat sinks, and various other key locations of interest. Profiling verification measured four consecutive cycles. An example of a Standard PA/PC cycle used is shown in Figure 4.

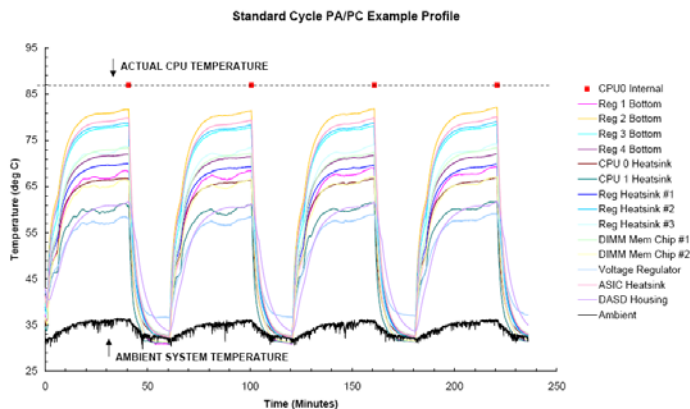


Figure 4: Standard Cycle PA/PC Example Profile

The resultant PA/PC thermal cycle temperature range (ΔT) was found to be approximately 65C (25C nominal ambient room temperature to just below 90C); as measured at the hottest location near the CPU devices.

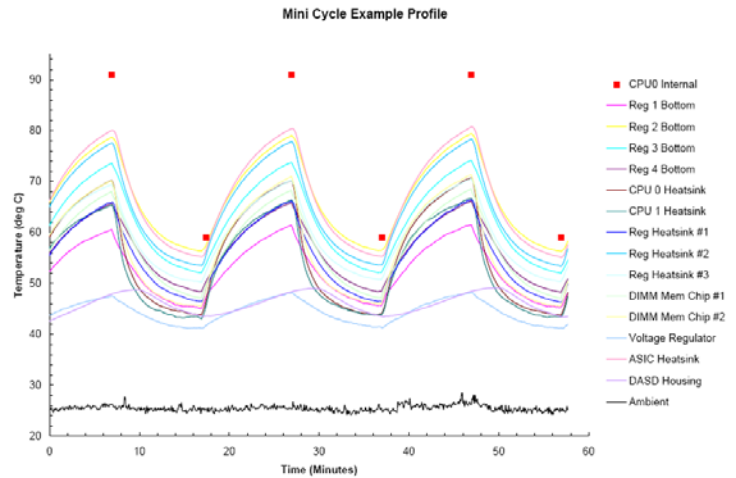


Figure 5: Mini Cycle example profile

For Mini Cycle profiling the same method was employed as described for PA/PC verification. The resultant Mini Cycle thermal cycle ΔT was found to be approximately 35C (55C to just below 90C); as measured at the hottest location near the CPU devices (Figure 5).

D. Exercisers, Controllers, and Data Collection

The key element responsible for the successful implementation of PA/PC and Mini Cycle testing was the software design / implementation of various data exercisers, system controllers, and data collection macros needed to simulate actual system operation.

Data exercisers were utilized to continually perform various read/write functions of looped data sets with computations. They were programmed to achieve maximum CPU and memory utilization, thus generating maximum thermal output of the system. While exercisers computed, stored, or accessed data, they did not control power on / off of the system. Separate script software was written to control power on / off and also to record resultant temperature measurements of the system.

E. Failure Detection

Power and Mini Cycling were designed to run until a system event was detected. System level events were determined during the system boot process. If an issue had occurred during the last cycle, the system would not properly boot and subsequent error codes would be generated. Evaluation of these error codes helped identify the location of the issue

within the hardware. Physical analysis was then conducted to determine root cause of identified events.

VI. Power Age / Power Cycle Results

A. Power Age / Power Cycling

Resultant thermal data was collected hourly recording CPU (hottest locations) and ambient system temperatures once the test was started, although not all locations were monitored (as described within the thermal profiling section above). An example output plot is shown in Figure 6. An issue was observed at 1,340 cycles. System boot problems and subsequent error code evaluation led to root cause issue understanding. In this case, the issue was resolved and Blade testing was restarted. As can be observed, a second issue was observed at 2,498 cycles. Again, error code evaluation helped determine the root cause of each event.

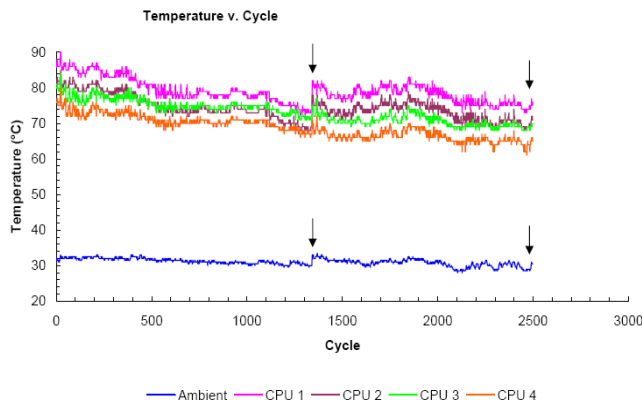


Figure 6: PA/PC Temperature vs. Issue Points

Electrical issues created system boot errors indicating that indeed an event had occurred. This indicates that the test can help with improved event detection accuracy at a system level.

B. Mini Cycling

Similar thermal output (Figure 6) was generated during Mini Cycle testing. At the time of publication, there was no system events observed after 16,000 Mini Cycles with testing still in progress.

VII. Four Point Bend Test Development

A four point bend method and apparatus was adapted from earlier works and standards [14] [15] with the intent to measure first failure points within various BGA package constructions at corresponding strain levels and displacements.

For this test case, multiple qualification programs, card complexity levels, and BGA package types were evaluated over a two year period. The

intent was to examine multiple data sets in an aggregate view, looking for trends and/or any specific linkages to reliability performance at a system level. A summary of the range of data collected for evaluation of this test protocol is shown below:

- 7 PCBA assemblies (of varying complexity)
- PCB thickness ranged from 0.062 to 0.087 in.
- 5 PCB laminate materials
- 3 surface finishes: OSP, ImmAg, and LF HASL
- 10 BGA packages ranging from 20 to 42.5mm²
- Primary attach vs. rework processes

Figure 7 shows the apparatus with test specimen under load. Depending upon the space constraints of each test card:

- load spans generally ranged from 30 - 40mm
- support spans ranged from 70 - 80mm
- displacement speed was set to 0.25mm/second
- maximum displacement ranged from 15 - 20mm

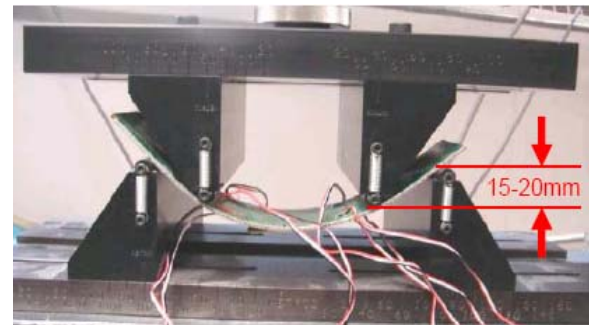


Figure 7: Four Point Bend Displacement

Each BGA test location was monitored with eight uni-axis strain gauges aligned to measure maximum bending strain. Four were located at each corner top side, and four were mounted at each corner bottom side as shown in Figure 8.



Figure 8: Uni-Axis Strain Gauge Locations

Resultant strain data were recorded for each of the eight monitored channels using a high speed data recorder measuring 1,000 readings per second. Board deflection was increased until first failure was detected on one of the eight channels. A first failure

plot example is shown in Figure 9. Top and bottom strain levels were recorded with corresponding compressive load values. As can be observed, both top and bottom strain gauge channels picked up the break fracture near 10mm of z-axis card displacement; corresponding PCB resultant micro strain and loads were recorded.



Figure 9: First Fracture Response

Measurements such as those shown in Figure 9 were conducted on a variety of card constructions as described above. First failure maximum strain levels were recorded and subsequent failure analysis conducted to verify root cause of each detected failure.

VIII. Four Point Bend Test Results

Topside strain failures ranged from 1,055 to 8,598 $\mu\epsilon$ with an average of 3,952 $\mu\epsilon$, while bottom side failures ranged from -1,615 to -8,421 $\mu\epsilon$ with an average of -4,314 $\mu\epsilon$. Standard deviation for both measurement populations were very high (2,202 $\mu\epsilon$ top and 2,089 $\mu\epsilon$ bottom) with coefficients of variation 56% and 48% respectively. Statistical review of the data indicates that there was significant variation observed during experimentation.

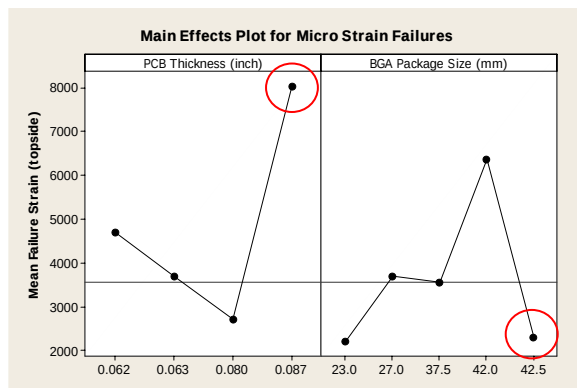


Figure 10: Main Effects Plot for PCB thickness and BGA Package Sizes Tested

Only minor differences were observed between surface finishes, PCB thicknesses, and BGA package sizes. An example main effects plot is shown in Figure 10 to illustrate the lack of trending observed in the data. Thick PCBs and large BGA package sizes did not behave in the same manner as the rest of the sample population.

Failure analysis of all specimens indicated that the primary failure mechanism during the test was found to be pad cratering as shown in Figure 11.

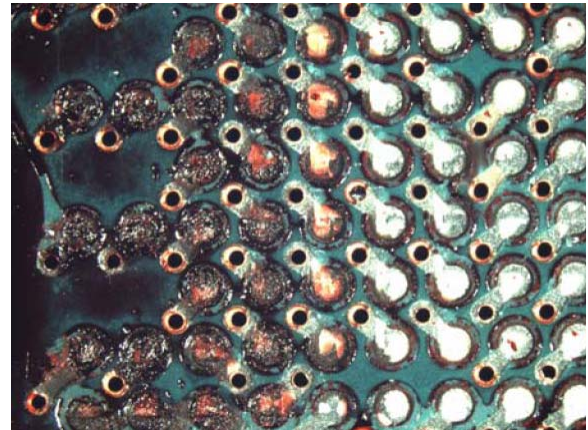


Figure 11: Example Pad Cratering Failure Mode

The results indicate that at the strain rates used, the copper pad to PCB laminate interface was weaker than the lead-free BGA interconnect solder joints.

Although there were minor differences in resulting strain levels observed across all tested samples, no significant link to system level reliability performance could be drawn.

IX. Test Value

One of the main objectives of this work was to assess the value of each test protocol examined as part of this study for use with high complexity, high reliability lead-free assembly constructions. The following sections discuss the benefits and drawbacks identified. Value contribution is also included based on a systems level reliability perspective.

A. Power Age Power Cycling

Several benefits of PA/PC were noted. Firstly, the test directly simulated actual system operating temperature gradients using lead-free assembled hardware. The thermal cycles used in this test were derived from actual heat duties created during power on / power off conditions of the system. While the test was able to closely simulate thermal gradients and peak temperatures, it must be noted that it *did not* simulate actual cyclic frequency and

isothermal dwell times of system operation in the field.

In comparison, when trying to predict thermal fatigue behavior using accelerated thermal cycling (ATC) protocols, there continues to be confidence and correlation issues when using acceleration factors (AFs) and models suitable for lead-free constructions. Prediction of actual system field performance when relying on these new AFs incurs higher risk. Therefore, the PA/PC test helps to provide additional insight on system field performance as lead-free predictive models continue to evolve. This alternate examination is especially helpful during this early transition period of high reliability Server/Storage products requiring reliability assessment prior to being put on the market.

Secondly, this PA/PC methodology can be used for any functional system. While a modular Blade Server system did cost effectively test multiple hardware configurations in this study, it is not a requirement. Power cycling experiments can be conducted on any product of interest.

Thirdly, the testing does not rely on interval testing of the product. Since product vehicles do not contain daisy chain nets for in-situ continuity monitoring, but rather functional circuit routings, product level ATC is often run with electrically functional (FCT) testing conducted at a fixed interval such as 250 cycles. If no failures are detected, the card is placed back in the thermal cycling chamber until the next interval checkpoint. This method has obvious limitations. The accuracy of the cycle count at card failure is limited by the functional test interval. For example, if a failure is detected at 500 cycles and the previous check point was at 250 cycles, the actual failure could have occurred any time between 251 to 500 cycles. PA/PC testing, on the other hand, more accurately determines the actual cycles of each event.

The main drawback of this test is that it can be very expensive. Blade Server testing for instance requires a full Blade hardware set including CPUs, memory, and hard drives. Complete firmware and software is required. Full chassis and rack systems are required. Sophisticated (custom) software is also required in the form of data exercisers, software timing controls, and data collection macros. All of these elements when added together can result in significant test expense.

Secondly, additional software programming skill is required for the development of this test. Advanced knowledge of firmware, operating systems, general programming, system control, and data generation are engineering prerequisites for conducting the test.

A final drawback to note is the longer test duration. ATC testing as per IPC 9701 is generally

run at one cycle per hour (1 CPH), with total test time to reach 1,000 cycles averaging 40-50 days (with check point FCT verification). In comparison, PA/PC also run at 1 CPH but a 2,500 cycle field requirement averages 105 days in test. Test time is therefore much longer for PA/PC; nearly 2.5 times longer than ATC. This extended time in test may not be suitable for some product introduction and qualification schedules.

B. Mini Cycling

At the time of publication evaluation of Mini Cycling is still in progress. With this in mind, the main benefit associated with this test protocol is to continue learning more about actual system reliability performance during smaller ΔT thermal cycles as generated by system power saving modes. Even at 3 CPH the main drawback of this test is again the extended time in test. For example, a 10,000 mini cycle checkpoint can take 140 days; while a 20,000 mini cycle checkpoint can take 280 days.

C. Four Point Bend Testing

No early brittle fractures were detected for any BGA samples studied. Significant displacements ($>10\text{mm}$) were required before any mechanical failures (pad cratering) occurred. This result is good news; well beyond the displacements typically found during printed circuit board assembly, test, and final box manufacturing steps [16] [17].

Despite these positive results, there were several drawbacks noted with this test from a system reliability perspective. Firstly, significant variability was observed across various PCB and BGA attributes. Since the primary response variable, PCB surface strain, does not have a unique and fixed relation to the imposed stress on package interconnects, measured failure strains can vary widely for different product applications. Proper usage would require a failure criterion unique for each combination of PCB thickness and package type.

Secondly, sample preparation required that the test card have all mechanical hardware removed along with excising the test specimen from the assembly. This process is often tedious, requiring patience and skill. The introduction of such mechanical forces likely contributes to the formation of micro cracks within solder joints further contributing to test variability.

Thirdly, the destructive nature of the test along with eight strain gauges per BGA test specimen makes the test expensive.

X. Conclusions

It is recommended that Power Age / Power Cycling and Mini Cycling be added as optional testing protocols to help assess lead-free system level reliability performance. The test (if affordable) is considered to be very valuable in assessing reliability risks thus improving confidence levels of system field operation. The test accurately simulated operating temperature gradients, but did not address frequency and isothermal dwell effects of the system. Since testing was conducted at a single accelerated frequency, effects of dwell and frequency were not identified. The effect of cyclic frequency in lead-free assemblies is a commonly recognized unknown within the electronics industry – an area clearly requiring additional study.

At our current level of understanding, the value of four point bend testing is considered low from a system level reliability perspective. With highly variable data output and numerous application dependent confounding effects, little linkage was found to actual system level performance. This relatively expensive (and destructive) test was deemed to have more drawbacks than benefits.

In conclusion, PA/PC and Mini Cycle testing assumes that there are still many unknowns with respect to system level reliability, while four point bend testing assumes that we understand when specific failure mechanisms may occur. This study has demonstrated that there is still much to learn regarding the assessment of lead-free high reliability, high complexity hardware systems. Continued testing simulating actual operating environments will help the industry learn more about the risks associated with converting high reliability systems to fully lead-free constructions.

Acknowledgements

The authors would like to sincerely thank the following people for their contributions to this work including Mark Hoffmeyer, Rick Dono, Jim Bielick, Marie Cole, Jim Wilcox, Joe Doman, Mark Stevens, Kim Wang, and Michk Huang.

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