

HotPak: A Tool For Rapid Thermal Mapping & Leakage Power Analysis of Flip-Chip Packages

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Abstract

In 2008 the Semiconductor Packaging group at Sun Microsystems published a technique for rapid thermal mapping of flip chip microprocessor/ASIC packages using analytical spectral superposition techniques. The primary focus of the current paper is to introduce a 100% pure Java application called HotPak, which embodies the analytical/computational engine from that paper, and to describe its multitude of features. HotPak has impressive benchmarks- on a typical laptop computer it takes less than 5 mins to do a complete thermal simulation for a microprocessor/ASIC layout with 10,000+ blocks. Since it is written in Java, it works flawlessly on Windows, Linux and MacOS. The predictions from the underlying engine have been verified experimentally via rigorous testing.

Keywords

Coolability, chip power fluctuation, thermal mapping, flip-chip

1. Introduction

Using the concepts of fourier spectral decomposition, an analytical 3D solution to the problem of conjugate heat transfer in flip chip electronic packages was published by the first and third authors in the IEEE Transactions of Components, Packaging & Manufacturing Technologies [1].

The interested reader is referred to [1] for details regarding the analytical solution. In this paper, we present a software tool called HotPak, which embodies the computational engine in [1] and describe its many features.

2. Software Features

HotPak is a 100% pure Java application. As such, it runs flawlessly in Windows, Linux, Solaris and MacOS environments. Here we describe the various functionalities and features of the software that are present in Rev. 2.11. At the IMAPS 2009 conference, demo(s) of the tool in action are expected to be available as part of the paper presentation.

HotPak, which is expected to be made available to the thermal community under open source licensing, has several features including the following:

- Multi-document interface so that multiple

parallel analyses on die floorplans can be conducted simultaneously ;

- Ability to specify geometries, material properties etc. in multiple units;
- Ability to specify TIM1/TIM2 material properties in tables or as specific values;
- Support to read in die floorplans in native flattened format as provided by chip design teams;
- Visualization of floorplan, power distribution and power density distribution in color, with ability to adjust ranges of power/density of interest;
- Export of visuals as high quality JPGs;
- Statistical characterization of the input floorplans to understand distributions of power and density over the die;
- Rapid thermal mapping of the die and case temperatures, and case flux;
- Visualization of die/case temperature and case flux distributions- including mouse gestures on the visualizations, and support for export of generated visualizations as high quality JPGs;
- Export of data in tabular form (for sources) and grid form for silicon reliability analysis;
- Sub-threshold leakage power analysis and associated thermal mapping

3. Graphical User Interface

HotPak supports the MDI or Multiple Document Interface paradigm. This permits the user to run multiple package thermal models simultaneously. Since HotPak supports software threading, all package models can run in tandem without the application hanging (Fig. 1).

Figure 2 shows the main application interface. A typical project pane has multiple tabs for model data entry and analysis. The first tab presented to the user is where model units are specified.

Figure 3 shows the Package tab. Here the various model parameters for the flip chip package are specified by the user. This includes material and geometry information for the silicon, TIM1 material, lid and heatsink.

Figure 4 shows the Blocks tab. Here the user specifies the flattened block layout data file that will be used for the analysis. Upon a successful read block information is loaded into tabular form that can be sorted, and various geometry/power summary statistics are reported.

Figure 5 shows the Floorplan tab. The loaded block data file can be represented visually as a floorplan here. Additionally, the Floorplan tab supports the visualization of the power distribution on the die, and the power density distribution also. Each representation can be exported separately as a high resolution JPEG image.

Figure 6 shows the Statistics tab. This tab supports the creation of histograms for the power and power density distribution on the die, i.e. it provided a means for understanding what percent of the blocks have a certain power/power density. This alternate visualization approach helps thermal designers compare the peak densities with the bulk values (total power/total area) and provide real-time feedback to chip designers. Again, the histograms can be exported as high-resolution JPEGs for archival/debug purposes.

Figure 7 shows the Die Thermal Map tab. In this tab the user conducts the thermal analysis of the selected floorplan in conjunction with the package model. As the simulation proceeds, a progress bar shows the status of the analysis. The resulting thermal map is displayed on the left part of the pane, and the block outlines can be selectively turned on/off as desired. As the mouse cursor moves over the die outline, the local temperature at the die is reported interactively along with the physical coordinates. The thermal map can be exported as a high resolution JPEG image, and the die temperatures can be exported as a gridded table for use in silicon reliability analysis by process technologists. Also, once a simulation is complete the tabular representation in the Blocks tab is updated with the temperatures at the geometric

center of each block in the layout.

Figures 8 and 9 are exact parallels of Fig. 7. Shown there are the Case Thermal Map and Case Flux Map tabs. As the names suggest, the user can determine the temperature distribution and the thermal flux distribution (respectively) at the package lid using these tabs in the tool. This data is often useful for sizing heatsinks for the cooling design.

Figure 10 shows the Leakage tab. This is a unique feature of HotPak which permits the real-time determination of leakage power distribution on the die using two models. In one, the user can specify leakage power at two distinct temperatures and in the alternative case, can directly specify the model parameters A & B. Either way, the leakage analysis proceeds iteratively and the results are shown interactively on the left portion of the pane. Once the leakage analysis completes, i.e. a converged estimate of the leakage power is determined, the simulation stops and the leakage power is reported.

Figure 11 shows the Leakage Thermal Map tab. This is where the user can determine the thermal map for the package considering the presence of leakage power (which would have been determined in the Leakage tab). In appearance and form/function, this tab is identical to the regular Die Thermal Map tab.

Whether the Die Thermal Map or Leakage Thermal Map tabs are used for analysis purposes, the determined package, TIM and sink thermal resistances R_{jc} , R_{cs} and R_{sa} are reported on the right hand portions of the respective tabs for ready reference.

4. Benchmarking

To compare the performance of the simulation engine in various application environments, the speed of the HotPak application was benchmarked on several compute platforms.

Table 1 summarizes the key findings; run times are under half an hour even for models with as high as 16,000 blocks/instances. It is noteworthy that the package designs with 6000, 11000 and 16000 block counts shown in Table 1 could not be simulated using conventional finite-element (FE) or finite-volume (FV) approaches- the granularity and close placement of cells posed severe challenges to the domain meshing and subsequent solution using FE/FV methods.

One interesting finding from the HotPak benchmarking effort is that the run times for the various models are largely independent of the underlying OS/architecture. This is consistent with the "write once/run anywhere" philosophy of the Java programming language which has been used to

develop HotPak. In fact, as Fig.12 shows, the key driver for the run times appears to be the resident memory installed in the compute platform of choice.

4. Concluding Remarks

In this study we have introduced a multi-faceted software application called HotPak which permits rapid 3D thermal analysis of flip chip packages, including leakage power analysis. It is anticipated that this tool will be available under open source licensing to the thermal community at large.

The benchmarks for HotPak's speed are impressive, and its underlying engine has been verified via extensive testing in the laboratory.

5. References

- [1] A Fourier Series-Based Analytical Solution for Three-Dimensional Conjugate Heat Transfer Problems in Microprocessor Cooling. Ankireddi, S.; Pecavar, S., IEEE Transactions on Components and Packaging Technologies, Volume 31, Issue 2, June 2008 Page(s):461 – 468

Table 1. HotPak Benchmarks

Machine	Linux Laptop	Linux Desktop	Windows PC
OS	Redhat Fedora Core 3	Redhat Enterprise Linux	XP Service Pack 2
CPU	Mobile AMD Athlon XP2500+	Intel Xeon	AMD Athlon XP2200
Architecture	32-bit	64-bit	32-bit
No. CPUs	1-way	2-way	1-way
Chip Speed	1.8 GHz	3.6 GHz	1.8 GHz
RAM	768 MB	8192 MB	512 MB
Swap Size	392 MB	2048 MB	OS Assigned
Wall time, 100 block model	< 2 min	< 2 min	< 2 min
Wall time, 6000 block model	5 min	3 min	9 min
Wall time, 11,000 block model	12 min	6 min	17 min
Wall time, 16,000 block model	17 min	10 min	26 min

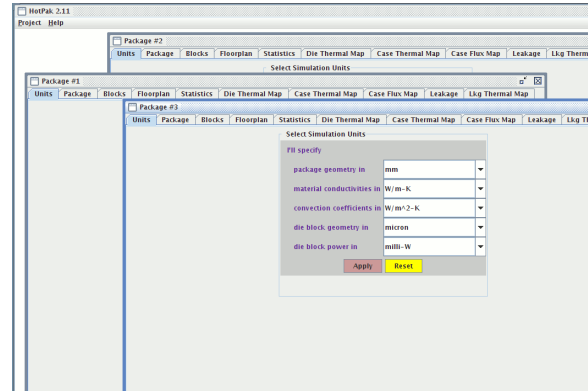


Fig. 1. HotPak's MDI (Multi Document Interface)

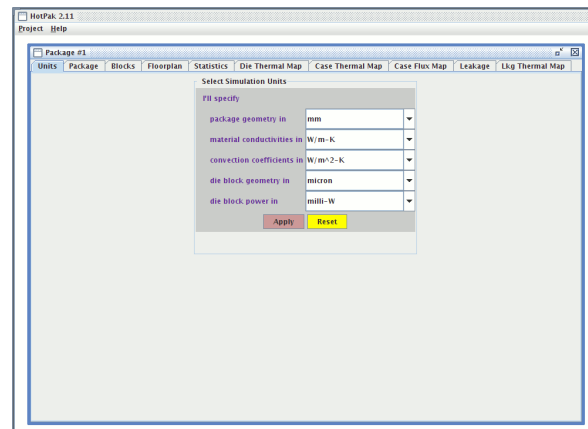


Fig. 2. Units Tab

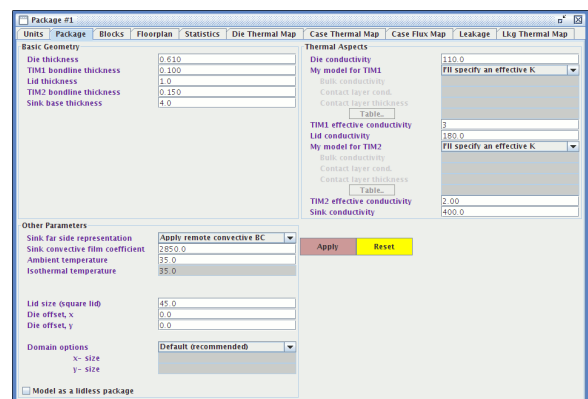


Fig. 3. Package Tab

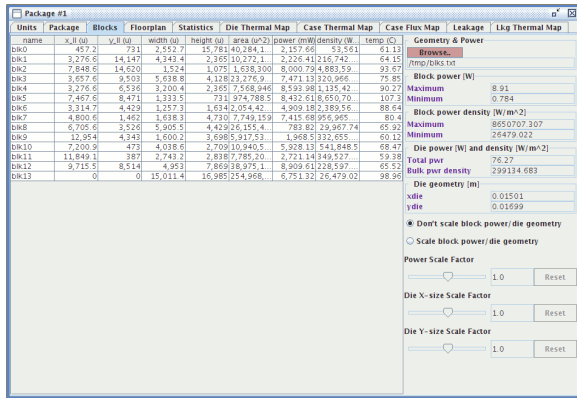


Fig. 4. Blocks tab

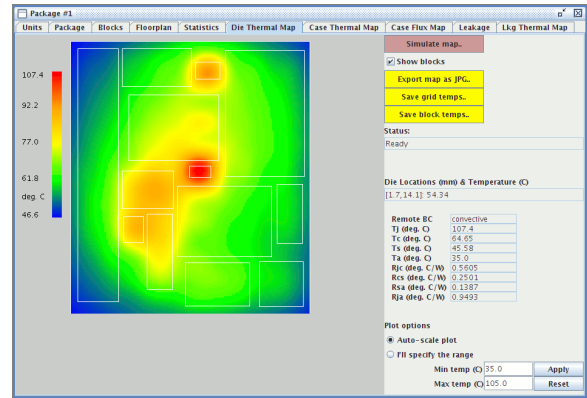


Fig. 7. Die Thermal Map tab

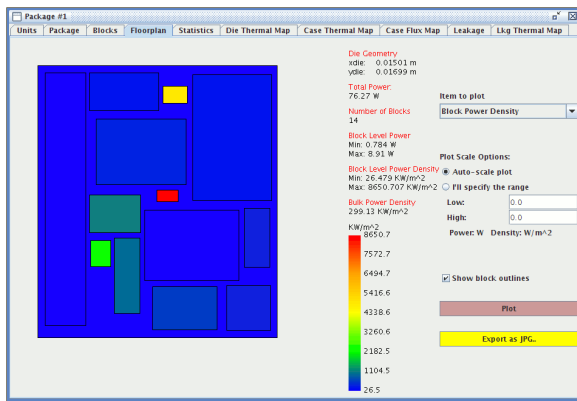


Fig. 5. Floorplan tab

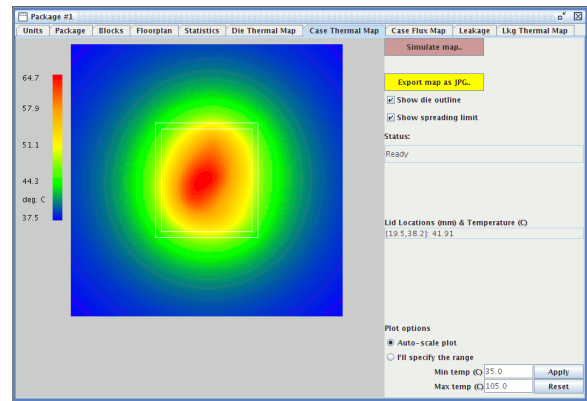


Fig. 8. Case Thermal Map tab

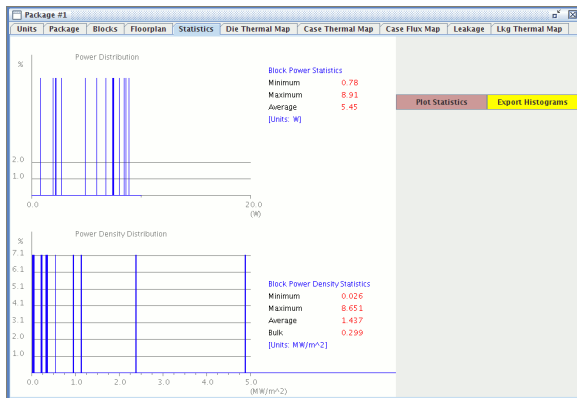


Fig. 6. Statistics tab

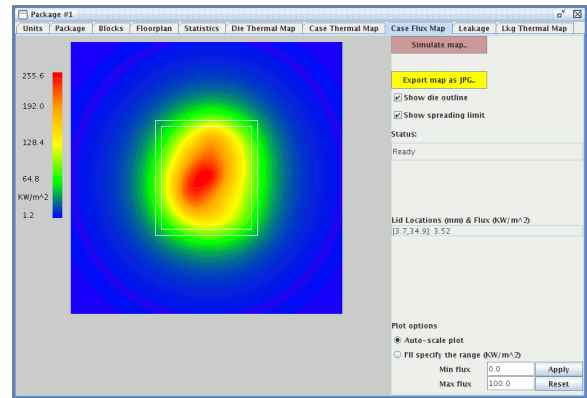


Fig. 9. Case Flux Map tab

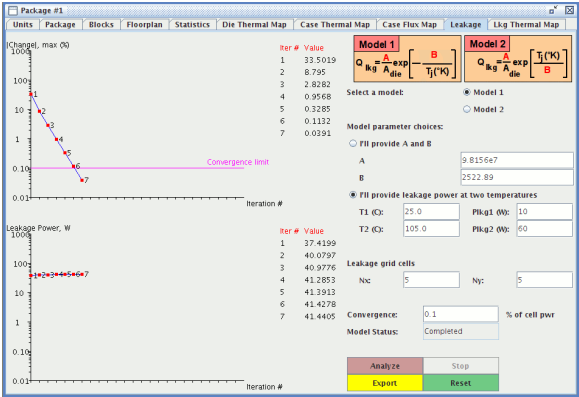


Fig 10. Leakage tab

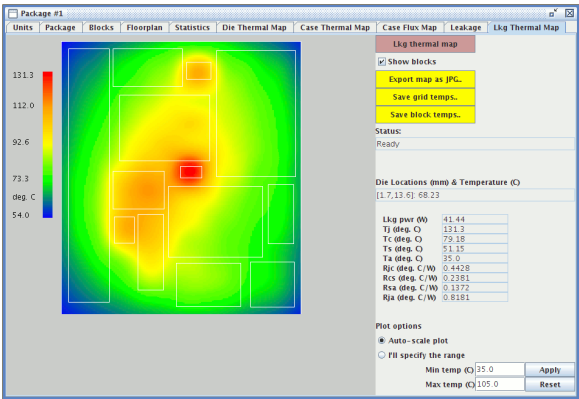


Fig. 11. Leakage Thermal Map tab

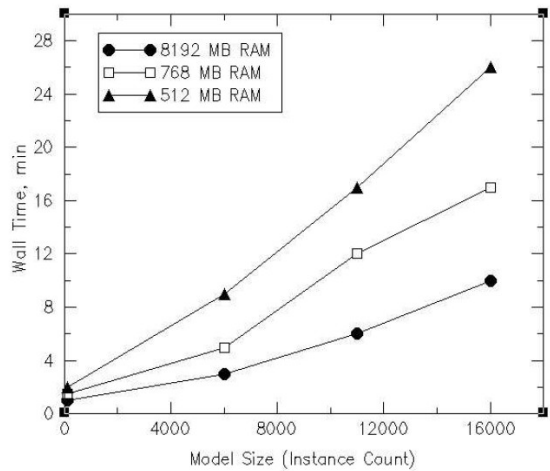


Fig. 12. HotPak benchmarks